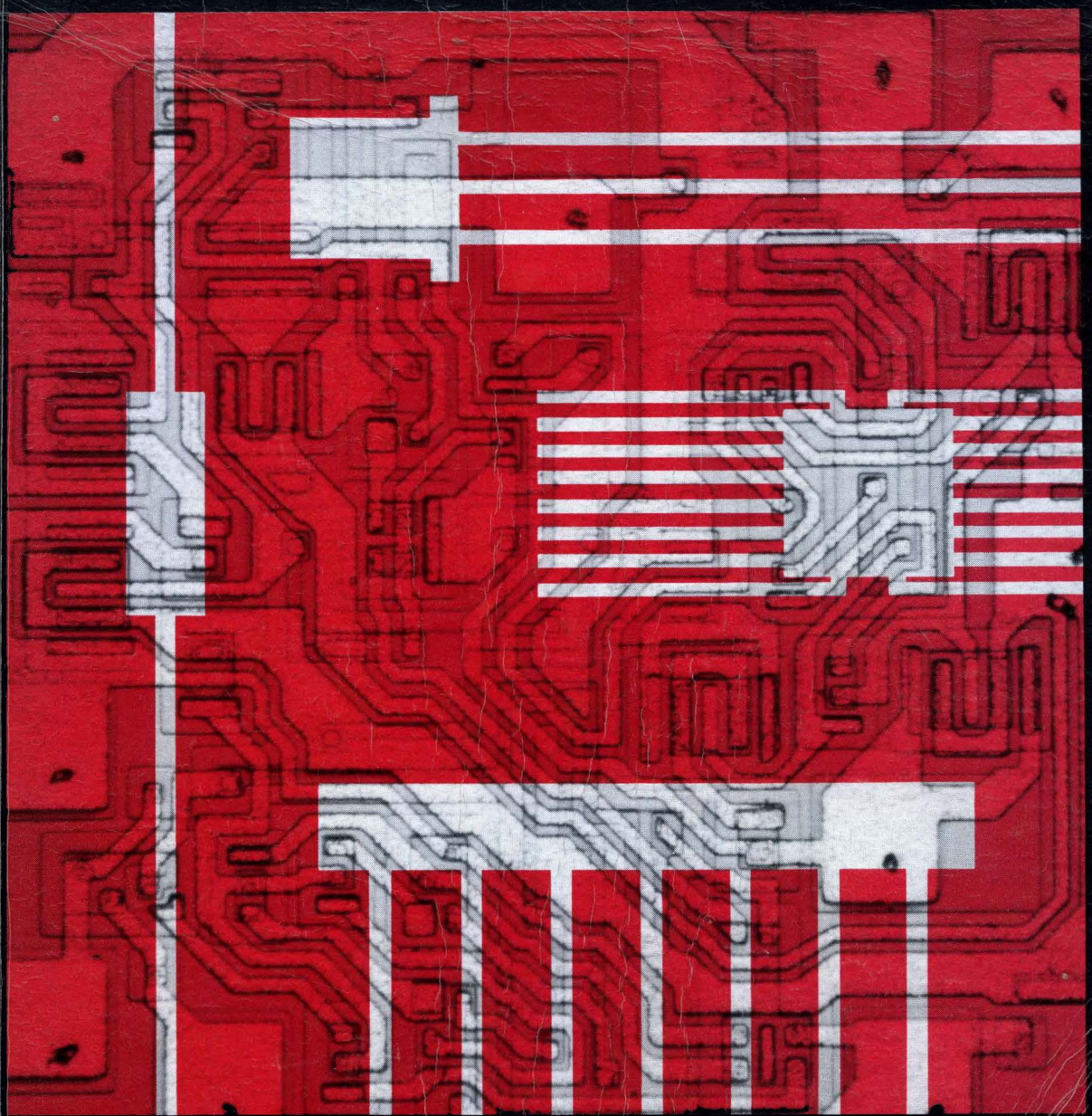
PRODUCT CATALOG 1972/1973

ITT SEMICONDUCTORS



PRODUCT CATALOG 1972/1973

ITT SEMICONDUCTORS

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725M72

Printed In U.S.A.

All ITT integrated circuits are available both in wafer and in chip form. Since the completed individual encapsulated product is capable of being more extensively and thoroughly tested than the wafer, these specifications are limited to the capability of the chip and the attendant testing equipment.

USE

DTL and Linear circuits are normally supplied with plain backing. Gold backing can be furnished upon special request. All other circuits are supplied with gold backing. Recommended die attach temperature is 420 °C for either type of backing. A 98% gold, 2% silicon preform is recommended for die attach with all plain-backed chips. One mil aluminum wire, ultrasonically bonded to the pads, is recommended for connecting the chip to the circuit.

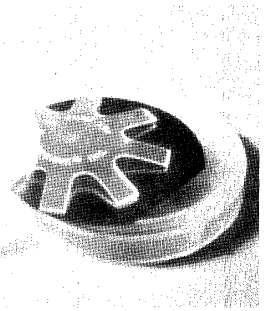
PACKAGING FOR SHIPMENT

Wafers will be shipped in the plastic package shown. Chips will be packaged in carriers as indicated.

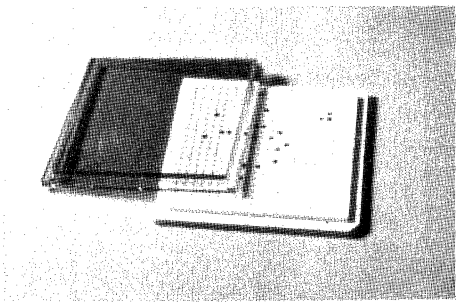
IDENTIFICATION

All integrated circuit dice will be identified by the appropriate three or four-digit code, together with the individual suffix number indicating the temperature range.

For example, a 930 limited-temperature range chip would be a "930-5." A 930 full-temperature range chip would be a "930-1."



I. C. WAFER PACKAGE



CHIP PACKAGE

MIL AND HI-REL SEMICONDUCTORS

Virtually all ITT Semiconductors are available with hi-rel processing. IC's, for example, can be processed for any portions of, or all of, MIL-STD-883 and MIL38510. Many diodes and transistors are available as JAN, JAN/TX, or MIL types.

Whenever you need hi-rel semiconductors, check ITT. Your local representative can give up-to-date information on availability, price, etc.

This series offers a wide range of digital integrated circuit devices from simple NAND gates to large complex functions. They form a TTL family (Transistor-Transistor Logic) guaranteed to operate over the following ambient temperature ranges:

Military range, 54 series	−55°C to 125°C
Industrial range, 74 series	0°C to 75°C

All devices operate over a frequency range between D.C. and typically 20 MHz, and are fully compatible with all 54/74 series TTL and 930 series DTL.
Clamping diodes are provided at the inputs to enhance the inherent high noise immunity when driving transmission lines. Most outputs are of totem pole configuration to give good drive capability, i.e. high fan-out, especially into large capacitive loads. Other outputs include an open-circuit collector connection.

FEATURES

High speed—typical propagation delay (gate) of 9 ns.
Guaranteed noise margin—greater than 400 mV.
Low power dissipation—10 mW per gate at 50% duty cycle.
Worst case fan-out of 10.
Low output impedance.
Logic levels guaranteed over range of supply voltage and operating temperature
Wide range of functions—many SSI and MSI functions.
Compatible with other DTL, TTL logic series.

INDEX FOR STANDARD 7400 SERIES

For the military range, replace 74 in the type number by 54.

TYPE	DESCRIPTION
ITT7400	Quad 2 i/p NAND
ITT7401	Quad 2 i/p NAND (open-collector 5-5 V rating)
ITT7401A	Quad 2 i/p NAND (open-collector 15 V rating)
ITT7402	Quad 2 i/p NOR
ITT7403	Quad 2 i/p NAND (open-collector 5-5 V rating)
ITT7403A	Quad 2 i/p NAND (open collector 15 V rating)
ITT7404	Hex inverter
ITT7405	Hex inverter (open-collector 5-5 V rating)
ITT7405A	Hex inverter (open-collector 15 V rating)
ITT7406	Hex inverter buffer/driver (open-collector 30 V rating)
ITT7407	Hex buffer/driver (open-collector 30 V rating)
ITT7410	Triple 3 i/p NAND
ITT7412	Triple 3 i/p NAND (open-collector 5 V rating)
ITT7412A	Triple 3 i/p NAND (open-collector 15 V rating)
ITT7413	Dual 4 i/p Schmitt Trigger
ITT7416	Hex inverter buffer/driver (open-collector 15 V rating)
ITT7417	Hex buffer/driver (open-collector 15 V rating)
ITT7420	Dual 4 i/p NAND
ITT7426	Quad 2 i/p high voltage interface NAND (open collector
ITT7428	Quad 2 i/p NOR buffer
ITT7430	8 i/p NAND
ITT7437	Quad 2 i/p NAND buffer
ITT7438	Quad 2 i/p NAND buffer (open collector 5.5 V rating)
ITT7440	Dual 4 i/p NAND Buffer
ITT7441A	B.C.D. to decimal decoder/driver
ITT7442	B.C.D. to decimal decoder
ITT7443	Excess 3 to decimal decoder
ITT7444	Excess 3 gray to decimal decoder
ITT7445	B.C.D. to decimal decoder (open collector 30 V rating)
ITT7450	Expandable dual 2 wide, 2 i/p A.O.I.
ITT7451	Dual 2 wide, 2 i/p A.O.I.
ITT7453	Expandable 4 wide, 2 i/p A.O.I.
ITT7454	4 wide, 2 i/p A.O.I.
ITT7460	Dual 4 i/p expander
ITT7470	D.C. clocked J-K flip-flop
ITT7472	J-K master-slave flip-flop
ITT7473	Dual J-K master-slave flip-flop
ITT7474	Dual D-type edge-triggered flip-flop
ITT7475	Quad bistable latch
ITT7476	Dual J-K master-slave flip-flop with preset and clear
ITT7480	Gated full adder
ITT7481	16-bit full memory
ITT7482	2-bit full adder
ITT7483	4-bit full adder
ITT7484	16-bit memory
ITT7486	Quad 2 i/p exclusive—OR
ITT7490	Decade counter
ITT7491A	8-bit shift register
ITT7492	Divide by 12 counter
ITT7493	4-bit binary counter
ITT7494	5-bit shift register
ITT7495	4-bit shift register (reversible)
ITT7496	4-bit shift register
ITT74104	Gated J-K master-slave flip-flop (see ITT9000)

TYPE	DESCRIPTION
ITT74105	Gated J-K master-slave flip-flop (see ITT9001)
ITT74107	Dual J-K master-slave flip-flop
ITT74118	Hex set/reset latch
ITT74121	Monostable
ITT74145	B.C.D. to decimal decoder (open-collector 15 V rating)
ITT74150	16-bit data selector/multiplexer
ITT74151	8-bit data selector/multiplexer
ITT74154	4-line-to-16-line decoder/demultiplexer (see ITT9311)
ITT74155	Dual 2 to 4 line decoder/demultiplexer
ITT74156	Dual 2 to 4 line decoder/demultiplexer (o/c 5-5V rating)
ITT74161	Synchronous binary up counter (see ITT9316)
ITT74180	8-bit parity generator/checker
ITT74192	Synchronous BCD-Up/Down counter
ITT74193	Synchronous Binary 4-bit up/down counter

FUNCTIONAL INDEX

Gates

FUNCTION	TYPE
NAND	ITT7400
	ITT7401*
	ITT7401A*
	ITT7403*
	ITT7403A*
	ITT7410
	ITT7412
	ITT7412A
	ITT7420
	ITT7426*
	ITT7430
	ITT7437
	ITT7438
	ITT7440
NOR	ITT7402
	ITT7428
Inverter	ITT7404
	ITT7405*
	ITT7405A*
	ITT7406
	ITT7416
Non-Inverter	ITT7407
	ITT7417
Schmitt Trigger	ITT7413
And-Or-Invert (A.O.I.)	ITT7450
	ITT7451
	ITT7453
	ITT7454
Expander	ITT7460*
Exclusive OR	ITT7486

Flip-flops

FUNCTION	TYPE
J-K	ITT7470
	ITT7472
	ITT7473
	ITT7476
	ITT74104
	ITT74105
	ITT74107
D-type	ITT7474
Latch	ITT7475
	ITT74118

Counters

Decade	ITT7490
Divide by 12	ITT7492
	ITT74192
Divide by 16	ITT7493
	ITT74161
	ITT74193

Shift registers

4 Bit	ITT7494
	ITT7495
5 Bit	ITT7496
8 Bit	ITT7491A

Memories

16 Bit RAM	ITT7481
	ITT7484

Decoders/demultiplexers

B.C.D. to decimal	ITT7441A*
	ITT7442
	ITT7445*
	ITT74145*
Excess 3 to decimal	ITT7443
Excess 3 gray to decimal	ITT7444
4 Line to 16 line	ITT74154
2 Line to 4 line	ITT74155
	ITT74156*

Data selector/multiplexer

16 Bit	ITT74150
8 Bit	ITT74151

Adders

2 Bit	ITT7482
4 Bit	ITT7483
1 Bit	ITT7480

Monostable — ITT74121

Parity gen/check

8 Bit	ITT74180

*Devices with open collector outputs.

INTRODUCTION TO TTL

The TTL circuit configurations are designed so that the uniform logic and noise margin levels apply to all the standard devices in the families. Thus many parameters and their limits are common. In addition the operating conditions are identified for each family. Once these standard operating conditions are understood it becomes possible for the designer to use the family by simply referring to the logic and connection diagrams on each data sheet. All common information is included in the remainder of this section.

For ease of reading, the data only refers to the ITT7400 series family but it is equally applicable to the ITT5400 series. Where there are exceptions these are clearly indicated on the individual data sheets concerned.

LOGIC DEFINITION

Positive logic is used throughout the data sheets. This is defined as follows.

Logical '0' = Low voltage; typically 0.2 V but $\langle$ 0.8 V
Logical '1' = High voltage; typically 3.3 V but $\rangle$ 2.0 V

Current flowing into a device terminal is defined as positive.

D.C. CHARACTERISTICS COMMON TO ALL DEVICES (except where otherwise stated)

D.C. tests are carried out under the specified conditions. All inputs and outputs are tested for all possible logic states. Worst state load currents and voltages are applied and the test limits are applicable over the full temperature range.

	Min.	Max.	Unit
Supply voltage, V_{CC}:			
74 series	4.75	5.25	V
54 series	4.5	5.5	V
Operating temperature:			
74 series	0	75	°C
54 series	−55	125	°C

D.C. noise margin typically greater than 1V.

ABSOLUTE MAXIMUM RATINGS

(above which the useful life of the device may be impaired)

Continuous supply voltage V_{CC} (Note 1) 7V
Input voltage . . . . . 5.5 V
Voltage between inputs . . . . . 5.5 V
Continuous input current . . . . . −10 mA
Standard output voltage . . . . . −0.5 to 5.5 V
Storage temperature . . . . . −65°C to 150°C

Note I
This rating is reduced to 5.5 V if unused inputs are connected directly to V_{CC}.

STANDARD CHARACTERISTICS (limits apply over the full range of operating temperature and for standard totem pole output except where otherwise stated).

PARAMETER — LIMIT (Note 8) — CONDITIONS

	Min.	Typ.	Max.	Unit	V_{CC}	
V_{IH}	2.0			V	Min.	$V_{OL}\langle$0.4V or $V_{OH}\rangle$2.4V (Note 1)
V_{IL}			0.8	V	Min.	$V_{OL}\langle$0.4V or $V_{OH}\rangle$2.4V (Note 2)
V_{OL} (standard output)		0.22	0.4	V	Min.	I_{OL}=16 mA, V_{IH}=2V or V_{IL}=0.8V (Note 3)
V_{OL} (buffer output) V_{OH}	2.4	3.3		V	Min.	V_{IL}=0.8V or V_{OH}=2.0V (Note 4)
I_{CEX} open collector only			250	µA	Min.	V_{IL}=0.8V, V_{IH}=2V, V_{OUT}=max. o/p voltage rating
$-I_F$		1.0	1.6	mA	Max.	V_F=0.4V (Note 5)
I_R			40	µA	Max.	V_R=2.4V, input loading-1 unit load (Note6)
I_R			1.0	mA	Max.	V_R=5.5 V irrespective of input loading
$-I_{SC}$						
54 series	20		55	mA	Max.	V_{OUT}=0 V (Note 7)
74 series	18		55	mA	Max.	V_{IH}=2.0V or V_{IL}=0.8V; apply according to logic function

Where characteristics for devices differ from the above table these are shown in the data sheets.

Note 1
Condition at outputs dependent on the truth table of the device. For example, for gates and buffers, V_{OL} < 0.4 V applies, and for flip-flops, shift registers, counters, decoders, etc. either V_{OL} < 0.4 V or V_{OH} > 2.4 V applies at each output. Output conditions do not apply for 7486, 7460, 7445, 74145, and 7441A. This parameter does not apply for 7413 and 74121, because of the Schmitt trigger inputs.

Note 2
Conditions at outputs dependent on the truth table of the device, for example; for gates and inverters V_{OH} > 2.4 V. Output conditions do not apply for devices with open collector output. This parameter does not apply for 7413, 74121.

Note 3
Conditions V_{IH} and V_{IL} depend on device truth table. Limits for 7441A, 7445 and 74145 are shown on the appropriate data sheets.

Note 4
This parameter for totem pole output devices only. V_{IL} and V_{IH} apply according to the truth table. I_{OH}=−400 μA for devices with Fan-out=10; I_{OH}= −800 μA for devices with Fan-out=20; I_{OH} = −1.2 mA for devices with Fan-out=30, etc.

Note 5
Limits apply for an input loading of 1 unit load; for other input loadings multiply limits by number of unit loads. For flip-flops, see appropriate data for test conditions.

Note 6
All other inputs at 0 V for 7472, 7473, 7476, 74107. For 7470 all other inputs at 0 V except J and K which are at 4.5 V. For 7474 consult data sheet. Limits to be multiplied by the input loading of the device.

Note 7
Maximum limit = 57 mA for devices with internal feedback connections, (e.g. flip-flops and some complex devices). For 7400 series simple NAND gates not more than two outputs may be shorted at any time. For all other devices and for all 5400 series not more than one output to be shorted at any time. Open collector devices: no parameter for $-I_{SC}$.

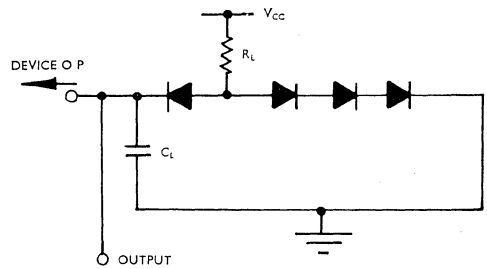
Note 8
Typical limits are at ambient temperature, T_A=25°C and V_{CC}=5 V.

A.C. TESTS

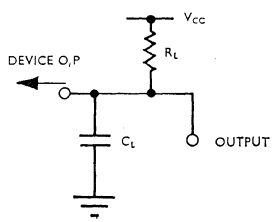
Testing of propagation delays is carried out using the typical switching load circuits shown below. These load circuits are designed to simulate full fan-out loading. An oscilloscope with high impedance probes and having a bandwidth of at least 100 MHz is suitable for these measurements.

TYPICAL SWITCHING TEST LOAD CIRCUITS

For totem pole outputs:



For open collector outputs:



ORDERING CODE FOR TTL CIRCUITS

Operating Temperature Range
5400 series −55 to +125°C
7400 series 0 to +75°C

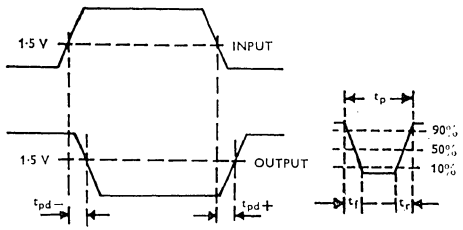
Package (add)
B for Flat Pack
J for Ceramic Dual In-Line
N for Plastic Dual In-Line

Example:
ITT7400J
is 0°C to +75°C Range in Ceramic Dual In-Line Package

Notes

1. Diodes are type 1N4148.
2. The values of C_L and R_L are quoted in the data sheets. Value of C_L includes probe and jig capitance.
3. The characteristics of the pulse generator used at the input of the device are stated in the data sheets. Typical characteristics are: V_{OUT}=3.5V; Rise time, tr, =Fall time, t_f,=less than 15 ns; Zo = 50 Ω; Pulse Repetition Frequency, P.R.F. = 1 MHz; Pulse width for gate, t_p = 500 ns.

Waveforms



1. HIGH LOGIC STATE '1' (ON STATE)

The NAND gate has two stable operating states. These are illustrated in Figs. 1A and 1B.

Fig. 1A. Typical 'ON' conditions with all inputs Logic '1'.

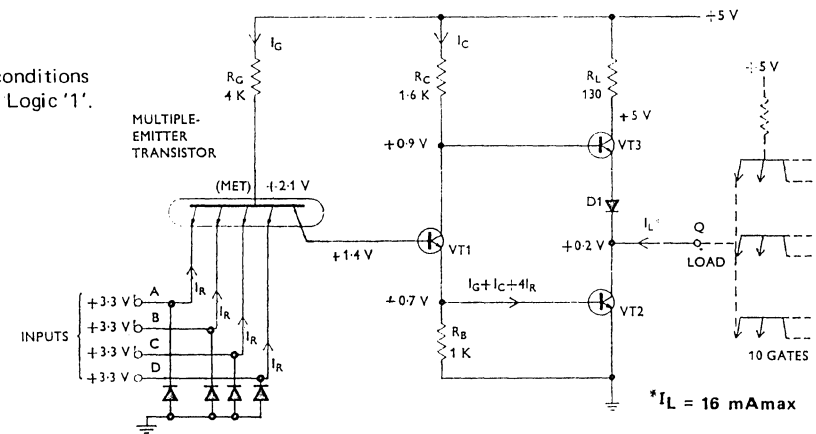
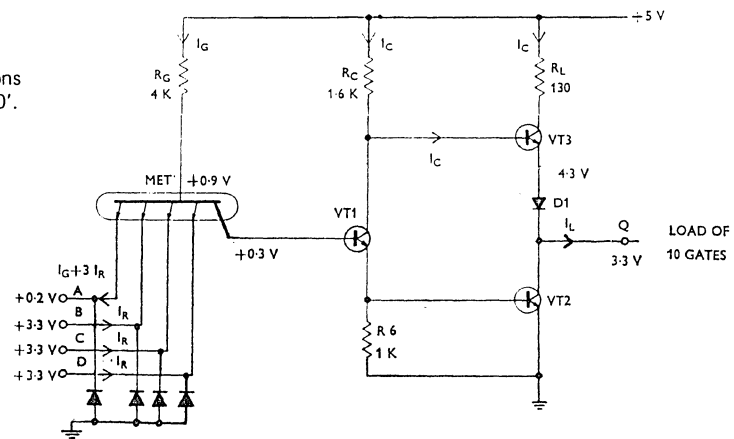
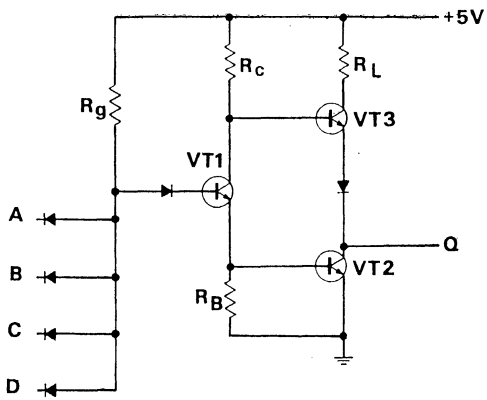


Fig. 1B. Typical 'OFF' conditions with one input Logic '0'.



The d.c. operation of this circuit is more readily understood if the multiemitter transistor (MET) connecting the inputs is considered equivalent to a diode AND gate in series with an offset diode connected to the base of transistor VT1. This is shown in Fig. 2, the emitter-base junctions of the MET forming the input diodes and the collector-base junction forming the offset diode.

Fig. 2. Simplified analogy of TTL gate.



When all the inputs are positive a logic '1' current flows from the positive supply through R_g into the base of VT1 which heavily conducts and turns VT2 'ON' into the saturated state. Since both VT1 and VT2 are saturated, there is insufficient voltage across the base emitter terminals of VT3 to render it conducting. The output voltage is about +0.2 V, (i.e. saturation voltage of VT2). The collector current of VT2 will consist of the total 'sinking' current from the gates connected to the output terminal. When the base current drive to VT2 is high, VT2 can remain saturated even with a large collector current, with adverse circuit tolerances and temperature variations. This permits a fan-out of up to 10. With a multiemitter transistor, more current flows from a positive held input than with a conventional D.T.L. gate (the leakage current of the reverse biassed input diode) since the MET is biassed in the inverted mode and the functions of emitter and collector are reversed. However, the MET is designed to have a very low inverse gain and I_R is kept to a minimum. I_R will equal the emitter base leakage current plus the product of inverse current gain and I_G.

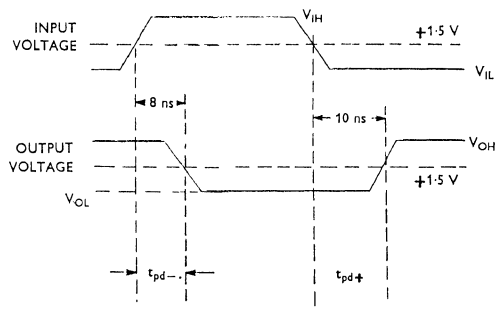
2. LOW OR OFF STATE

The opposite state shown in Fig. 1B is achieved if the voltage of any number of inputs is reduced below a threshold level of about + 1.5 volts. Fig. 1B shows the conditions when input A is at +0.2 volts (a typical output voltage of a previous gate). No base current flows into VT1 since the collector of the MET is at too low a potential, with respect to its base.
Therefore, no current will flow through VT1 and VT2 other than leakage current (which can be neglected in this analysis). The transistor VT3 will conduct to provide sufficient output current to maintain following gates connected to the output terminal at 3.3 V positive in logic 1. The fan-out is high (10) under worst case conditions because of the low output impedance of VT3.

3. CHANGEOVER BETWEEN STATES

The transistor action of the MET considerably improves the switching speed when compared with a DTL gate. In switching from the ON to the OFF state the MET saturates and rapidly removes the charge stored in VT1 turning it off. Then VT2 begins to turn off and VT3 turns on as the collector potential of VT1 rises. VT3 assists VT2 to turn off and pulls the output terminal rapidly positive, charging any load capacitance. The diode D1 helps to prevent VT2 and VT1 from conducting simultaneously and RL limits the current through VT3 to a safe value during the switch over if the output terminal is accidentally shorted.

Fig. 3. Propagation delay waveforms.



Switching from the OFF to the ON state is more rapid than ON to OFF since none of the transistors VT1, VT2 and MET are saturated in the OFF condition. The switch to the ON condition is particularly fast owing to additional drive by transistor VT1 in turning on VT2. Fig. 3 shows the typical switching times from this gate.

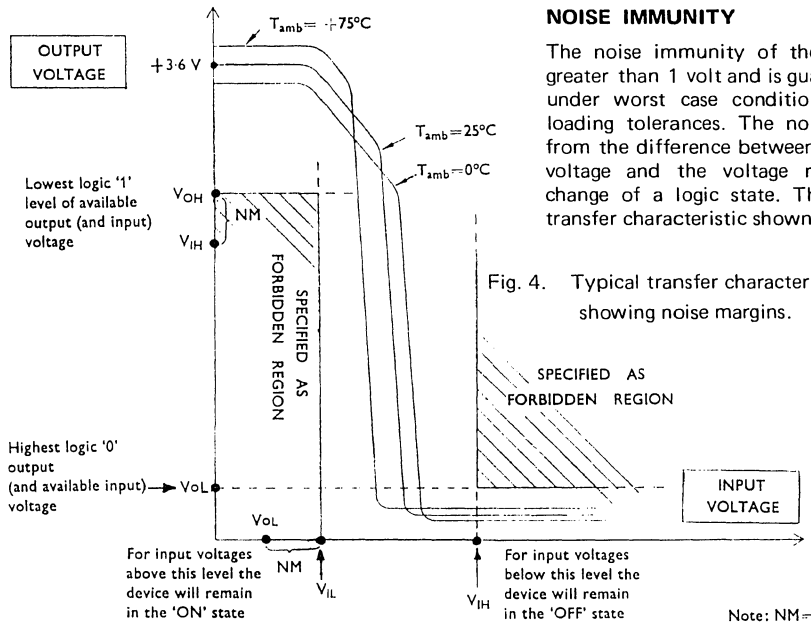


Fig. 4. Typical transfer characteristic showing noise margins.

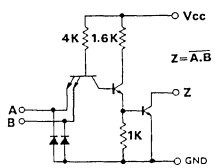
NOISE IMMUNITY

The noise immunity of the TTL gate is typically greater than 1 volt and is guaranteed 0.4 V minimum under worst case conditions for temperature and loading tolerances. The noise immunity is derived from the difference between extreme limits of input voltage and the voltage required to ensure the change of a logic state. This is illustrated by the transfer characteristic shown in Fig. 4.

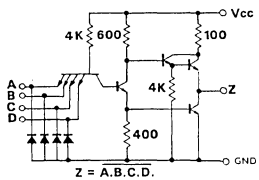
GATES DIFFERING FROM THE STANDARD CIRCUIT

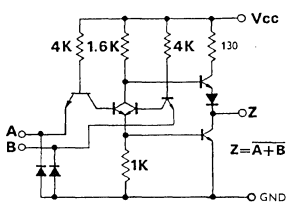
Typical variations from the standard NAND gate circuit configuration are shown in the following circuit diagrams.

Open collector (e.g. 7401)



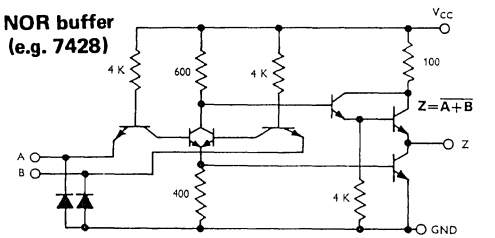
NAND buffer (e.g. 7440)

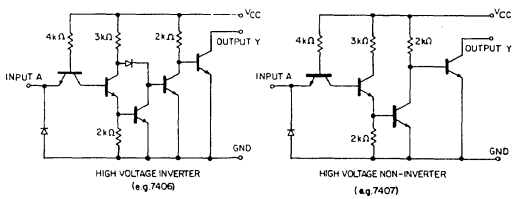




NOR gate (e.g. 7402)

NOR buffer (e.g. 7428)





BASIC RULES FOR THE USE OF TTL DEVICES

1. Spare inputs should be connected to used inputs if the fan-out permits. Otherwise connected to the V_{CC} power line via a resistor of value 1 K ohm or greater. This is particularly important for the 'preset' and 'clear' asynchronous inputs.
2. Gates from the same package may be paralleled where necessary for better driving capability.

3. Interconnection lengths of 12 inches or less (capacitance of about 50 pF) are unlikely to give ringing problems; lengths up to 24 inches are possible with good ground arrangements. Greater length will probably require line driving precautions (see separate Application Note).
4. 'Wired-OR' can be performed at the output terminals of open-collector networks however a speed penalty is incurred by the introduction of a resistive pull-up.
5. In calculating system speeds, due allowance should be made for the maximum set-up and minimum clock pulse width times on flip-flops, as well as the propagation delays of the elements used.
6. If relays are driven from TTL circuitry, care must be taken to ensure that the load connection wires to the relay contacts do not introduce noise into the logic system. This can be done by allowing these wires only to enter the logic system enclosure at a point close to the relay contacts, or in extreme cases by also shielding the relay.
7. Similarly external inputs should be brought on to the printed circuit connections at right angles to the other wiring, the printed circuit itself being laid out to ensure least coupling between inputs and other connections.
8. If system speed is high, allowance should be made when calculating power supply requirements for the increased network supply currents due to current spiking and line driving. An allowance at 10 MHz of 15% for spiking and up to 0.5 mA per each gate node for the line driving will be adequate for this.
9. Decouple every 10 gates or their equivalent in MSI functions with 0.01 μF to 0.1 μF capacitors of R.F. rating.

In conclusion, a careful perusal of the data sheet together with the points mentioned above, will help in achieving a trouble free logic design at the first attempt.

DRIVING DTL LOGIC FROM TTL DEVICES

When driving ITT930 series DTL from 74/5400 series TTL the full fan-out of the TTL is available.

DRIVING TTL LOGIC FROM DTL DEVICES

Driving ITT7400 series TTL from ITT930 series DTL necessitates a reduction of the full fan-out from 8 to 3 for standard gates and from 25 to 20 for buffers. Increased fan-out can be achieved with standard DTL gates by using an additional pull-up resistor.

SYMBOLS AND THEIR DEFINITIONS

C_L	Load capacitor in switching test circuit (includes probe and jig capacitance).
Fan-out	Number of unit loads an output can drive.
f_{max}	Maximum clock frequency.
I_{CCH}	Supply current for highest dissipation logic state.
I_{CCL}	Supply current for lowest dissipation logic state.
I_F	Input forward current.
I_R	Input reverse current.
I_{SC}	Output short circuit current.
I_{CEX}	Output leakage current.
I_{OL}	Low state output current.
I_{OH}	High state output current.
I_{CC}	Supply current.
I_{IN+}	Input current at V_{T+}.
I_{IN-}	Input current at V_{T-}.
P_{dyn}	Dynamic power dissipation.
R_L	Load resistor in switching test circuit.
T_A	Ambient temperature.
t_h	Input hold time.
t_{h+}	Logical '1' hold time.
t_{h-}	Logical '0' hold time.
t_{cp}	Clock pulse width.
t_p	Preset or clear pulse width.
t_{po}	Output pulse width.
t_{pd+}	Propagation delay to logical '1' on output.
t_{pd-}	Propagation delay to logical '0' on output.
t_n	State of output (or input) before the active edge of the clock pulse.
t_{n+1}	State of output (or input) after the active edge of the clock pulse.
t_{min}	Minimum width trigger pulse.
t_{sp+}	Logical '1' input set up time.
t_{sp-}	Logical '0' input set up time.
V_{CC}	Supply voltage.
V_H	Hysteresis voltage.
V_{IH}	Input high voltage to ensure V_{OL} (or V_{OH})*.
V_{IL}	Input low voltage to ensure V_{OH} (or V_{OL})*.
V_{OL}	Output low voltage.
V_{OH}	Output high voltage.
$V_{OH(M)}$	Output breakdown voltage of open collector device.
V_{IN}	Voltage at an input.
V_{OUT}	Voltage at an output.
V_{T+}	Positive edge threshold voltage.
V_{T-}	Negative edge threshold voltage.
WIRED-OR	The commoning of open collector outputs with a pull-up resistor to perform the AND function.

***Output level dependent on device logic as found from truth table.**

ITT7400	Quad 2 input NAND gate
ITT7401, ITT7401A	Quad 2 input NAND gate with open collector output
ITT7402	Quad 2 input NOR gate
ITT7403, ITT7403A	Quad 2 input NAND gate with open collector output
ITT7404	Hex inverter
ITT7405, ITT7405A	Hex inverter (open collector)
ITT7406	Hex inverter/buffer/driver (open collector)
ITT7407	Hex buffer/driver (open collector)
ITT7410	Triple 3 input NAND gate
ITT7412	Triple 3 input NAND gate (open collector)
ITT7412A	Triple 3 input NAND gate (open collector)
ITT7416	Hex inverter/buffer/driver (open collector)
ITT7417	Hex inverter/driver (open collector).
ITT7420	Dual 4 input NAND gate
ITT7426	Quad 2 input high voltage interface NAND gate (open collector)
ITT7428	Quad 2 input NOR buffer
ITT7430	Single 8 input NAND gate
ITT7437	Quad 2 input NAND buffer
ITT7438	Quad 2 input NAND buffer (open collector)
ITT7440	Dual 4 input NAND buffer

DESCRIPTION

ITT7400, ITT7410, ITT7420, ITT7430, ITT7440 are standard totem pole output gate devices.
ITT7401(A), ITT7403(A), ITT7405(A), ITT7412(A), ITT7438 are open collector output devices featuring:

Wired or capability
Output rating 5.5V - Suffix "A" denotes 15V

ITT7406, 7416, 7407, 7417 are high voltage open collector devices featuring:

Output rating 30V (54/7406, 54/7407),
15V (54/7416, 54/7417)
Sink current 40 mA (7406, 07, 16, 17),
30 mA (5406, 07, 16, 17)

ITT7426 is an open collector device featuring:

Wired or capability
Output rating 15V
Low I_{CEX}
} **Suitable as MOS interface device**

ITT7437, 7438, 7440 is a NAND buffer featuring a FAN OUT OF 30.
ITT7402 is a NOR gate with standard totem pole output.
ITT7428 is a NOR buffer featuring: FAN OUT OF 30.

The circuits of all these devices are the same as those shown in the general information section, except some have a different number of inputs.

TYPICAL CHARACTERISTICS

Device type		Propagation delay ns	Power dissipation per package (50% duty cycle) mW
Quad 2 input NAND	7400	9	40
Triple 3 input NAND	7410	9	30
Dual 4 input NAND	7420	9	20
Single 8 input NAND	7430	9	10
Open collector 2 input NAND	7401,01A	22	40
	7403,03A	22	40
	7412,12A	22	40
Quad 2 input interface NAND	7426	22	40
Hex inverter	7404	9	60
Open collector Hex inverter	7405(A)	24	60
	7406,16	15	105
	7407,17	14	145
Dual 4 input NAND buffer	7440	9	53
Quad 2 input NAND buffer	7437	10	107
Quad 2 input NAND buffer (Open Collector)	7438	12	93
Quad 2 input NOR gate	7402	9	55
Quad 2 input NOR buffer	7428	9	100

Input loading factor . . . . . 1 unit load

Fan out (for totem pole outputs):
- Standard gates . . . . . 1 to 10 unit loads
- Buffer gates . . . . . 1 to 30 unit loads

7406, 07, 16, 17 . . . . . 40 mA Sink Current
7406, 07, 16, 17 . . . . . 30 mA Sink Current

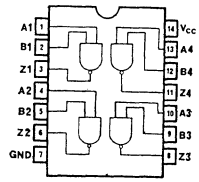
Output voltage rating for
- open collector outputs 5.5V

Except those with suffix A
- and 7426, 7416, 7417 . . . . . 15.0V

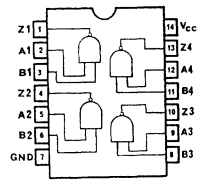
Except 7406, 7407. . . . . 30.0V

Pin configuration (top view)

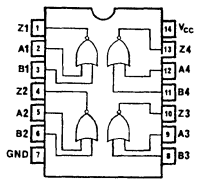
7400, 7403, 7403A, 7426, 7437, 7438



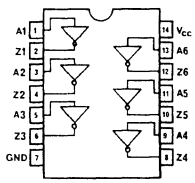
7401, 7401A



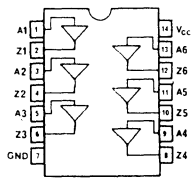
7402, 7428



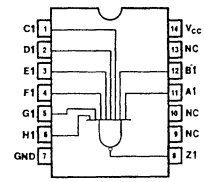
7404, 7405, 7405A, 7406, 7416



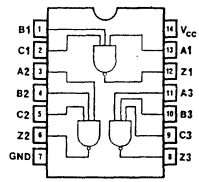
7407, 7417



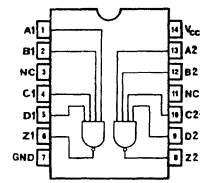
7430



7410, 7412, 7412A



7420, 7440



D.C. CHARACTERISTICS

Information on the absolute maximum ratings and the other D.C. characteristics of these devices (which are common to other integrated circuits in this series) is stated in the general information section.

PARAMETER	LIMIT				CONDITIONS	
	Min.	Typ.	Max.	Unit	V_{CC}	
I_{CCL}						
ITT7400, 01, 01A, 03, 03A, 26		12	22	mA	Max.	V_{IN} on all inputs=5.0V
7407, 17		21	30	mA		
7410, 12, 12A		9	16.5	mA		
7406, 16		24	38	mA		
7420		6	11	mA		
7430		3	5.5	mA		
7404, 05, 05A		18	33	mA		
7440		17	27	mA		
7402		14	27	mA		
7428		35	56	mA		
7437, 38		34	54	mA		

PARAMETER	LIMIT				CONDITIONS	
	Min.	Typ.	Max.	Unit	V_{CC}	
I_{CCH}						
7400, 01, 01A, 03, 03A		4	8	mA	Max.	V_{IN} on all inputs=0 V
7406, 16		30	42	mA		
7407, 17		29	41	mA		
7410, 12, 12A		3	6	mA		
20		2	4	mA		
30		1	2	mA		
26, 40		4	8	mA		
04, 05, 05A		6	12	mA		
02		8	16	mA		
28		12	24	mA		
37		9	15.5	mA		
38		5	8.5	mA		

Exceptions to common characteristics:

PARAMETER		LIMIT				CONDITIONS	
		Min.	Typ.	Max.	Unit	V_{CC}	
$-I_{SC}$	7428	40		125	mA	Max.	*V_{OUT}=0V
$-I_{SC}$	7440	18		70	mA	Max.	*V_{OUT}=V_{IN}=0V
$-I_{SC}$	5440,54/7437	20		70	mA	Max.	*V_{OUT}=V_{IN}=0V
$V_{OH(M)}$	7426	15			V	Min.	V_{IL}=0.8V, I_{OH}=1mA
I_{CEX}	7426			50	μA	Min.	V_{IL}=0.8V, V_{OUT}=12V
V_{OL}	7406/16			0.7V.		Min.	V_I=2.0V, I_{OL}=40mA
V_{OL}	5406/16			0.7V		Min.	V_I=2.0V, I_{OL}=30mA
V_{OL}	7407/17			0.7V		Min.	V_I=0.8V. I_{OL}=40mA
V_{OL}	5407/17			0.7V		Min.	V_I=0.8V, I_{OL}=30mA
V_{OL}	54/7407/17			0.4V		Min.	V_I=0.8V, I_{OL}=16mA
I_{OH}	54/7406			250μA		Min.	V_I=0.8V, V_{OH}=30V
I_{OH}	54/7416			250μA		Min.	V_I=0.8V, V_{OH}=15V
I_{OH}	54/7407			250μA		Min.	V_I=2.0V, V_{OH}=30V
I_{OH}	54/7417			250μA		Min.	V_I=2.0V, V_{OH}=15V

*Only one output to be short-circuited at any time.

SWITCHING CHARACTERISTICS

Switching test circuits as shown in the general information section.

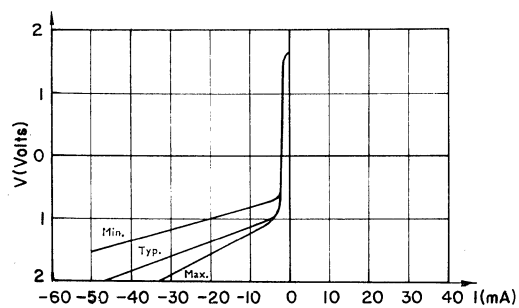
Note
Other inputs of the gate under test taken to 2.4 V, except 7402, other input of the gate under test taken to ground. For 7428 the pulse input is taken to a 7400 series gate with the other inputs at 2.4 V and whose output is connected to one input of the gate under test (other inputs of gate under test taken to ground).

Characteristics of pulse from generator at a device input:

t_r = 10 ns, t_f = 4 ns, t_p = 500 ns, P.R.F. = 1 MHz, Z_o = 50 Ω, Amplitude = 3.5 V, except for 7428 where $t_r = t_f \langle$ 15 ns.

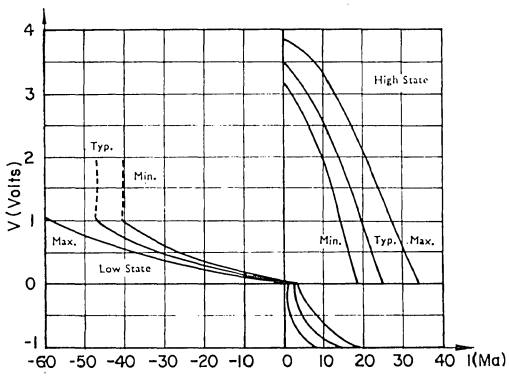
PARAMETER	LIMIT				CONDITIONS
	Min.	Typ.	Max.	Unit	
t_{pd+}					
7400,10,20,30		10	22	ns	See test circuits in introduction, C_L=15 pF, R_L=400 Ω
7401,01A,03,03A,12,12A		35	45	ns	R_L=4 K Ω, C_L=15 pF
7426		16	24	ns	R_L=1 K Ω, C_L=15 pF
7404		10	22	ns	R_L=400 Ω, C_L=15 pF
7405,05A		40	55	ns	R_L=400 Ω, C_L=15 pF
7406,16		10	15	ns	R_L=110 Ω, C_L=15 pF
7407,17		6	10	ns	R_L=110 Ω, C_L=15 pF
7440		10	22	ns	R_L=133 Ω, C_L= 15 pF
7402		10	22	ns	R_L=400 Ω, C_L=15 pF
7428		10	15	ns	R_L=133 Ω, C_L=15 pF
7437		13	22	ns	R_L=133 Ω, C_L=45 pF
7438		14	22	ns	R_L=133 Ω, C_L=45 pF
t_{pd-}					See test circuit:
7400,10,20,30		8	15	ns	R_L=400 Ω, C_L=15 pF
7426		11	17	ns	R_L=1 K Ω, C_L=15 pF
7406,16		15	23	ns	R_L=110 Ω, C_L=15 pF
7407,17		20	30	ns	R_L=110 Ω, C_L=15 pF
7401,01A,03,03A,12,12A		8	15	ns	R_L=400 Ω, C_L=15 pF
7404,05,05A		8	15	ns	R_L=400 Ω, C_L=15 pF
7440		8	15	ns	R_L=133 Ω, C_L=15 pF
7402		8	15	ns	R_L=400 Ω, C_L=15 pF
7428		8	15	ns	R_L=133 Ω, C_L=15 pF
7437		8	15	ns	R_L=133 Ω, C_L=45 pF
7438		11	18	ns	R_L=133 Ω, C_L=45 pF

TYPICAL CHARACTERISTICS OF STANDARD NAND GATES



Typical and 95% Limit Input Characteristics (at 5 V and 0°C to 75°C)

Typical and 95% Limit Output Characteristics (at 5 V and 0°C to 75°C)



APPLICATION NOTES

Wired-Or Function

The purpose of the 5.5 V open collector devices is primarily to perform the 'wired-OR' function which can not be implemented by the standard active pull up output circuit. The open collector devices require an external resistor between output and V_{CC}. The choice of resistor value is a compromise between fan out requirements, the number of commoned outputs, power dissipation and speed. Limiting values of R_X are given by the following inequalities.

$$R_X > \frac{V_{CC}(max.) - V_{OL}(max.)}{(10-N)\, I_F}$$

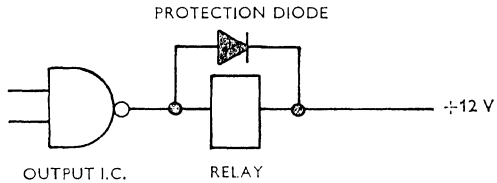
$$R_X < \frac{V_{CC}(min.) - V_{OH}(min.)}{M.I_{CEX} + N.I_R}$$

Where M=Number of outputs commoned together in the 'Wired-OR' function; N=Fan out required.

High Voltage Output

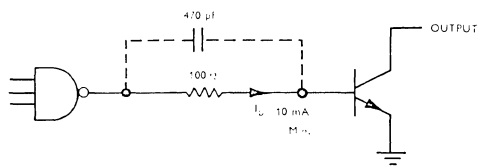
A typical use of the high voltage open collector device:

Miniature relay drives – A protection diode is required to prevent turn off transients damaging the output transistor (as shown).



Output Interfacing

When interfacing between TTL logic and lamps, relays etc. a discrete driving transistor is normally used. If there are several such interface transistors being driven from one multiple gate TTL device a problem is encountered in determining the value of base resistor to be used, to ensure maximum base drive without risk of over dissipating the ICC, when all outputs are high. The circuit shown below is suitable for use with the ITT devices and gives minimum base current of 10 mA.



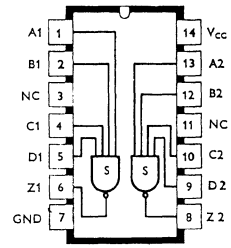
Standard 74 Series Gate

The inclusion of the 470 pF capacitor will give a considerable improvement in speed of this circuit. If the transistor used is a 2N2369A propagation delay times from the gate inputs to output of 10ns can be achieved.

ITT7413
DUAL 4-INPUT POSITIVE NAND SCHMITT TRIGGER

- **Temperature compensated thresholds**
- **Hysterisis 0.8 V**
- **Fan out=10, low state**
- **Fan out-20, high state**
- **Operates from signal with slow rise and fall times**
- **Pulse shaper**

Pin configuration (top view)



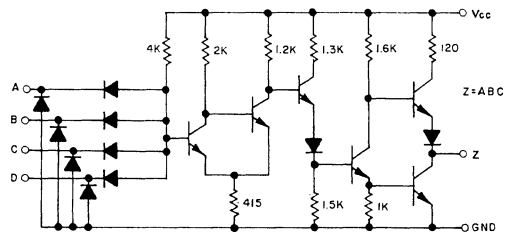
ITT7413

TYPICAL CHARACTERISTICS

Propagation delay . . . . . 17 ns
Power dissipation (50% duty cycle) . . . . 85 mW
Input loading factor . . . . . 1 unit load
Fan out . . . . . 1 to 10 unit loads, low state
1 to 20 unit loads, high state
Positive threshold . . . . . 1.7 V
Negative threshold . . . . . 0.9 V

Circuit diagram of one gate

Resistance values in ohms



D.C. CHARACTERISTICS

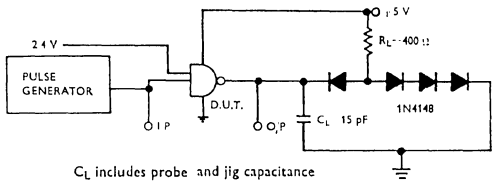
PARAMETER	LIMIT				CONDITIONS	
	Min.	Typ. at 25°C	Max.	Units	V_{CC}	
V_{T+} positive edge threshold voltage	1.5	1.7		V	5.0V	V_{OL} ⟨ 0.4V
V_{T-} negative edge threshold		0.9	1.1	V	5.0V	V_{OH} ⟩ 2.4V
V_H hysteresis	0.4	0.8		V	5.0V	
$-I_{IN+}$ input current at V_{T+}		0.65		mA	5.0V	$V_{IN}=V_{T+}$
$-I_{IN-}$ input current at V_{T-}		0.85		mA	5.0V	$V_{IN}=V_{T-}$
I_{CCH}		20	36	mA	Max.	V_{IN} on all inputs 5.0V
I_{CCL}		14	28	mA	Max.	V_{IN} on all inputs 0V

Information on the absolute maximum ratings and the other D.C. characteristics of this device (which are common to other integrated circuits in this series) is stated in the general information section.

SWITCHING CHARACTERISTICS V_{CC}=5.0 V, T_{AMB}=25°C

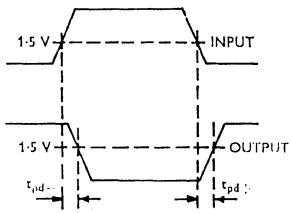
PARAMETER	LIMIT				CONDITIONS
	Min.	Typ.	Max.	Unit	
t_{pd+}		18	35	ns	See test circuit
t_{pd-}		15	30	ns	See test circuit

Switching test circuit

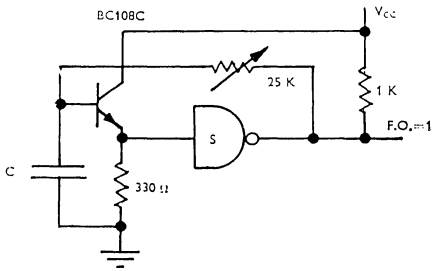


Pulse Characteristics
t_r = 10 ns
t_p = 4 ns
f_o = 500 ns
P.R.F. = 1 MHz
Z_o = 50 Ω
Amplitude - 3.5 V

Waveforms



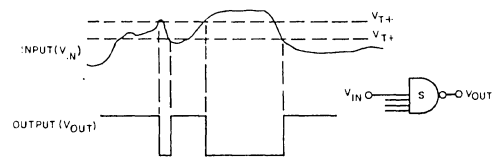
An alternative circuit is also illustrated which avoids the use of such large and expensive capacitors to achieve low frequencies. It also has the advantage of easy adjustment. Typical values of C for 1 Hz with transistor current gain of 200 is 40 μF.



APPLICATION NOTES

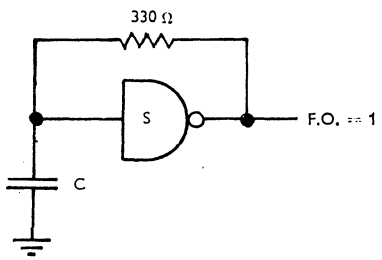
Pulse Shaper

Any input signal with slowly changing voltages will be unambiguously shaped by the ITT7413 due to its schmitt input.



Multivibrator

The circuit shown will have operated as a self starting multivibrator having frequency range of 1 Hz to 10 MHz. Typical values of C are 2,000 μF for 1 Hz and 200 pF for 10 MHz. Mark space ratio 1:3.

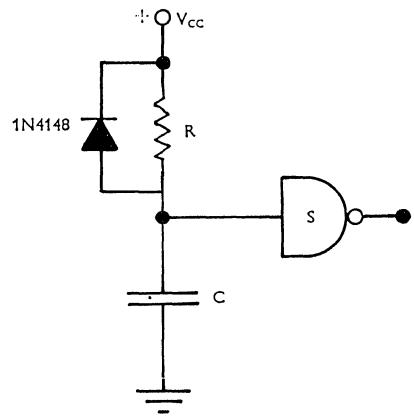


Supply Switch on Reset Driver

It is often required that I.C. logic systems should be reset to a known state on switch on of supply voltage. This function is automatically provided by the circuit shown. The output pulse is given approximately by the relation

$$t = 0.4\,C\left(\frac{4R \times 10^3}{R + 4 \times 10^3}\right)$$

This time constant should be designed to be longer than the start up time of the V_{CC} power supply. The diode is provided to ensure fast discharge of C.

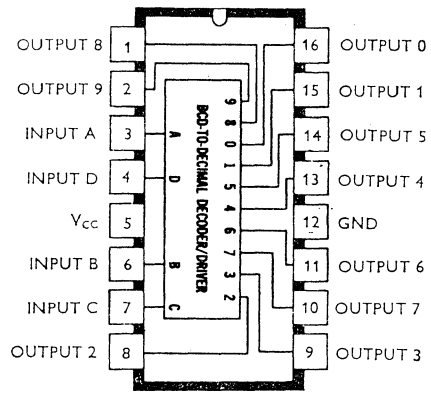


- **For driving gas-filled cold cathode indicator tubes**

TYPICAL CHARACTERISTICS

Power dissipation	140 mW
Input loading factor	1 unit load
Output load	⩽7 mA
Output voltage	85 V

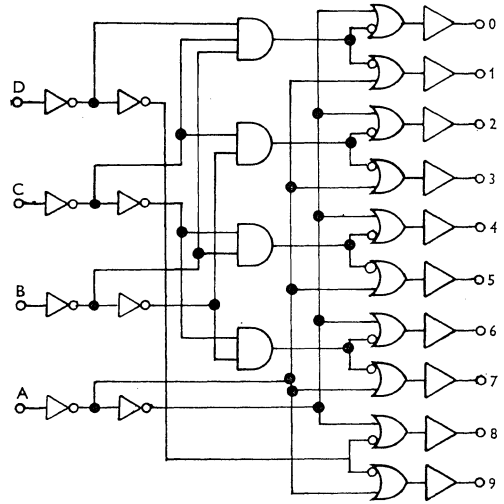
Pin configuration (top view)



Truth Table

D	C	B	A	O/P	OVER RANGE				
0	0	0	0	0	1	0	1	0	2&8
0	0	0	1	1	1	0	1	1	3&9
0	0	1	0	2	1	1	0	0	4&8
0	0	1	1	3	1	1	0	1	5&9
0	1	0	0	4	1	1	1	0	6&9
0	1	0	1	5	1	1	1	1	7&9
0	1	1	0	6					
0	1	1	1	7					
1	0	0	0	8					
1	0	0	1	9					

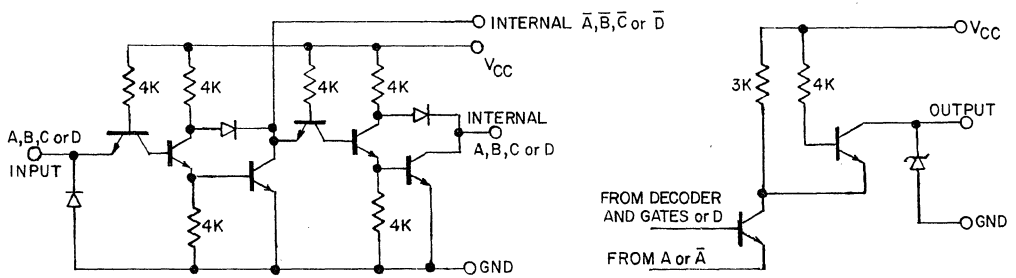
Logic diagram



DESCRIPTION

The input circuitry of the ITT7441A consists of eight inverters which are used to produce true and complement logic levels of the input signals which are suitable for internal use. The decoding from BCD is achieved by four AND gates and ten NOR gates. The output drivers are designed to drive gas-filled indicator tubes. The circuitry of the output is such that when it is in the off state it can always withstand the unused cathode voltage and operate with minimal current (thus keeping background glow to a minimum). In addition due to special control of the breakdown of the output transistors, there is no tendency for the non conducting output transistors to oscillate.

Circuit diagram of typical input and output circuits
Resistance values in ohms

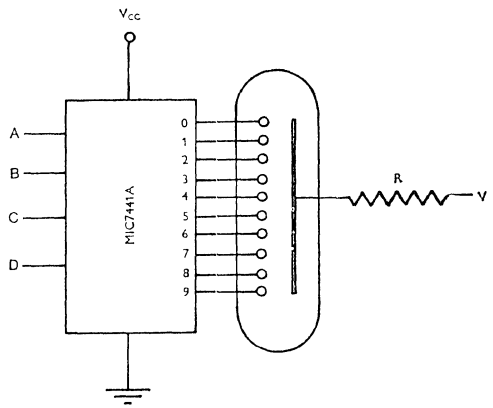


PARA-METER	LIMIT				CONDI-TIONS
	Min.	Typ.at 25°C	Max.	Units	V_{CC}
$V_{OH(M)}$	70	85		V	Max. I_{OH}=2 mA
I_{CEX}			50	μA	Max. V_{CEX}=55V
V_{OL}			2.4	V	Min. I_{OL}=7 mA
I_{CC}		21	42	mA	Max.

Information on the absolute maximum ratings and the other DC characteristics of this device (which are common to other integrated circuits in this series) is stated in the general information section.

NUMERICAL INDICATOR TUBE DRIVING

The circuit illustrates typical connection of ITT-7441A to a numerical indicator tube.



R and V are selected from tube manufacturers data. The ground connection must be of low impedance.

The ITT7441A ensures that the prebias voltage does not fall below 70 volts. A numerical indicator tube must be chosen such that the prebias current does not exceed 2 mA at a prebias voltage of 70 volts.

APPLICATION NOTE

Decoding

It is not generally realized that decoders designed as BCD to decimal decoders can be used with non-standard input and output connections. This allows the user greater flexibility on board layout for BCD, and ability to decode other codes.
The charts below show some possible input and output connections for the following codes:
BCD, Excess three Gray, Gray, Biquinary and 2421.
Also shown is the truth table for each code. The box represents the decoder with standard connections marked. To the left of the box are shown the variations of input connections and to the right the variations of output connections.

BCD

Input a	Input b			Output a	Output b	D	C	B	A	Dec
			0	0	0	0	0	0	0	0
			1	1	1	0	0	0	1	1
A	A	A	2	2	4	0	0	1	0	2
			3	3	5	0	0	1	1	3
B	C	B	4	4	2	0	1	0	0	4
			5	5	3	0	1	0	1	5
C	B	C	6	6	6	0	1	1	0	6
			7	7	7	0	1	1	1	7
D	D	D	8	8	8	1	0	0	0	8
			9	9	0	1	0	0	1	9

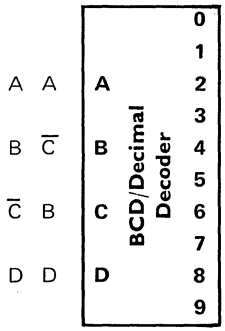
BCD/Decimal Decoder

Excess Three Gray

Input a	Input b			Output a	Output b	D	C	B	A	Dec
			0	1	1	0	0	1	0	0
			1	8	8	0	1	1	0	1
D	D	A	2	2	4	0	1	1	1	2
			3	7	5	0	1	0	1	3
A	$\overline{B}$	B	4	4	2	0	1	0	0	4
			5	5	7	1	1	0	0	5
$\overline{B}$	A	C	6	3	3	1	1	0	1	6
			7	6	6	1	1	1	1	7
$\overline{C}$	$\overline{C}$	D	8	0	0	1	1	1	0	8
			9	9	9	1	0	1	0	9

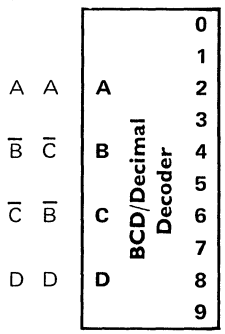
BCD/Decimal Decoder

Gray



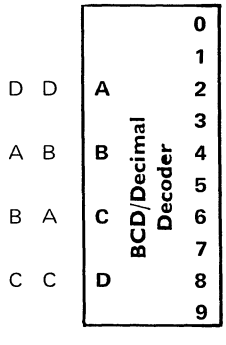
Output a	Output b	D	C	B	A	Dec
7	7	0	0	0	0	0
6	6	0	0	0	1	1
4	0	0	0	1	1	2
5	1	0	0	1	0	3
0	4	0	1	1	0	4
1	5	0	1	1	1	5
3	3	0	1	0	1	6
2	2	0	1	0	0	7
8	8	1	1	0	0	8
9	9	1	1	0	1	9

2421



Output a	Output b	D	C	B	A	Dec
6	6	0	0	0	0	0
7	7	0	0	0	1	1
4	2	0	0	1	0	2
5	3	0	0	1	1	3
2	4	0	1	0	0	4
3	5	0	1	0	1	5
0	0	0	1	1	0	6
1	1	0	1	1	1	7
8	8	1	1	1	0	8
9	9	1	1	1	1	9

Biquinary



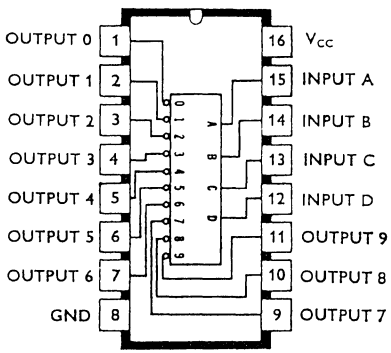
Output a	Output b	D	C	B	A	Dec
0	0	0	0	0	0	0
5	5	0	0	0	1	1
1	2	0	0	1	0	2
6	7	0	0	1	1	3
2	1	0	1	0	0	4
7	6	1	0	0	0	5
3	3	1	0	0	1	6
8	8	1	0	1	0	7
4	4	1	0	1	1	8
9	9	1	1	0	0	9

- **2421 Decoder**
- **Biquinary Decoder**
- **3 line to 8 line decoder with strobe**
- **Recognition of invalid input codes**

TYPICAL CHARACTERISTICS

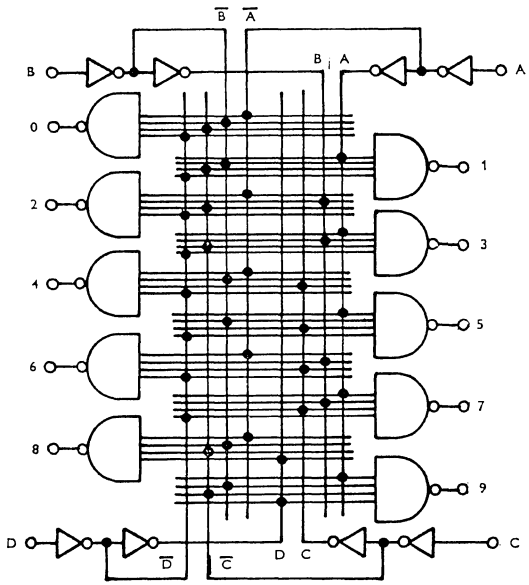
Propagation delay	25 ns
Power dissipation	140 mW
Input loading factor	1 unit load
Fan out	1 to 10 unit loads

Pin configuration (top view)



Logic Diagram

Connections are shown for the ITT7442. The matrix connections are different for the ITT7443 and the ITT7444 and they can be determined from the truth table.

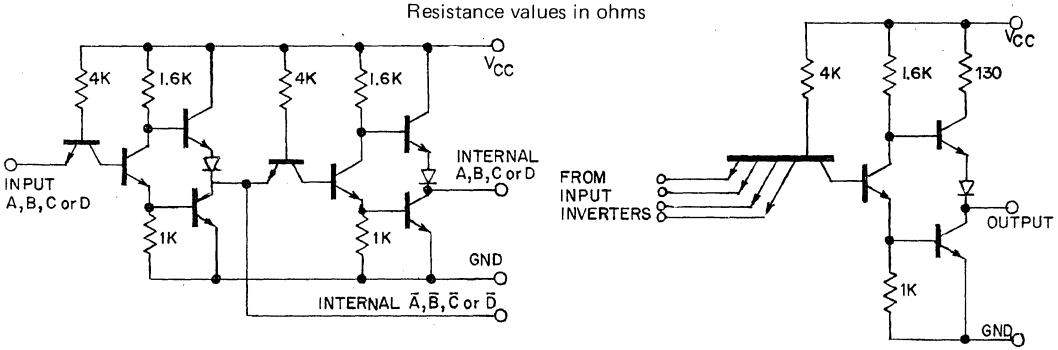


Truth Table

	BCD Input				Excess 3 Input				Excess 3 Gray Input				Decimal Output									
Dec.	D	C	B	A	D	C	B	A	D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	0	0	0	0	0	0	1	1	0	0	1	0	0	1	1	1	1	1	1	1	1	1
1	0	0	0	1	0	1	0	0	0	1	1	0	1	0	1	1	1	1	1	1	1	1
2	0	0	1	0	0	1	0	1	0	1	1	1	1	1	0	1	1	1	1	1	1	1
3	0	0	1	1	0	1	1	0	0	1	0	1	1	1	1	0	1	1	1	1	1	1
4	0	1	0	0	0	1	1	1	0	1	0	0	1	1	1	1	0	1	1	1	1	1
5	0	1	0	1	1	0	0	0	1	1	0	0	1	1	1	1	1	0	1	1	1	1
6	0	1	1	0	1	0	0	1	1	1	0	1	1	1	1	1	1	1	0	1	1	1
7	0	1	1	1	1	0	1	0	1	1	1	1	1	1	1	1	1	1	1	0	1	1
8	1	0	0	0	1	0	1	1	1	1	1	0	1	1	1	1	1	1	1	1	0	1
9	1	0	0	1	1	1	0	0	1	0	1	0	1	1	1	1	1	1	1	1	1	0
Over Range Conditions																						
10	1	0	1	0	1	1	0	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1
11	1	0	1	1	1	1	1	0	1	0	0	1	1	1	1	1	1	1	1	1	1	1
12	1	1	0	0	1	1	1	1	1	0	0	0	1	1	1	1	1	1	1	1	1	1
13	1	1	0	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1
14	1	1	1	0	0	0	0	1	0	0	0	1	1	1	1	1	1	1	1	1	1	1
15	1	1	1	1	0	0	1	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1

Circuit diagram of typical input and output circuits

Resistance values in ohms

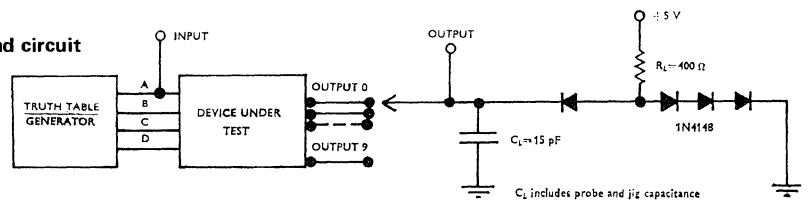


SWITCHING CHARACTERISTICS V_{CC}=5.0 V, T_{AMB}=25°C

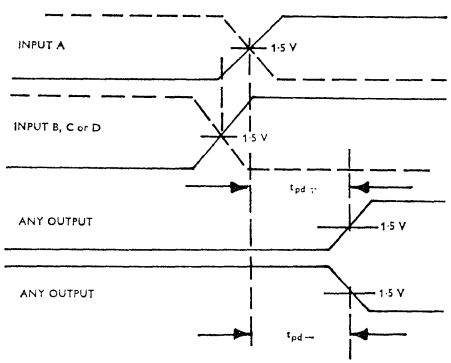
PARAMETER	LIMIT				CONDITIONS
	Min.	Typ.at 25°C	Max.	Units	
t_{pd} + through two logic levels	10	17	25	ns	Use switching load circuit
t_{pd} + through three logic levels		26	35	ns	
t_{pd} − through two logic levels	10	22	30	ns	Use switching load circuit
t_{pd} − through three logic levels		26	35	ns	

Information on the absolute maximum ratings and the other D.C. characteristics of these devices (which are common to other integrated circuits in this series) is stated in the general information section.

Switching load circuit



Waveforms



Truth Table

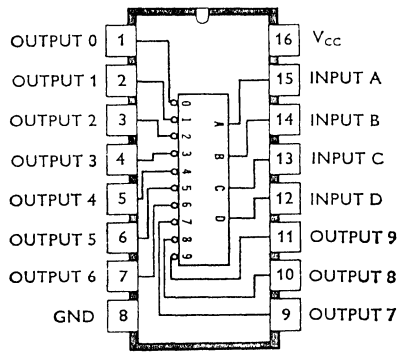
Generator Characteristics
t_r = 10 ns
t_f = 4 ns
R.F. = 1 MHz
Amplitude = 3.5 V
Z_O = 50 Ω
Transitions on B, C, & D must occur before transition on A.

- **80 mA Output Sink-Current**
- **ITT7445 30 Volt Output**
- **ITT74145 15 Volt Output**
- **Recognition of Invalid Codes**
- **Decoder Excess Three Gray, Gray, Biquinary and**
- **Other Codes**

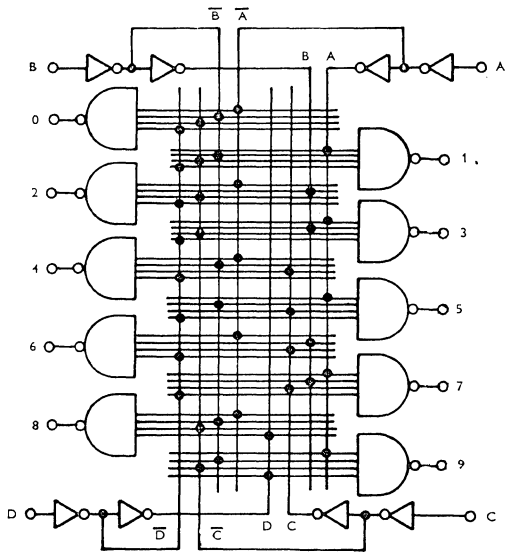
TYPICAL CHARACTERISTICS

Propagation delay . . . . . 35 ns
Power dissipation . . . . . 215 mW
Input loading factor . . . . . 1 unit load
Output voltage rating
ITT7445 . . . . . 30 V
ITT74145 . . . . . 15 V

Pin Configuration



Logic diagram



DESCRIPTION

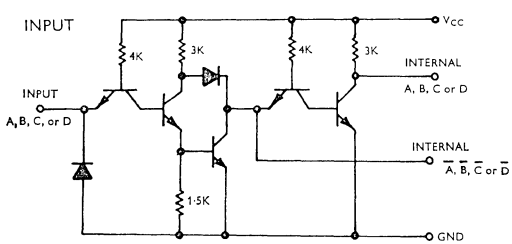
These decoders consist of eight inverters and ten output gates. Each pair of inverters are connected in series to provide true and complement signals of the four inputs. The ten output gates are of special design to enable them to have the high voltage rating and high current capability. These output gates each have four inputs which are used to provide full decoding so that invalid input states give no output.

Truth Table

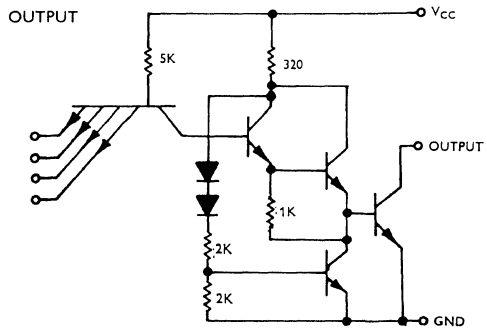
INPUTS				OUTPUTS									
D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	0	0	0	0	1	1	1	1	1	1	1	1	1
0	0	0	1	1	0	1	1	1	1	1	1	1	1
0	0	1	0	1	1	0	1	1	1	1	1	1	1
0	0	1	1	1	1	1	0	1	1	1	1	1	1
0	1	0	0	1	1	1	1	0	1	1	1	1	1
0	1	0	1	1	1	1	1	1	0	1	1	1	1
0	1	1	0	1	1	1	1	1	1	0	1	1	1
0	1	1	1	1	1	1	1	1	1	1	0	1	1
1	0	0	0	1	1	1	1	1	1	1	1	0	1
1	0	0	1	1	1	1	1	1	1	1	1	1	0
OVER RANGE CONDITIONS													
1	0	1	0	1	1	1	1	1	1	1	1	1	1
1	0	1	1	1	1	1	1	1	1	1	1	1	1
1	1	0	0	1	1	1	1	1	1	1	1	1	1
1	1	0	1	1	1	1	1	1	1	1	1	1	1
1	1	1	0	1	1	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1	1	1	1	1

Circuit diagram of typical input and output circuits

Resistance values in ohms



PARAMETER	LIMIT				CONDITIONS
	Min.	Typ.at 25°C	Max.	Units	V_{CC}
I_{CCH} supply current for highest dissipation state					
74 series	43	70		mA	Max. Any valid
54 series	43	62		mA	Max. input code
I_{CCL} supply current for lowest dissipation state					
74 series	31	53		mA	Max. Any invalid
54 series	31	45		mA	Max. input code

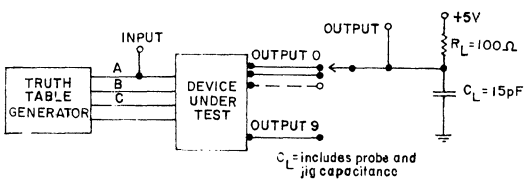


Information on the absolute maximum ratings and the other D.C. characteristics of this device (which are common to other integrated circuits in this series) is stated in the general information section.

SWITCHING CHARACTERISTICS V_{CC}=5.0 V, T_{AMB}=25°C

PARAMETER	LIMIT				CONDITIONS
	Min.	Typ.at 25°C	Max.	Units	
t_{pd}+ propagation delay to logical '1'			50	ns	Use switching load circuit
t_{pd}- propagation delay to logical '0'			50	ns	Use switching load circuit

Switching load circuit

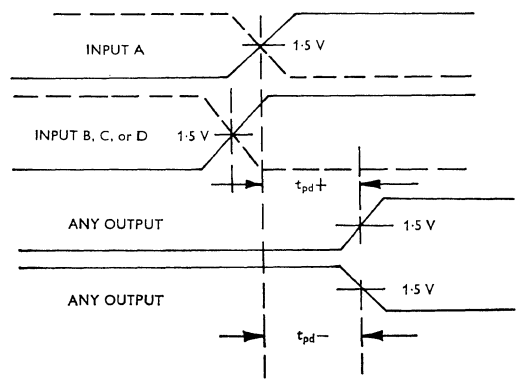


Truth Table
Generator Characteristics

t_r = 10 ns
t_f = 4 ns
R.F. = 1 MHz
Amplitude - 3.5 V

Z_O = 50 Ω
Transition on B, C or D must occur before transition on A.

Waveforms

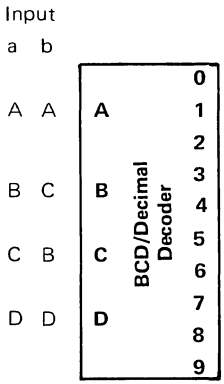


APPLICATION NOTE

Decoding

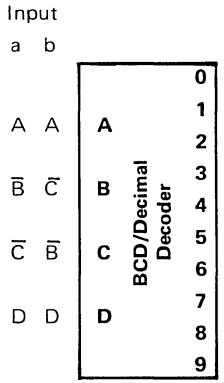
It is not generally realised that decoders designed as BCD to decimal decoders can be used with non standard input and output connections. This allows the user greater flexibility on board layout for BCD, and ability to decode other codes.
The following charts show some possible input and output connections for the following codes: BCD, Excess Three Gray, Gray, Biquinary and 2421. Also shown is the truth table for each code. The box represents the decoder with standard connections marked. To the left of the box are shown the variations of input connections and to the right the variations of output connections.

BCD



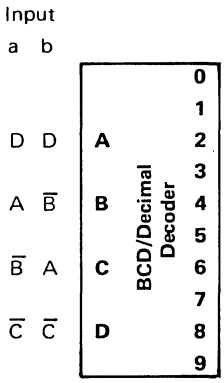
Output	a	b	D	C	B	A	Dec
0	0	0	0	0	0	0	0
1	1	1	0	0	0	1	1
2	2	4	0	0	1	0	2
3	3	5	0	0	1	1	3
4	4	2	0	1	0	0	4
5	5	3	0	1	0	1	5
6	6	6	0	1	1	0	6
7	7	7	0	1	1	1	7
8	8	8	1	0	0	0	8
9	9	9	1	0	0	1	9

2421



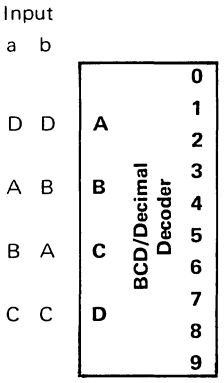
Output	a	b	D	C	B	A	Dec
0	6	6	0	0	0	0	0
1	7	7	0	0	0	1	1
2	4	2	0	0	1	0	2
3	5	3	0	0	1	1	3
4	2	4	0	1	0	0	4
5	3	5	0	1	0	1	5
6	0	0	0	1	1	0	6
7	1	1	0	1	1	1	7
8	8	8	1	1	1	0	8
9	9	9	1	1	1	1	9

Excess Three Gray



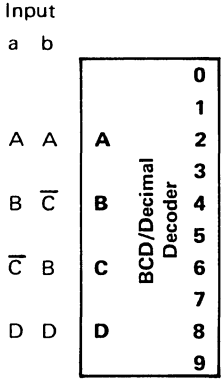
Output	a	b	D	C	B	A	Dec
0	1	1	0	0	1	0	0
1	8	8	0	1	1	0	1
2	2	4	0	1	1	1	2
3	7	5	0	1	0	1	3
4	4	2	0	1	0	0	4
5	5	7	1	1	0	0	5
6	3	3	1	1	0	1	6
7	6	6	1	1	1	1	7
8	0	0	1	1	1	0	8
9	9	9	1	0	1	0	9

Biquinary



Output	a	b	D	C	B	A	Dec
0	0	0	0	0	0		0
1	5	5	0	0	0	1	1
2	1	2	0	0	1	0	2
3	6	7	0	0	1	1	3
4	2	1	0	1	0	0	4
5	7	6	1	0	0	0	5
6	3	3	1	0	0	1	6
7	8	8	1	0	1	0	7
8	4	4	1	0	1	1	8
9	9	9	1	1	0	0	9

Gray

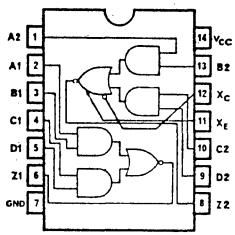


Output	a	b	D	C	B	A	Dec
0	7	7	0	0	0	0	0
1	6	6	0	0	0	1	1
2	4	0	0	0	1	1	2
3	5	1	0	0	1	0	3
4	0	4	0	1	1	0	4
5	1	5	0	1	1	1	5
6	3	3	0	1	0	1	6
7	2	2	0	1	0	0	7
8	8	8	1	1	0	0	8
9	9	9	1	1	0	1	9

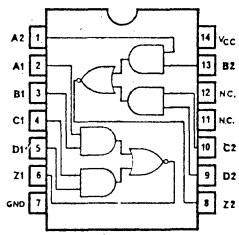
TYPICAL CHARACTERISTICS

Propagation delay	9 ns
Power dissipation	29 mW (7450, 7451)
(50% duty cycle)	23 mW (7453, 7454)
Input loading factor	1 unit load
Fan-out	1 to 10 unit loads

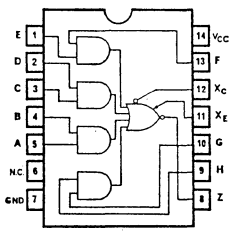
Pin configuration (top views)



ITT7450

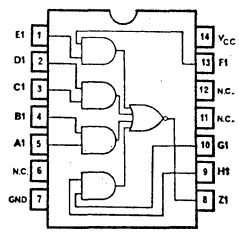


ITT7451



ITT7453

Make no external connection to pins 11 and 12

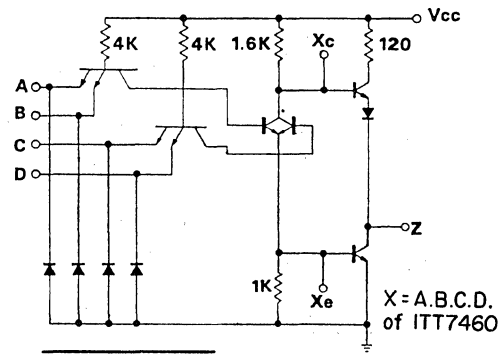


ITT7454

If expander is not used leave pins 11 and 12 open

Circuit diagram of one gate (ITT7450 and ITT7451)

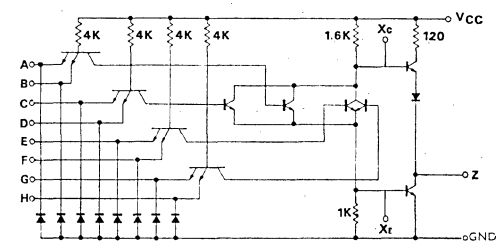
Resistance values in ohms



$Z = \overline{(A.B) + (C.D) + (X)}$

The ITT7451 and ITT7454 do not have the expanding inputs X_E and X_C

Circuit diagram of ITT7453 and ITT7454



$Z = (A.B) + (C.D) + (E.F) + (G.H) + (X)$
where X = A.B.C.D. of ITT7460

PARAMETER	LIMIT				CONDITIONS	
	Min.	Type at 25°C	Max.	Units	V_{CC}	
I_{CCH}						
ITT7450, ITT7451		7.4	14	mA	Max.	V_{IN} on all inputs
ITT7453, ITT7454		5.1	9.5	mA	Max.	5.0 V
I_{CCL}		4.0	8.0	mA	Max.	V_{IN} on all inputs 0V

Information on the absolute maximum ratings and the other D.C. characteristics of these devices (which are common to other integrated circuits in this series) is stated in the general information section.

D.C. CHARACTERISTICS OF ITT7450/3 EXPANDER INPUTS AT 0°C

PARAMETER	LIMIT				CONDITIONS	
	Min.	Type	Max.	Unit	V_{CC}	
I_X expander current			3.1	mA	Min.	V_{CE}=0.4V, I_{OL}=16mA (Note 1)
V_{BE} base emitter voltage of output transistor			1.0	V	Min.	I_{OL}=16mA, R_{CE}=0, I_E=260μA (Note 1)
V_{OH} output high voltage	2.4	3.3		V	Min.	I_{OH}=−400μA, I_E−270μA, I_C−270μA (Note 1)
V_{OL} output low voltage		0.22	0.4	V	Min.	I_{OL}=10mA, I_E=430μA, R_{CE}=130 (Note 1)

D.C. CHARACTERISTICS OF ITT5450/3 EXPANDER INPUTS AT −55°C

PARAMETER	LIMIT				CONDITIONS	
	Min.	Type	Max.	Unit	V_{CC}	
I_X expander current			2.9	mA	Min.	V_{CE}=0.4V, I_{OL}=16mA (Note 1)
V_{BE} base emitter voltage of output transistor			1.0	V	Min.	I_{OL}=16mA, R_{CE}=0, I_E=410μA (Note 1)
V_{OH} output high voltage	2.4	3.3		V	Min.	I_{OH}=−400μA, I_E=150μA, I_C=−150μA (Note 1)
V_{OL} output low voltage		0.22	0.4	V	Min.	I_{OL}=16mA, I_E=300μA, R_{CE}=138 (Note 1)

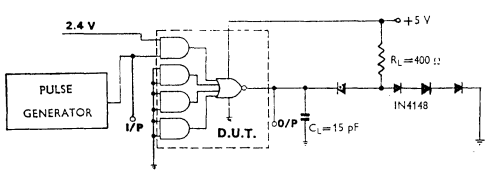
Note 1

V_{CE}, I_E, I_C and R_{CE} refer to voltage, current and resistance on X_E and X_C terminals.

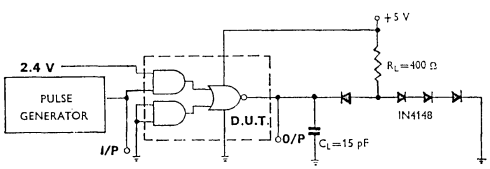
SWITCHING CHARACTERISTICS V_{CC}=5.0 V, T_{AMB}=25°C

PARAMETER	LIMIT				CONDITIONS
	Min.	Type	Max.	Units	
t_{pd}^+		10	22	ns	See test circuits
t_{pd}^-		8	15	ns	See test circuits

Switching test circuit for ITT7453/4

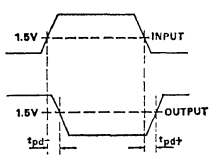


Switching test circuit for ITT7450/1



Pulse Characteristics
t_f = 10 ns
t_r = 4 ns
t_c = 500 ns
P.R.F. = 1 MHz
Z_o 50 Ω
Amplitude = 3.5 V

Waveforms

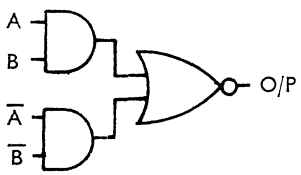


USE OF EXPANDER

The expander points are provided so that the input of the ITT7450 or the ITT7453 can be increased by a maximum of four 4-input NAND gates. Both X_C and X_E expander points must be used to connect to the X_C and X_E outputs of the ITT7460 expander.

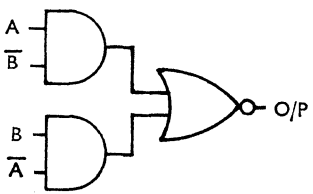
USE AS AN EXCLUSIVE OR GATE

The connections as an exclusive OR gate are shown below with inputs A and B.



A	B	O/P
0	0	0
1	0	1
0	1	1
1	1	0

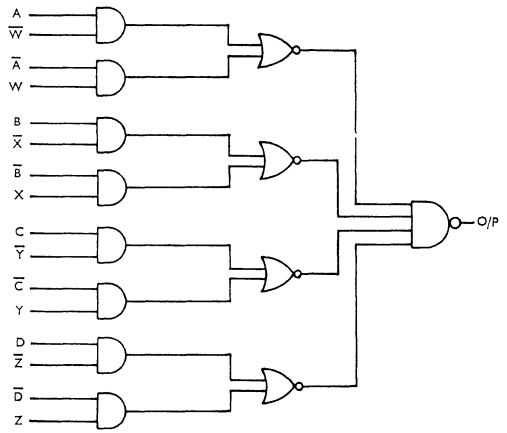
The inverse of exclusive OR function can also be obtained



A	B	O/P
0	0	1
1	0	0
0	1	0
1	1	1

ITT7450 and ITT7451 USED AS A COMPARATOR

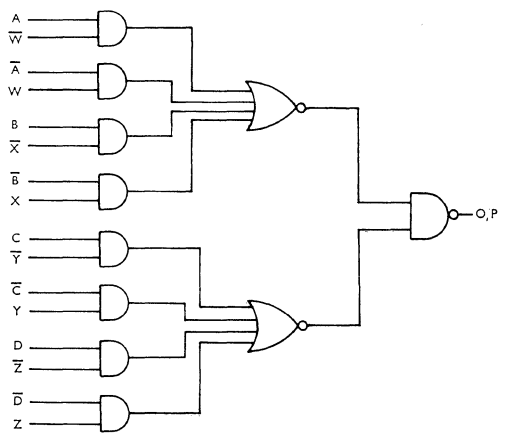
Two binary numbers ABCD and WXYZ.



When ABCD = WXYZ O/P = 0
when ABCD ⟩ or ⟨ WXYZ O/P = 1

ITT7453 and ITT7454 USED AS A COMPARATOR

Two binary numbers ABCD and WYXZ.



When ABCD - WXYZ O/P = 0
when ABCD ⟩ or ⟨ WXYZ O/P = 1

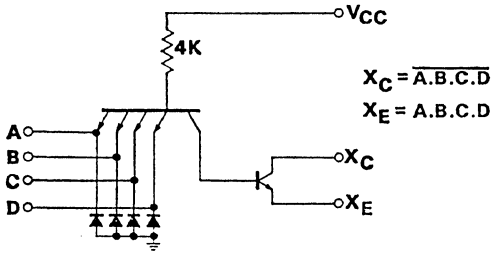
TYPICAL CHARACTERISTICS

Propagation delay . . . . . 13 ns
Power dissipation (50% duty cycle) . . . . . 8 mW
Input loading factor . . . . . 1 unit load

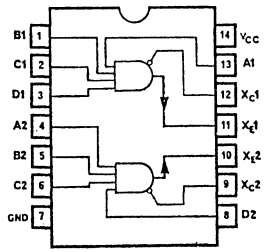
The ITT7460 expander is intended for use with the ITT7450 or 53 AND-OR-INVERT gates. Not more than four expander gates (two packages) should be connected to any AND-OR-INVERT gate. The X_C and X_E outputs of the expander should be connected respectively to X_C and X_F expander inputs of the AND-OR-INVERT gates. Inter-connecting leads should be kept as short as possible.

Circuit diagram of one expander

Resistance values in ohms



Pin configuration



PARAMETER	LIMIT				CONDITIONS	
	Min.	Type at 25°C	Max.	Units	V_{CC}	
V_{ON} on state voltage			0.4	V	Min.	V_E=1V, V_{IH}=2.0V, $R_{C/VCC}$=1.1K, T_{AMB}=Min.
I_{OFF} off-state output current—7460			270	µA	Min.	V_C=v.5V, V_{IL}=0.8V
5460			150	µA	Ma	$R_{E/GND}$=1.2K, T_{AMB}=Min.
I_{ON} on-state output current—7460	−300			µA	Max.	V_{IH}=2.0V, V_E=1.0V
5460	−430			µA		T_{AMB}=Min.
$-I_F$ input forward current		1.0	1.6	mA	Max.	V_F=0.4V
I_R input reverse current			40	µA	Max.	V_R=2.4V
			1.0	mA	Max.	V_R=5.5V

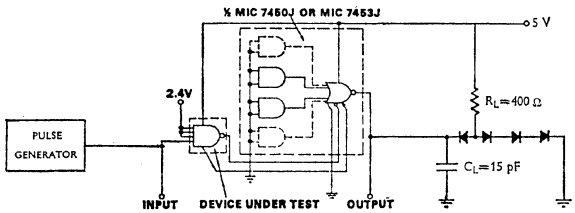
INPUT EXPANDER

PARAMETER	LIMIT				CONDITIONS	
	Min.	Type	Max.	Units	V_{CC}	
I_{CCH} supply current for highest dissipation (off state)		2	4	mA	Max.	V_{IN} on all inputs OV, V_E=0.85V
I_{CCL} supply current for lowest dissipation (on state)		1.2	2.5	mA	Max.	V_{IN} on all inputs 5.0V, V_E=-.85V

Information on the absolute maximum ratings and the other D.C. characteristics of this device (which are common to other integrated circuits in this series) is stated in the general information section.

PARAMETER	LIMIT			CONDITIONS
	Min.	Type	Max. Units	
t_{pd}+propagation delay to logical '1' (through ITT7450 or ITT7453)		15	30 ns	See test circuits
t_{pd} - propagation delay to logical '0' (through ITT7450 or ITT7453)		10	20 ns	See test circuit

Switching test circuit

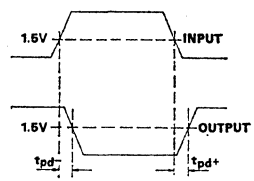


C_L includes probe and jig capacitance.

Pulse Characteristics

t_f = 10 ns
t_r = 4 ns
t_p = 500 ns
P.R.F. = 1 MHz
Z_o = 50 Ω
Amplitude = 3.5 V

Waveforms



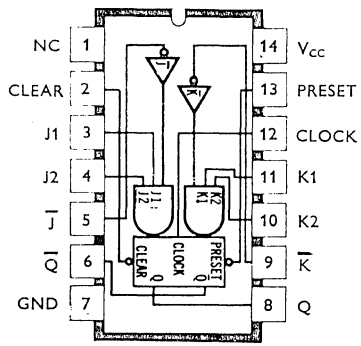
TYPICAL CHARACTERISTICS

Maximum clock frequency	35 MHz
Propagation delay	22 ns
Power dissipation	75 mW
Input loading factor	
Clock and any J or K input	1 unit load
Preset and clear	2 unit loads
Fan out	1 to 10 unit loads
Clock pulse transition time to logical '1'	5 ns to 150 ns
Clock pulse width t_{cp}	20 ns
Preset and clear pulse width t_p	25 ns

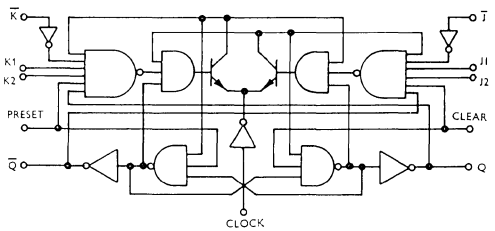
Truth Table

SYNCHRONOUS				ASYNCHRONOUS			
t_n		t_n+1					
J	K	Q	$\overline{Q}$	Preset	Clear	Q	$\overline{Q}$
0	0	No change		0	0	0	0
1	0	1	0	1	0	0	1
0	1	0	1	0	1	1	0
1	1	Complement		1	1	No control	

Pin configuration



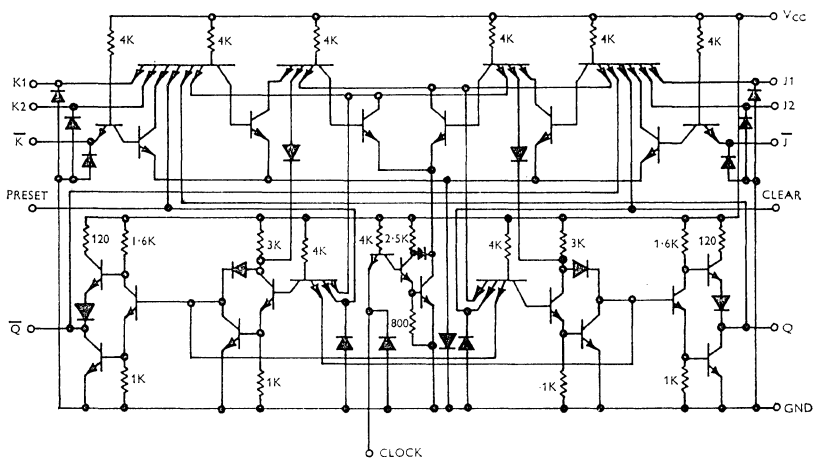
Logic diagram



DESCRIPTION

This device features twin J and K inputs, single $\overline{J}$ and $\overline{K}$ inputs, asynchronous preset and clear inputs and positive edge triggered clock input. At the threshold voltage, on the positive transition of the clock, input information is transferred to the outputs. Above or below the threshold the J and K inputs are disabled. The asynchronous inputs will operate the device only with clock low. The truth table shows the modes of operation.

Circuit diagram (Resistance values in ohms)

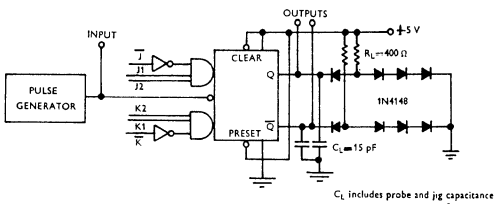


PARAMETER	LIMIT				CONDITIONS
	Min.	Typ. at 25°C	Max.	Units	V_{CC}
$-I_F$ input forward current.					
All J & K inputs and clock		1.0	1.6	mA	Max. V_F=0.4V
Preset and clear		2.0	3.2	mA	Max. Note 1
I_R input reverse current.					
All J & K inputs and clock			40	μA	Max. V_R=2.4V
Preset and clear			80	μA	Max. All other inputs at OV except $\overline{J}$ and $\overline{K}$ which are at 4.5 V
I_R All inputs			1	mA	Max. V_R=5.5V All other inputs at OV except $\overline{J}$ and $\overline{K}$ which are at 4.5V
$-I_{SC}$ short circuit output current					
74 series	18		57	mA	Max. V_{OUT}=OV
54 series (Note 2)	20		57	mA	Max. Preset and clear=OV
I_{CC} supply current		13	26	mA	Max.

Note 1
Test with all inputs at 4.5 V except $\overline{J}$ and $\overline{K}$ which are at OV. When testing J and K inputs all other inputs, to the appropriate input AND gate must be at logical '1'.

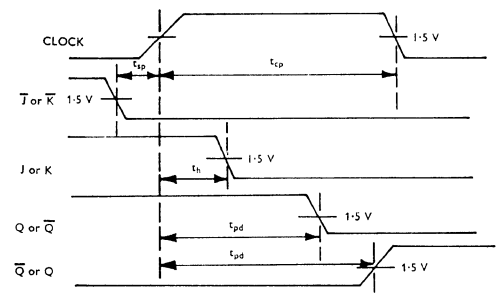
Note 2
Not more than one output to be shorted at any time.

Test circuit 1

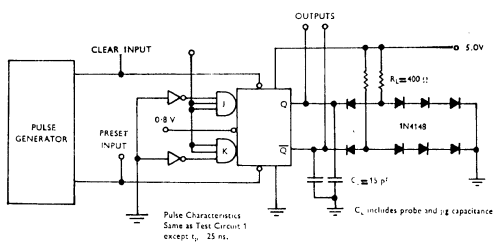


Pulse Characteristics
t_r = 10 ns
t_f = 4 ns
t_{cp} = 20 ns
R.F. = 1 MHz
Amplitude = 3.5 V

Waveforms



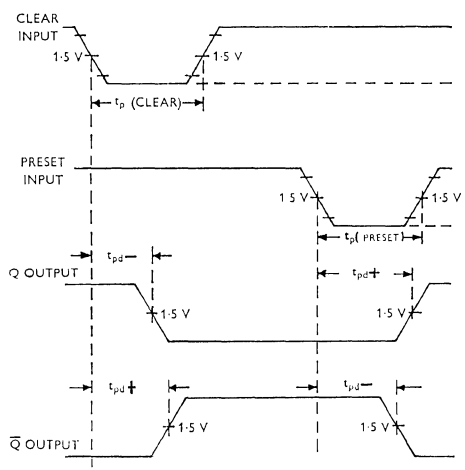
Test circuit 2



SWITCHING CHARACTERISTICS V_{CC}=5.0V, T_{AMB}=25°C

PARAMETER	LIMIT				CONDITIONS
	Min.	Typ.	Max.	Unit	
f_{max} maximum input clock frequency	20	35		MHz	Use test circuit 1. $\overline{J}$ and $\overline{K}$ at OV J1, K1, J2 and K2 at 2.4 V
t_{sp} minimum input set up time at $\overline{J}$ and $\overline{K}$		10	20	ns	Use test circuit 1. $\overline{J}$ or $\overline{K}$ at OV J1, J2, K1 and K2 at 2.4 V
t_h minimum input hold time at J1, J2, K1, K2		0	5	ns	Use test circuit 1. $\overline{J}$ and $\overline{K}$ at OV K1 and K2 or J1 and J2 at 2.4 V
t_{pd}+ propagation delay time to logical '1'					Clock at 0.8 V, $\overline{J}$ and $\overline{K}$ at OV
Clear or preset to output			50	ns	J and K at 2.4 V. Use test circuit 2.
Clock to output	10	27	50	ns	Use test circuit 1. $\overline{J}$ and $\overline{K}$ at OV, J and K as truth table
t_{pd}- propagation delay time to logical '0'					Clock at 0.8 V. $\overline{J}$ and $\overline{K}$ at OV.
Clear or preset to output			50	ns	J and K at 2.4 V. Use test circuit 2.
Clock to output	10	18	50	ns	Use test circuit 1. J and K at OV, J and K as truth table

Waveforms



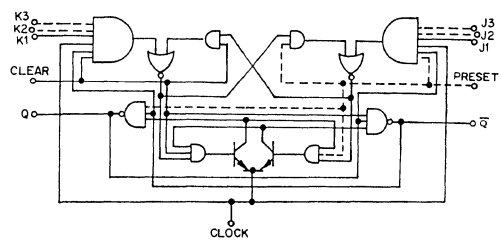
TYPICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

Maximum clock frequency	20 MHz
Propagation delay	20 ns
Power dissipation:	
Single type	50 mW
Dual type	100 mW
Input loading factor:	
J and K inputs	1 unit load
Direct and clock inputs	2 unit loads
Fan-out	1 to 10 unit loads
Clock pulse width t_{cp}	20 ns
Preset and clear pulse width t_p	25 ns
Input set up time t_{sp}	t_{cp}
Input hold time t_h	0 ns

Truth Table

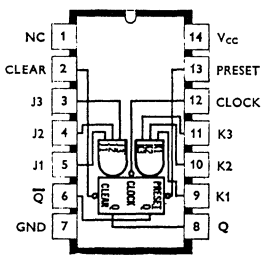
SYNCHRONOUS				ASYNCHRONOUS			
t_n		t_n+1		Preset	Clear	Q	$\overline{Q}$
J	K	Q	$\overline{Q}$	0	0	1	1
0	0	No change		1	0	0	1
1	0	1	0	0	1	1	0
0	1	0	1	1	1	No control	
1	1	Complement					

Logic diagram

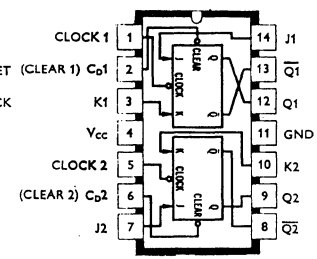


Pin configurations

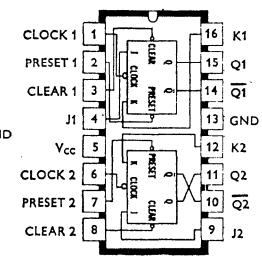
ITT7472



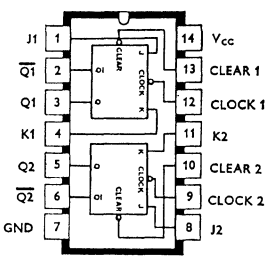
ITT7473



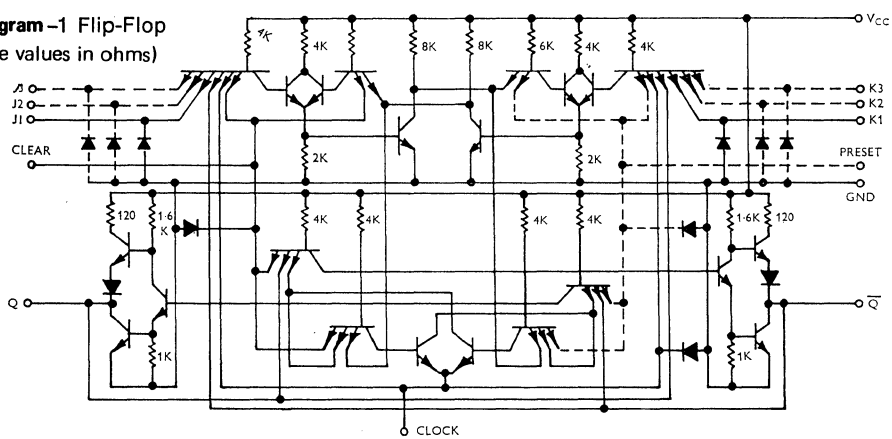
ITT7476



ITT74107



Circuit diagram –1 Flip-Flop
(Resistance values in ohms)



DESCRIPTION

These devices consist of gated Master and slave bistables. The ITT7472 with preset, clear and triple J and K inputs. The ITT7473 and ITT74107 with clear and single J and K inputs. The ITT7476 with preset, clear and single J and K inputs. The direct inputs will operate the device irrespective of the state of clock J or K inputs. The clock input operates as follows, on a positive going transition first the slave bistable is isolated from the master, then information is transferred from the J and K inputs to the master bistable. On a negative going transition first the J and K inputs are disabled then the information is transferred to the slave bistable. Operation will be according to the truth table if J and K information is present before and during the period that the clock is high. Because of the internal feedback from the Q and $\overline{Q}$ outputs to the J and K input AND gates one or other of the gates will have a logical '0' on one internal input. The external inputs cannot affect that gate. The other input AND gate will have a logical '1' on its internal input, if one of the external inputs goes to a logical '1' at any time while the clock is high the master bistable will change state and the Q and $\overline{Q}$ outputs will follow on the negative transition of the clock.

PARAMETER	LIMIT				CONDITIONS	
	Min.	Type at 25°C	Max.	Units	V_{CC}	
$-I_F$ input forward current						
All J and K inputs		1.0	1.6	mA	Max.	V_F=0.4V
Preset, clear and clock		2.0	3.2	mA	Max.	(Note 1)
I_{CC} supply current						
Single type		10	20	mA	Max.	
All dual types		20	40	mA		

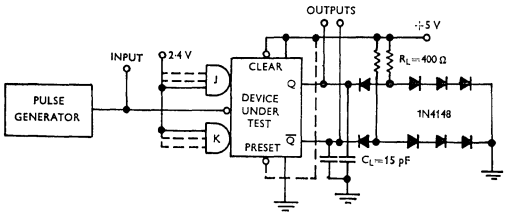
Note 1
Test with all other inputs at 4.5 V. Use preset or clear to set device to appropriate logic state. Clock to be tested for both logic states. When testing J or K inputs all other inputs including internal inputs to the appropriate input AND gate must be at logical '1'.

Information on the absolute maximum ratings and the other D.C. characteristics of this device (which are common to other integrated circuits in this series) is stated in the general information section.

SWITCHING CHARACTERISTICS V_{CC}=5.0V, T_{AMB}=25°C

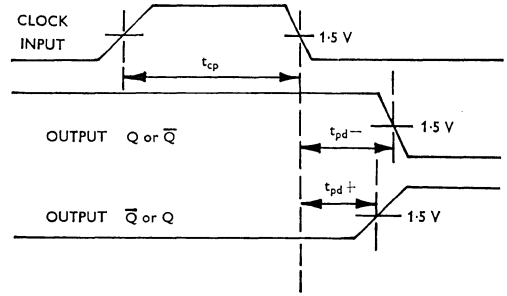
PARAMETER	LIMIT				CONDITIONS
	Min.	Type	Max.	Units	
f_{max} maximum input clock frequency	15	20		MHz	Use test circuit 1
t_{pd}+ propagation delay time to logical '1'					
Clear or preset to output		16	25	ns	Use test circuit 2
Clock to output	10	16	25	ns	Use test circuit 1
t_{pd}- propagation delay time to logical '0'					
Clear or preset to output		25	40	ns	Use test circuit 2
Clock to output	10	25	40	ns	Use test circuit 1

Test Circuit 1



C_L includes probe and jig capacitance

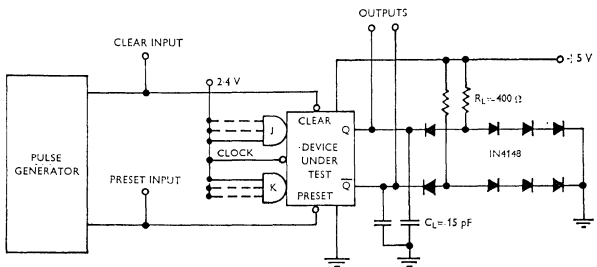
Waveforms



Pulse Characteristics

t_r = 10 ns
t_f = 4 ns
t_{cp} = 20 ns
R.F. = 1 MHz
Amplitude = 3.5 V

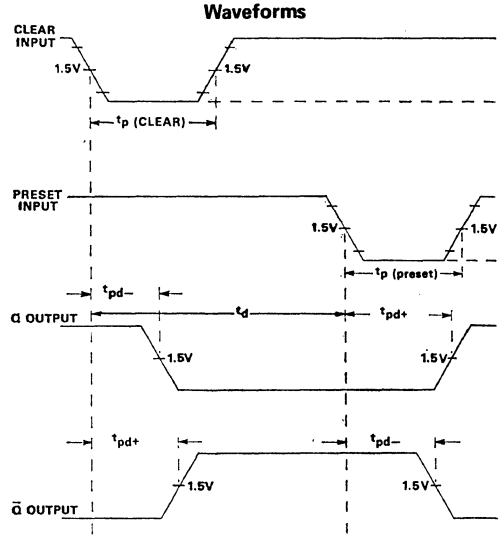
Test circuit 2)



C_L includes probe and jig capacitance

Pulse Characteristics
Same as Test Circuit 1, except t_p =25 ns.

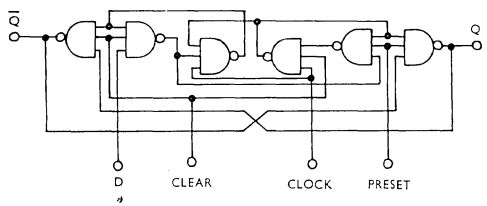
Waveforms



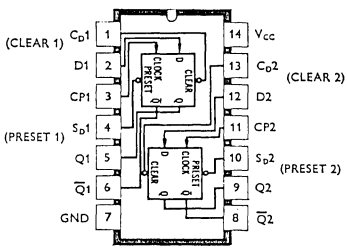
TYPICAL CHARACTERISTICS AND OPERATING CONDITIONS

Maximum clock frequency . . . . . 25 MHz
Propagation delay . . . . . 17 ns
Power dissipation . . . . . 85 mW
Input loading factor:
Preset or data . . . . . 1 unit load
Clear or clock . . . . . 2 unit loads
Fan out . . . . . 1 to 10 unit loads
Clock pulse width t_{cp} . . . . . 30 ns min.
Preset or clear pulse width t_p . . . . . 30 ns min.

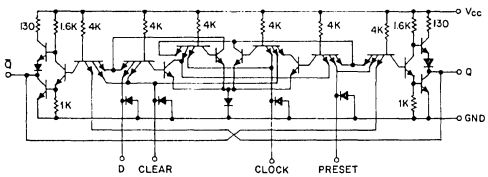
Logic diagram



Pin configuration
(top view)



Circuit diagram of one flip-flop
Resistance values in ohms



Truth Table

SYNCHRONOUS			ASYNCHRONOUS			
t_n		t_n+1	Preset	Clear	Q	$\bar{Q}$
D Input	Q	$\bar{Q}$	0	0	1	1
0	0	1	1	0	0	1
1	1	0	0	1	1	0
			1	1	No Control	

DESCRIPTION

The ITT7474 is an edge triggered D type flip-flop in which the transfer of the D input data takes place during the positive transition of the clock input. When the clock input is above or below the transfer threshold the 'D' input is inhibited. The transfer threshold is not directly related to the transition time of the positive going edge. Preset and clear inputs operate irrespective of the logic state of the clock or D input.

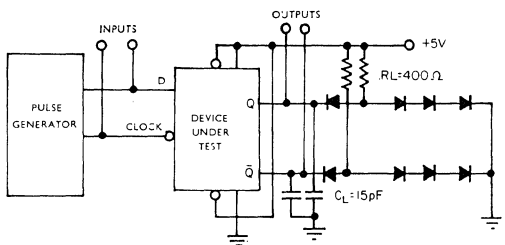
PARAMETER		LIMIT				CONDITIONS	
		Min.	Typ. at 25°C	Max.	Unit	V_{CC}	
$-I_F$	Preset or D input		1.0	1.6	mA	Max.	V_F=0.4V
	Clear or clock		2.0	3.2	mA	Max.	V_F=0.4V
I_R	D input			40	μA	Max.	V_R=2.4V
	Preset or clock			80	μA	Max.	V_R=2.4V
	All inputs			1	mA	Max.	V_R-5.5V
	Clear			120	μA	Max.	V_R=2.4V
I_{CC}			17	30	mA	Max.	All inputs high

Information on the absolute maximum ratings and the other D.C. characteristics of this device (which are common to other integrated circuits in this series) is stated in the general information section.

SWITCHING CHARACTERISTICS V_{CC}=5.0V, T_{AMB}=25°C

PARAMETER	LIMIT				CONDITIONS
	Min.	Typ.	Max.	Unit	
f_{max} maximum input clock frequency	15	25		MHz	Use test circuit 1
t_{sp} minimum input set up time		15	20	ns	Use test circuit 1
t_h minimum input hold time		2	5	ns	Use test circuit 1
t_{pd+} clear or preset to output			25	ns	Use test circuit 2
t_{pd+} clock to output	10	14	25	ns	Use test circuit 1
t_{pd-} clear or preset to output			40	ns	Use test circuit 2
t_{pd-} clock to output	10	20	40	ns	Use test circuit 1

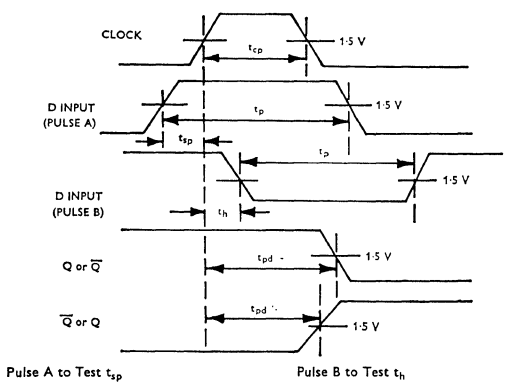
Test Circuit 1



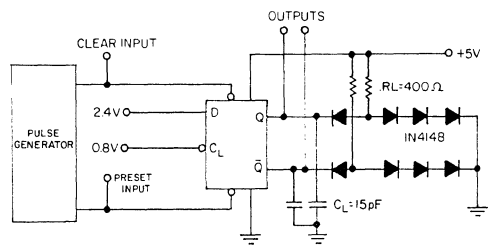
Pulse Characteristics C_L includes probe and jig capacitance

t_r = 10 ns
t_f = 4 ns
t_{cp} = 30 ns
t_p (D input) = 60 ns
R.F. clock = 1 MHz
R.F D input = ½ R.F clock
Amplitude = 3.5 V

Waveforms



Test Circuit 2

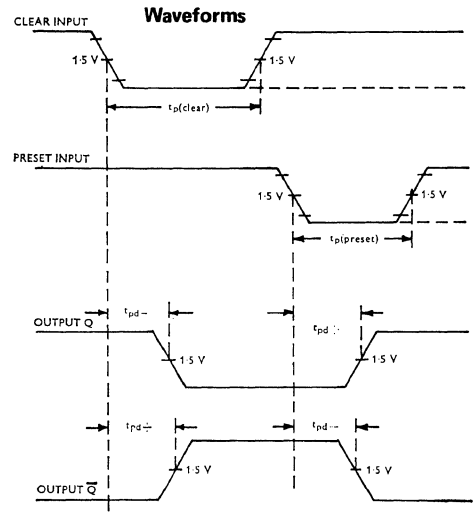


Pulse Characteristics C_L includes probe and jig capacitance

t_r = 4 ns
t_f = 10 ns
t_p = 25 ns
R.F = 1 MHz

Amplitude = 3.5V

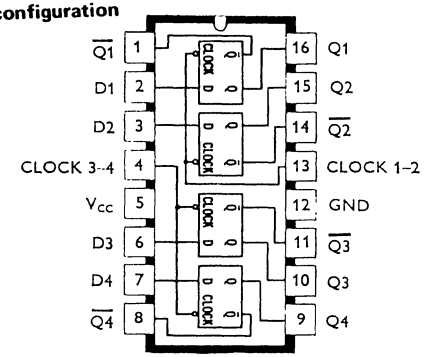
Waveforms



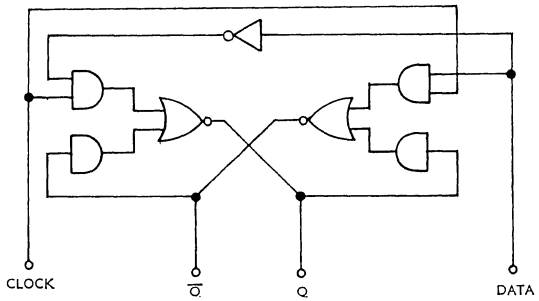
TYPICAL CHARACTERISTICS

Propagation delay . . . . . 12 ns
Power dissipation . . . . . 160 mW
Input loading factor
D input . . . . . 2 unit loads
Clock input. . . . . 4 unit loads
Fan-out . . . . . 1 to 10 unit loads

Pin configuration



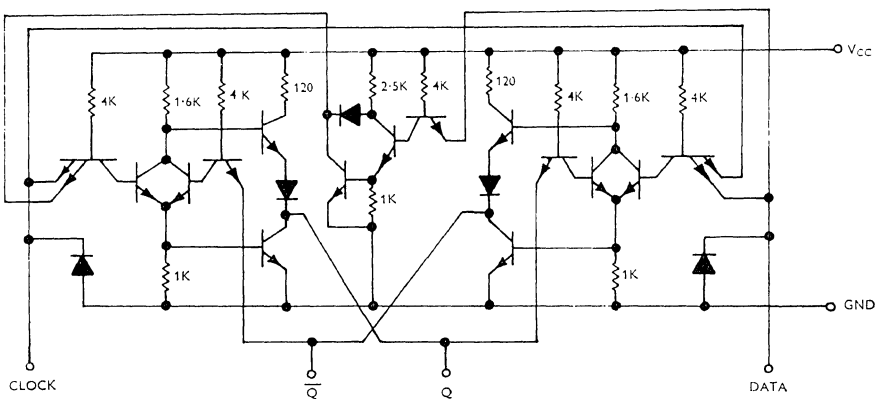
Logic diagram



DESCRIPTION

These latches consist of two cross coupled AND-OR-INVERT gates and one data inverter. When the clock input goes to a logical '0' state the Q output remains in its last logic state. When the clock goes to a logical '1' state the Q output follows the logic state of the D input.

Circuit diagram (Resistance values in ohms)



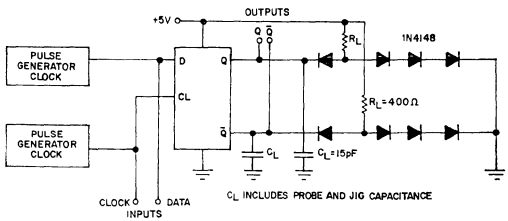
PARAMETER	LIMIT				CONDITIONS	
	Min.	Typ. at 25°C	Max.	Units	V_{CC}	
I_{CCH} supply current highest dissipation state		34		mA	Max.	Clock at logical '0', Data at logical 1'
I_{CCL} supply current lowest dissipation state						
64/7475		28	53	mA	Max.	Clock and data inputs at logical '0'
5475		28	46	mA		

Information on the absolute maximum ratings and the other D.C. characteristics of this device (which are common to other integrated circuits in this series) is stated in the general information section.

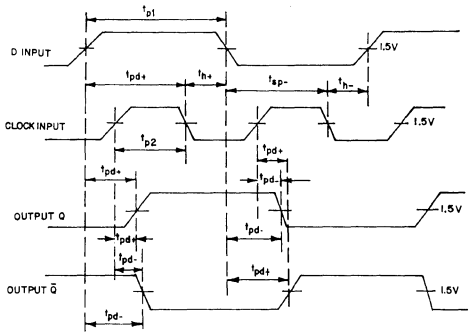
SWITCHING CHARACTERISTICS V_{CC}=5.0V, T_{AMB}=25°C

PARAMETER	LIMIT				CONDITIONS
	Min.	Typ.	Max.	Unit	
t_{sp+} minimum logical '1' set up time 'D' input		7	20	ns	Use test circuit
t_{sp+} minimum logical '0' set up time 'D' input		14	20	ns	Use test circuit
t_{h+} maximum logical '1' hold time at 'D' input	0	−15		ns	Use test circuit
t_{h-} maximum logical '0' hold time at 'D' input	0	−6		ns	Use test circuit
t_{pd+} propagation delay time to logical '1'					
D to Q		16	30	ns	Use test circuit
D to $\bar{Q}$		24	40	ns	Clock at logical '1'
Clock to Q or $\bar{Q}$		16	30	ns	Use test circuit
t_{pd+} propagation delay time to logical '0'					
D to Q		14	25	ns	Use test circuit
D to $\bar{Q}$		7	15	ns	Clock at logical '1'
Clock to Q or $\bar{Q}$		7	15	ns	Use test circuit

Switching test circuit



Waveforms



The pulse generators have the following characteristics

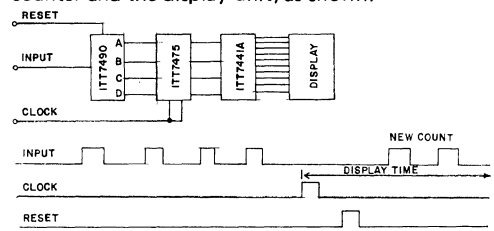
Amplitude	= 3.5 V	R.F data	= ½ clock R.F
t_r	= 10 ns	t_{p1}	= 1 µs
t_f	= 4 ns	t_{p2}	= 500 ns
R.F clock	= 1 MHz		

Phase relation between clock and data signals can be varied to test t_{sp} and t_h.

APPLICATION NOTES

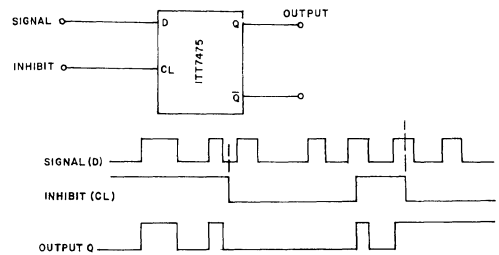
1. Short Term Memory

In counting applications it is usual to display the final count for a period of time, while the counter is counting new information. This requirement is readily fulfilled by using the ITT7445 between the counter and the display unit, as shown.



2. Gating

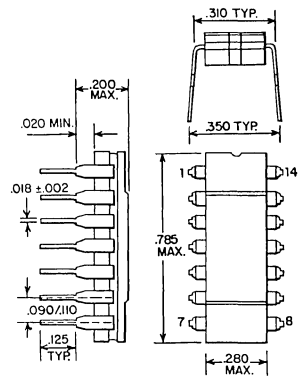
The transfer of signals through a 2 input NAND gate is prevented by applying a logical '0' to the control input. This causes the output always to be high when the gate is closed. It is sometimes required that the output remains in the logic state that is present the instant the inhibit signal is applied. This function is readily achieved by utilizing the ITT7475.

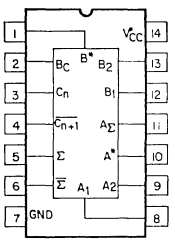


GATED FULL ADDERS

The ITT54/7480J is a single-bit, high-speed, binary full adder with gated complementary inputs, complementary sum (Σ and $\overline{\Sigma}$) outputs and inverted carry output, designed for medium- and high-speed, multiple-bit, parrallel-add/serial-carry applications. The circuit (see schematic diagram) uses diode-transistor logic (DTL) for the gated inputs, and high-speed, high-fan-out transistor-transistor logic (TTL) for the sum and carry outputs. The circuit is entirely compatible with both DTL and TTL logic families. A single-inversion, high-speed, Darlington-connected serial-carry circuit is added to minimize the amount of "look-ahead" and carry cascading circuitry required.

DIMENSIONS





ABSOLUTE MAXIMUM RATINGS

CHARACTERISTICS		UNITS
Supply Voltage V_{CC} (See Note 4)	7	Volts
Input Voltage, V_{in} (See Notes 4 and 5)	5.5	Volts
Operating Case Temperature Range:		
ITT5480J Circuits	−55 to 125	°C
Operating Free-Air Temperature Range:		
ITT5480J, ITT5480J Circuits	−55 to 125	°C
ITT7480J Circuits	0 to 70	°C
Storage Temperature Range	−65 to 150	°C

RECOMMENDED OPERATING CONDITIONS

Supply Voltage V_{CC}:	ITT5480J Circuits	5 Volts ± 10%
	ITT7480J Circuits	5 Volts ± 10%
Fan-Out:	$\overline{C_{n+1}}$, N	1 to 5
	Σ or $\overline{\Sigma}$, N	1 to 10
	A* or B*, N	1 to 3

NOTES:
1. $A = \overline{A^* A_C}$, $B = \overline{B^* B_C}$ where $A^* = \overline{A_1 A_2}$, $B^* = \overline{B_1 B_2}$.
2. When A* or B* are used as inputs, A_1 and A_2 or B_1 and B_2 respectively must be connected to GND.
3. When A_1 and A_2 or B_1 and B_2 are used as inputs, A* or B* respectively must be open or used to perform Dot-OR logic.
4. The voltages are with respect to ground terminal.
5. Input signals must be zero or positive with respect to network ground terminal.

TRUTH TABLE

(See Notes 1, 2, and 3)

C_n	B	A	$\overline{C_{n+1}}$	$\overline{\Sigma}$	Σ
0	0	0	1	1	0
0	0	1	1	0	1
0	1	0	1	0	1
0	1	1	0	1	0
1	0	0	1	0	1
1	0	1	0	1	0
1	1	0	0	1	0
1	1	1	0	0	1

ELECTRICAL CHARACTERISTICS (over operating temperature range unless otherwise noted)

SYMBOL	PARAMETER	TEST FIGURE	MIN	TYP‡	MAX	UNITS	TEST CONDITIONS†
$V_{in(1)}$	Logical 1 input voltage	1 and 2	2			V	V_{CC} = MIN
$V_{in(0)}$	Logical 0 input voltage	1 and 2			0.8	V	V_{CC} = MIN
$V_{out(1)}$	Logical 1 output voltage	2	2.4	3.5		V	V_{CC} = MIN
$V_{out(0)}$	Logical 0 output voltage	1		0.22	0.4	V	V_{CC} = MIN
$I_{in(0)}$	Logical 0 level input current at A_1, A_2, B_1, B_2, A_c or B_c	3			−1.6	mA	V_{CC} = MAX, V_{in} = 0.4 V
$I_{in(0)}$	Logical 0 level input current at A* or B*	4			−2.6	mA	V_{CC} = MAX, V_{in} = 0.4 V
$I_{in(0)}$	Logical 0 level input current at $\overline{C_n}$	4			−8	mA	V_{CC} = MAX, V_{in} = 0.4 V
$I_{in(1)}$	Logical 1 level input current at A_1, A_2, B_1, B_2, A_c or B_c	5			15 1	μA mA	V_{CC} = MAX, V_{in} = 2.4 V V_{CC} = MAX, V_{in} = 5.5 V
$I_{in(1)}$	Logical 1 level input current at $\overline{C_n}$	6			200 1	μA mA	V_{CC} = MAX, V_{in} = 2.4 V V_{CC} = MAX, V_{in} = 5.5 V
I_{os}	Short-circuit output current at Σ or Σ§	7		−20 −18	−57 −57	mA mA	V_{CC} = MAX ITT5480J ITT7480J
I_{os}	Short-circuit output current at C_{n+1}§	7		−20 −18	−70 −70	mA mA	V_{CC} = MAX ITT5480J ITT7480J
I_{CC}	Supply current	8		21 21	31 35	mA mA	V_{CC} = MAX ITT5480J ITT7480J

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time.

SWITCHING CHARACTERISTICS, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM INPUT	TO OUTPUT	FIGURE 9 TEST NO.	MIN	TYP	MAX	UNITS	TEST CONDITIONS
t_{pd1}	C_n	$\overline{C_{n+1}}$	1		13	17	ns	C_L = 15 pF, R_L = 780 Ω
t_{pd0}			2		8	12	ns	C_L = 15 pF, R_L = 780 Ω
t_{pd1}	B_C	$\overline{C_{n+1}}$	3		18	25	ns	C_L = 15 pF, R_L = 780 Ω
t_{pd0}			4		38	55	ns	C_L = 15 pF, R_L = 780 Ω
t_{pd1}	A_C	Σ	5		52	70	ns	C_L = 15 pF, R_L = 400 Ω
t_{pd0}			6		62	80	ns	C_L = 15 pF, R_L = 400 Ω
t_{pd1}	B_C	$\overline{\Sigma}$	7		38	55	ns	C_L = 15 pF, R_L = 400 Ω
t_{pd0}			8		56	75	ns	C_L = 15 pF, R_L = 400 Ω
t_{pd1}	A_1	A*	9		48	65	ns	C_L = 15 pF
t_{pd0}			10		17	25	ns	C_L = 15 pF
t_{pd1}	B_1	B*	11		48	65	ns	C_L = 15 pF
t_{pd0}			12		17	25	ns	C_L = 15 pF

¶ t_{pd1} is propagation delay time to logical 1 level. t_{pd0} is propagation delay time to logical 0 level.

TYPICAL APPLICATIONS

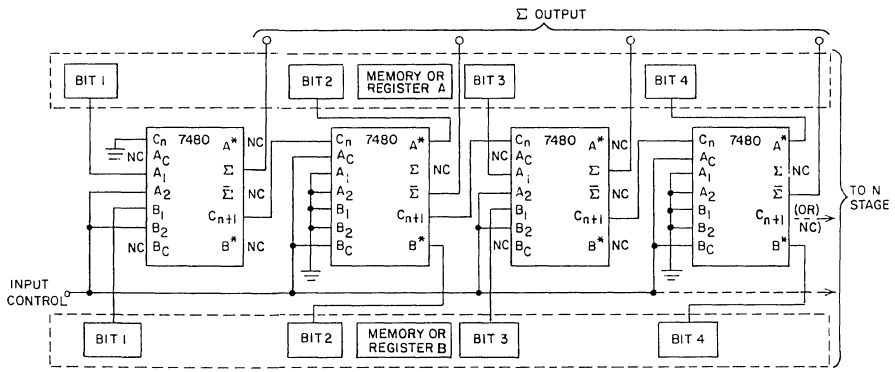
n-bit binary adder or subtractor (see figures A and B)

The ITT7480J is designed specifically for N-bit adder or subtractor operations without external gates or inverters. In both applications, the sum or difference functions are generated in parallel while the carry functions are obtained serially. When the number of stages is small, the add or subtract time determines the maximum system clock rate. However, as the number of bits increases, the time required for the carry function to ripple through each bit becomes the limiting factor. Normally the ripple time of adders built with standard integrated circuits is excessive, and the resulting system speed is so slow that other more complex methods are required to perform these functions.

In the ITT7480J, two methods are used to reduce the carry delay. The carry circuit employs a high-speed Darlington output, and the logic gating has only one inversion between the C_n input and the C_{n+1} output. This logic configuration results in an inverted carry output, and consequently an inverted carry input to the succeeding stage. To counteract this inverted input without sacrificing propagation time through the carry, gates are provided within the circuit to invert the A and B inputs and the resulting sum or difference output. This interconnection method is illustrated by bit 2 and bit 4 of the adder (Figure A). The inverted carry output is a true carry from bit 2 and bit 4, enabling the use of noninverted A and B inputs for the odd-numbered bits.

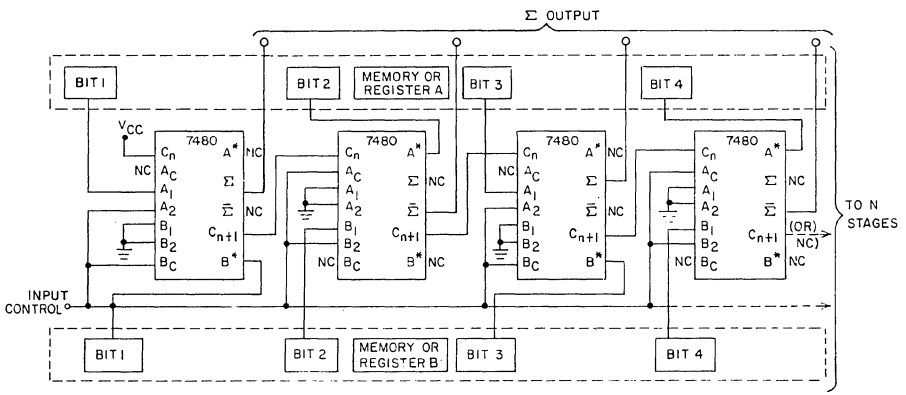
When performing subtraction (Figure B) the C_n input to bit 1 is connected to a logical 1 and input bits and input control functions for the subtrahend (memory or register B) are effectively inverted.

The input control is used to disable the A and B inputs when memory or register information is being shifted. A logical 0 applied to this line will bring each sum or difference output to a logical 0 condition and maintain this level regardless of the state of the input information into each bit. For the adder (Figure A), input control is applied to A_2 and B_2 of odd-numbered bits and to A_C and B_C of even numbered bits. For the subtractor (Figure A), input control is applied to A_2 and B_C of the odd-numbered bits and to A_C and B_2 of the even-numbered bits. These alternating patterns are necessary to complement the varying input sequence which they control.



NOTE: Functions noted as NC are open.

FIGURE A — N-BIT BINARY ADDER



NOTE: Functions noted as NC are open.

FIGURE B — N-BIT BINARY SUBTRACTOR

TYPICAL APPLICATIONS

n-bit binary adder with register selection (see figure C)

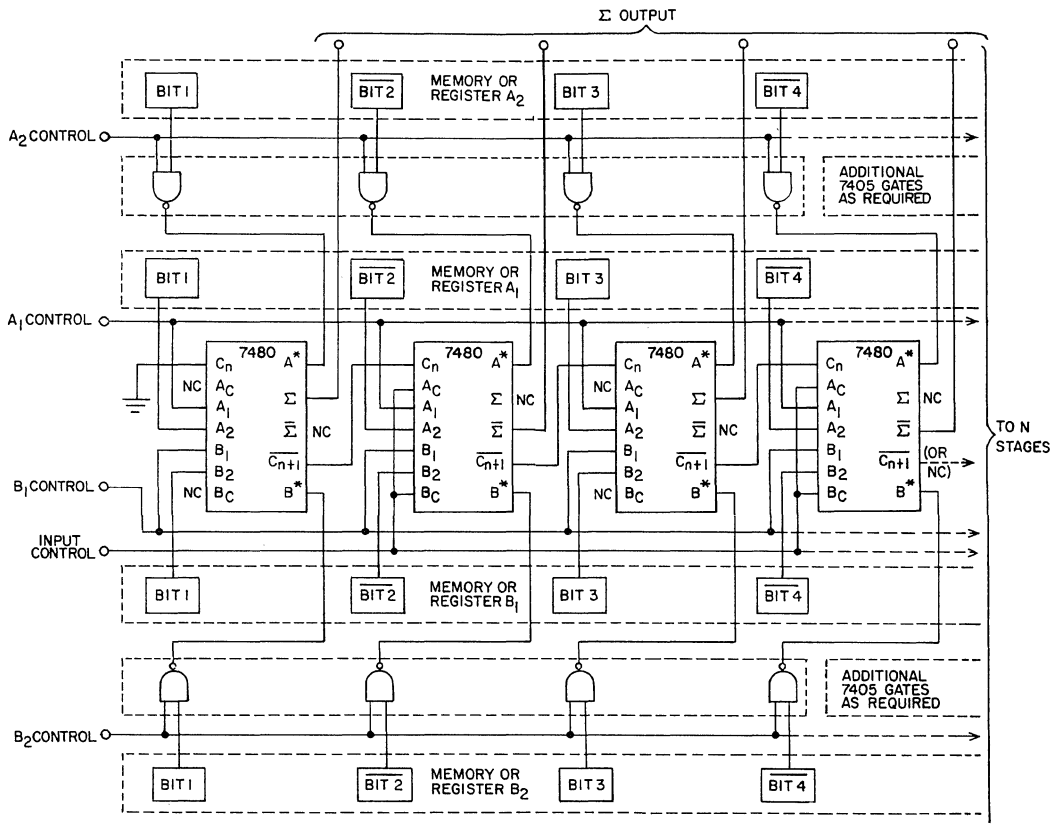
This application fully utilizes the flexibility of the input gating available with the ITT7480J. Two "A" registers and two "B" registers drive a single adder for each bit required. Register selection is performed internally for registers A_1 and B_1, and externally by a type ITT7405J TTL gate for registers A_2 and B_2. Dot-OR logic is performed at the A* and B* nodes within the adder when the register selection is made.

Operation is as follows: To add the contents of Register A_1 to Register B_1, A_2 and B_2 control lines are brought to the logical 0 state. In similar fashion, the contents of register A_1 are added to register B_2 by holding A_2 and B_1 control lines at a logical 0. Four register combinations may be used. Even-numbered input ibts from each register must be inverted since the A* and B* inputs are being used to perform Dot-OR logic. This is not a configuration restriction for flip-flop type registers and memories, but may require additional logic elements if other storage configurations are used as inputs.

The input control function is available as in the previous application and is implemented by bringing all four register control lines and the input control line to a logical 0 level. This condition ensures a logical 0 at each Σ output regardless of "A" and "B" register logic levels.

Up to four "A" registers and four "B" registers may be implemented in a fashion analogous to that shown in Figure C. Inputs from the register-control gates (ITT7405J) of the additional registers would be Dot-OR connected with A_2 and B_2 registers at the A* and B* inputs.

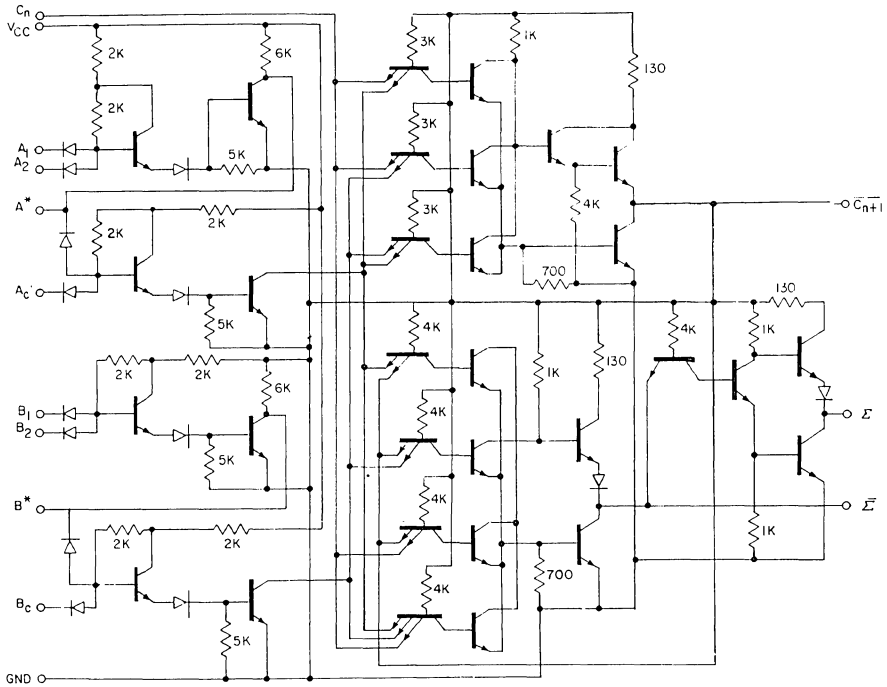
To perform N-bit subtraction, the C_n input at bit 1 is connected to a logical 1 and bit inputs from each register or memory used as a subtrahend must consist of the complement of bit inputs shown for the adder addend. Input control remains the same.



NOTE: Functions noted as NC are open.

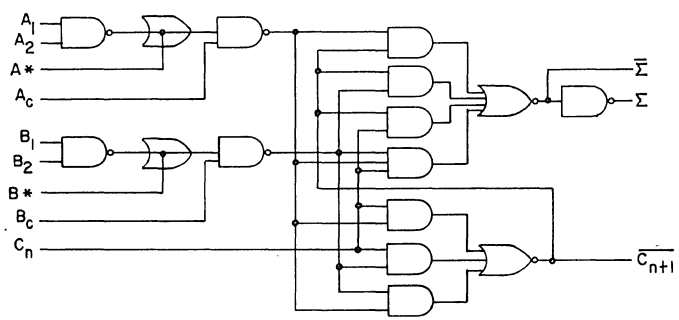
FIGURE C — N-BIT ADDER WITH REGISTER SELECTION

SCHEMATIC



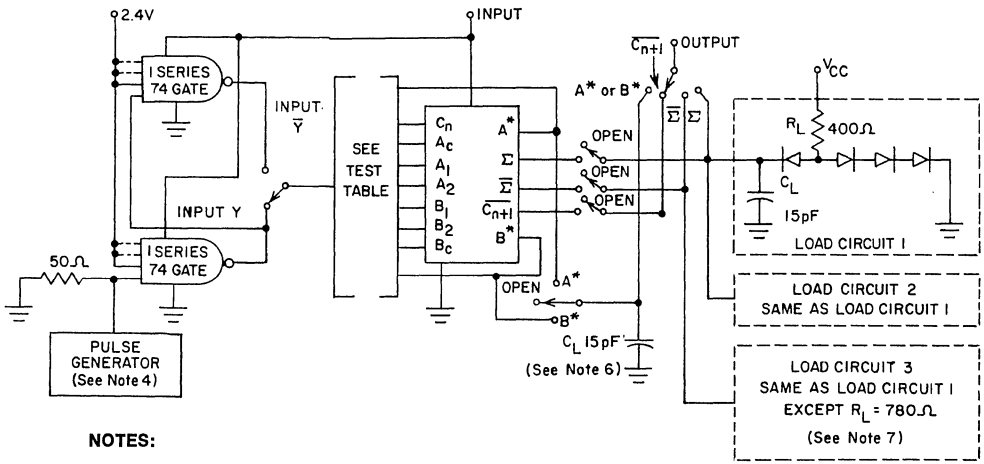
Component values shown are nominal.
Resistor values are in ohms.

FUNCTIONAL BLOCK DIAGRAM



PARAMETER MEASUREMENT INFORMATION

SWITCHING CHARACTERISTICS

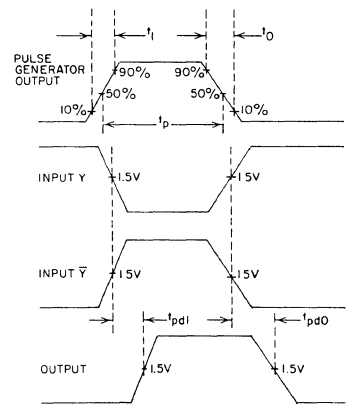


NOTES:

1. Perform test in accordance with test table.
2. Each output is tested separately.
3. Voltage values are with respect to network GND terminal.
4. The generator has the following characteristics: $V_{gen}=3$ V, $t_i=t_o\leq 15$ ns, $t_p=0.5\ \mu$s, PRR=1 MHz, and $Z_{out}\approx 50\ \Omega$.
5. Inputs and outputs not otherwise specified are open.
6. C_L includes probe and jig capacitance.
7. Load circuit 2 simulates output load of 5.
8. All diodes are 1N3064.

TEST TABLE (See Note 5)

TEST NO.	OUTPUT UNDER TEST	APPLY INPUT Y TO	APPLY INPUT Y TO	APPLY +2.4 V TO	APPLY GND TO	APPLY OUTPUT LOADING TO
1	$\overline{C_{n+1}}$	None	C_n	None	B_1	$\overline{C_{n+1}}$ (N=5)
2	$\overline{C_{n+1}}$	None	C_n	None	B_1	$\overline{C_{n+1}}$ (N=5)
3	$\overline{C_{n+1}}$	B_C	None	C_n	A_1, B_1	$\overline{C_{n+1}}$ (N=5)
4	$\overline{C_{n+1}}$	B_C	None	C_n	A_1, B_1	$\overline{C_{n+1}}$ (N=5)
5	Σ	A_C	None	C_n	A_1, B_1	Σ (N=10) Σ (N=10) $\overline{C_{n+1}}$ (N=5)
6	Σ	A_C	None	C_n	A_1, B_1	Σ (N=10) Σ (N=10) $\overline{C_{n+1}}$ (N=5)
7	$\overline{\Sigma}$	B_C	None	C_n	B_1	$\overline{\Sigma}$ (N=10)
8	$\overline{\Sigma}$	B_C	None	C_n	B_1	$\overline{\Sigma}$ (N=10)
9	A*	None	A_1	A_2	None	A* (C_L=15 pF)
10	A*	None	A_1	A_2	None	A* (C_L=15 pF)
11	B*	None	B_1	B_2	None	B* (C_L=15 pF)
12	B*	None	B_1	B_2	None	B* (C_L=15 pF)



VOLTAGE WAVEFORMS

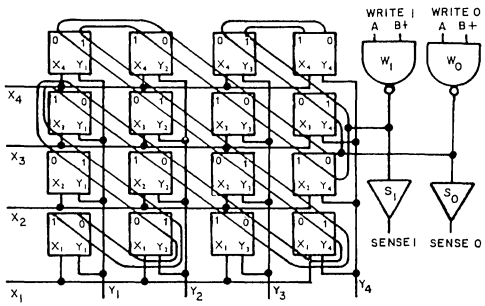
FIGURE 9 — SWITCHING TIMES

ITT7481 DIRECT WRITE INPUT
ITT7484 STROBED WRITE INPUT

TYPICAL CHARACTERISTICS

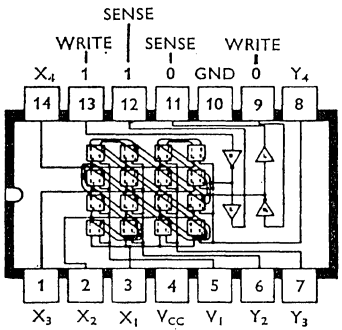
Power dissipation	275 mW
Read time	20 ns
Fan-in	See D.C. tests
Fan-out	See D.C. tests

Logic diagram

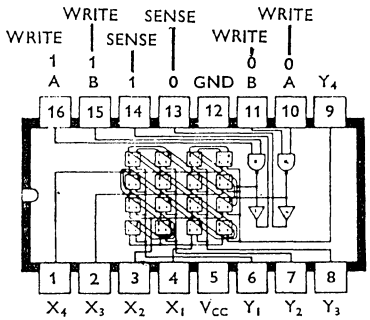


Pin configurations (top view)

ITT7481

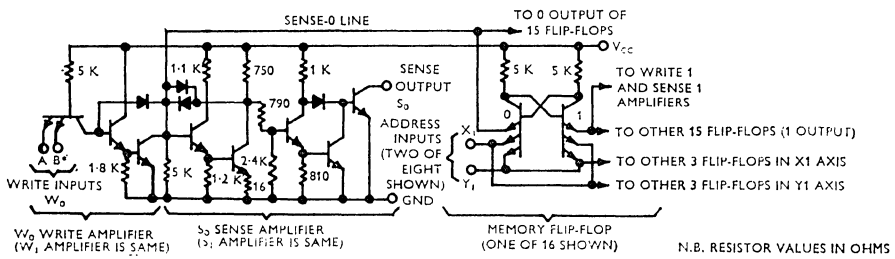


ITT7484



ITT7484 only

Circuit diagram showing one memory element and sense/write '0' amplifier



†The ITT7484 is the same as the ITT7481, but with the addition of strobed write inputs (as shown above).

Note: Sense outputs, S_0 and S_1, are open-collector outputs.

DESCRIPTION

The ITT7481 and ITT7484 are 16-bit memory circuits organized in a 4x4 matrix. Each memory bit can be addressed directly by 4 'X' lines and 4 'Y' lines. Information is contained within each memory element by a bistable transistor circuit, with each transistor having three emitters to provide the necessary gating. The information contained within each element is written in by addressing the particular bit at the address inputs with a logical 1. A 'Zero' is written in by applying a logical 1 to the common write zero input and similarly, a 'one' is written in by applying logical 1 to the common write '1' input. The read-out is non-destructive. Information within each element is read-out by addressing each bit using the appropriate address inputs X_{1-4} and Y_{1-4}. The read output signal is obtained at the output of the sense amplifiers as a logical '0' on the sense 1 or sense 0 outputs depending upon whether there is a logic '1' or '0' stored in the bit.

The information in the memory is destroyed when supply voltage is removed, i.e. it is volatile.

The store can be considered as 16 words of only one bit. A larger scratch pad memory can be constructed by using many of these devices with the appropriate common address lines. Alternatively, the store can be used as a single 16-bit memory with serial write-in and read-out.

PARAMETER	LIMIT				CONDITIONS	
	Min.	Typ.at 25°C	Max.	Unit	V_{CC}	
V_{IH} input voltage at X or Y inputs to ensure writing or sensing	2.1			V	Min.	I_{OL}=20mA*, I_{OL}=40mA†, V_{OL} 0.4V
V_{IH} input voltage at W_0 or W_1 to ensure writing	2			V	Min.	I_{OL}=20mA*, I_{OL}=40mA†, V_{OL}<0.4V
V_{IL} input voltage at X or Y inputs to prevent writing			0.8	V	Min.	I_{OL}=20mA*, I_{OL}=40mA†, V_{OL}<0.4V
V_{IL} input voltage at X or Y inputs to prevent sensing			1	V	Min.	$-I_{OH}$=250μA, V_{OH}=5.5V
V_{IL} input voltage at W_0 or W_1 to prevent writing			1	V	Min.	I_{OL}=20mA*, I_{OL}=40mA†, V_{OL}<0.4V
V_{OH} logical 1 output voltage	5.5			V	Min.	$-I_{OH}$=250μA
V_{OL} logical 0 output voltage			0.4	V	Min.	I_{OL}=20mA*, I_{OL}=40mA†
$-I_F$ logical 0 input current at W_0 or W_1 inputs			1.6	mA	Max.	V_{IL}=0.4V

PARAMETER	LIMIT				CONDITIONS	
	Min.	Typ.at 25°C	Max.	Unit	V_{CC}	See Test Circuit
$-I_F$ logical 0 input current at all X and Y inputs			11	mA	Max.	V_{IL}=0.4V
I_R logical 1 input current at W_0 or W_1 inputs			40	μA	Max.	V_{IH}-2.4V
			1	mA	Max.	V_{IH}-5.5V
I_R logical 1 input current at all X and Y inputs			400	μA	Max.	V_{IH}-4.5V
			3	mA	Max.	V_{IH}=5.5V
I_{CC}						
5481-84		55	78	mA	Max.	
7481-84		55	91	mA	Max.	

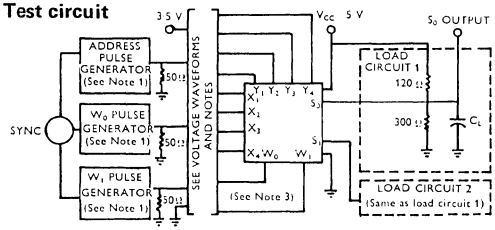
*ITT5481, ITT5484 only.
†ITT7481, ITT7484 only.

Information on the absolute maximum ratings of these devices is stated in the general information section.

SWITCHING CHARACTERISTICS V_{CC}=5V, T_{AMB}=25°C

PARAMETER	LIMIT			CONDITIONS
	Min.	Max.	Unit	
t_{pd-} propagation delay from address inputs	22	45	ns	Address each memory bit C_L=15pF
To sense outputs	27	55	ns	C_L=200pF
t_{pd+} propagation delay from address inputs	15	25	ns	Address each memory bit C_L=15pF
To sense outputs	20	35	ns	C_L=200pF
t_{pd-} propagation delay from address inputs to sense outputs	20	30	ns	C_L=15pFY, locations only addressed. Address X1 to X4
t_{WR} write recovery time	30	60	ns	Address each memory bit C_L=15pF

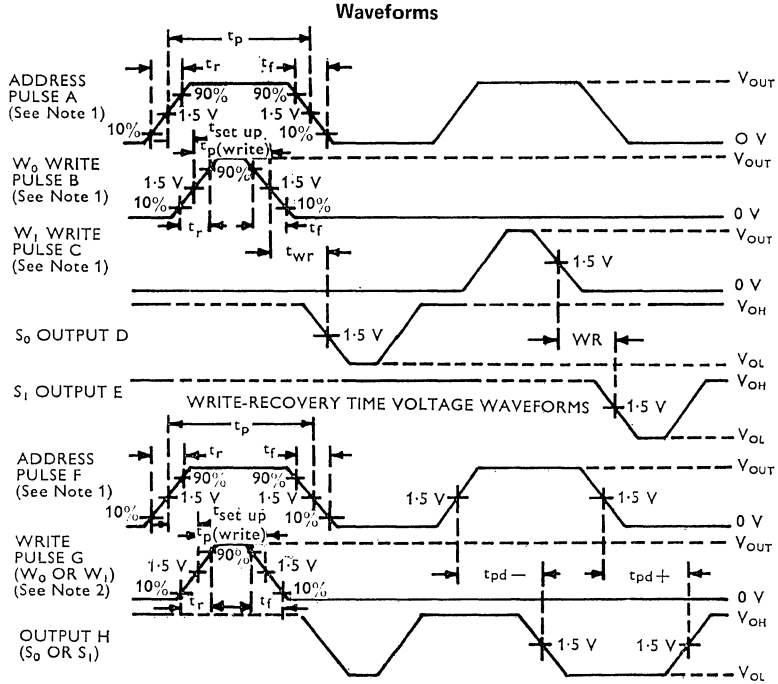
Test circuit



NOTES:

1. The pulse generators have the following characteristics: V_{OUT}=3V, t_r=t_f=10ns, t_{setup}=0 to 10ns. For the address pulse generator, t_p=100ns and P.R.F.=2MHz. For the W_0 and W_1 pulse generators, t_p=25ns and P.R.F.=1MHz.
2. C_L includes probe and jig capacitance.
3. For the ITT7484, unused W_0 and W_1 inputs are 3.5V.

Waveforms

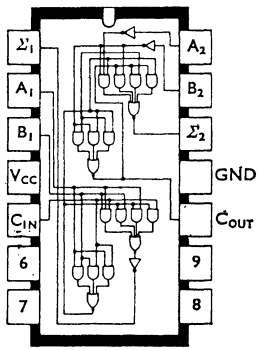


ITT7482
TWO BIT BINARY FULL ADDER

TYPICAL CHARACTERISTICS

Carry propagation delay . . . . . 15 ns
Power dissipation . . . . . 175 mW
Input loading factor at
A_1 B_1 C_{IN} inputs . . . . . 4 unit loads
Input loading factor at A_2 B_2 inputs . . 1 unit load
Maximum fan out Σ_1 Σ_2 output 10
Maximum fan out C_{OUT} output 5

Pin configuration
(top view)



DESCRIPTION

The ITT7482 is a 2-bit binary full adder intended for parallel addition circuits. Sum outputs are provided for each bit and the carry output is obtained by routing the carry from the bit addition through to the second bit addition. The sum output provides full fan-out of 10 from its totem pole output but the carry output is restricted to maximum fan-out of 5.

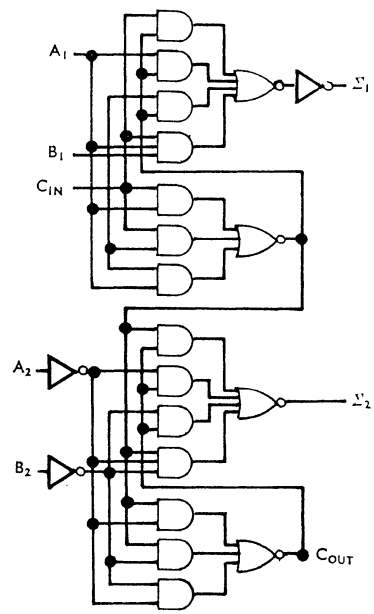
PARAMETER	LIMIT			CONDITIONS
	Min.	Typ.	Max.	Units	
I_{CCH}					
7482		35	58	mA	V_{CC} maximum
5482		35	50	mA	V_{CC} maximum

Information on the absolute maximum ratings and the other D.C. characteristics of this device (which are common to other integrated circuits in this series) is stated in the general information section.
The maximum limit of short circuit output current at C_{OUT} is −70mA.

Truth Table

Input				Output					
				When C_{IN}=0			When C_{IN}=1		
A_1	B_1	A_2	A_2	Σ_1	Σ_2	C_{OUT}	Σ_1	Σ_2	C_{OUT}
0	0	0	0	0	0	0	1	0	0
1	0	0	0	1	0	0	0	1	0
0	1	0	0	1	0	0	0	1	0
1	1	0	0	0	1	0	1	1	0
0	0	1	0	0	1	0	1	1	0
1	0	1	0	1	1	0	0	0	1
0	1	1	0	1	1	0	0	0	1
1	1	1	0	0	0	1	1	0	1
0	0	0	1	0	1	0	1	1	0
1	0	0	1	1	1	0	0	0	1
0	1	0	1	1	1	0	0	0	1
1	1	0	1	0	0	1	1	0	1
0	0	1	1	0	0	1	1	0	1
1	0	1	1	1	0	1	0	1	1
0	1	1	1	1	0	1	0	1	1
1	1	1	1	0	1	1	1	1	1

Logic Diagram

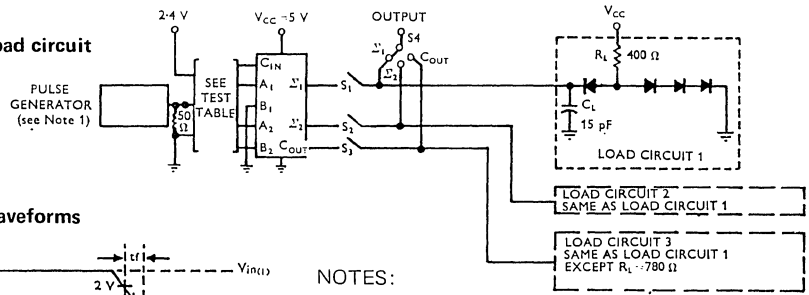


SWITCHING CHARACTERISTICS V_{CC}=5V, T_{AMB}=25°C

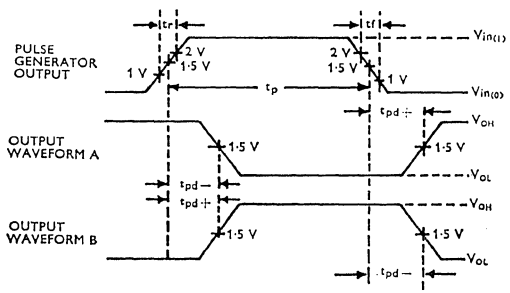
PARAMETER			LIMITS				CONDITIONS		
	From input	To output	Min.	Typ. at 25°C	Max.	Units	V_{CC}		Test No.
t_{pc+}	C_{IN}	Σ_1			34	ns	5V	*	1
t_{pd-}	C_{IN}	Σ_1			40	ns	5V	*	2
t_{pd+}	C_{IN}	Σ_2			38	ns	5V	*	3
t_{pd-}	C_{IN}	Σ_2			42	ns	5V	*	4
t_{pd+}	B_2	Σ_2			40	ns	5V	*	5
t_{pd-}	B_2	Σ_2			35	ns	5V	*	6
t_{pd+}	C_{IN}	C_{OUT}		17	27	ns	5V	*	7
t_{pd-}	C_{IN}	C_{OUT}		12	19	ns	5V	*	8

*As test circuit with C_L=15 pF R_L=400 Ω

Switching test load circuit



Waveforms



NOTES:

1. The generator has the following characteristics: $V_{in(1)} \geq 2.4V$, $V_{in(0)} \leq 0.4V$, t_r = 8 15 ns, t_f = 3 to 5 ns, PRF = 1 MHz, t_p = 200 ns, and $Z_{out} \approx 50\ \Omega$.
2. Perform test in accordance with test table.
3. Each output is tested separately.
4. Voltage values are with respect to network ground terminal.
5. C_L includes probe and jig capacitance.

All diodes are IN4148.

Test Table

Test No.	Parameter	Apply pulse Generator Output to	Output under Test (S4)	Apply 2.4 V to	Apply GND to	S1	S2	S3
1	t_{pd+}	C_{IN}	Σ_1 (Waveform A)	A_1	A_2,B_1,B_2	Closed	Open	Open
2	t_{pd-}							
3	t_{pd+}	C_{IN}	Σ_2 (Waveform A)	A_1,A_2	B_1,B_2	Open	Closed	Closed
4	t_{pd-}							
5	t_{pd+}	B_2	Σ_2 (Waveform B)	None	A_1,B_1,A_2 and C_{IN}	Open	Closed	Open
6	t_{pd-}							
7	t_{pd+}	C_{IN}	C_{OUT} (Waveform B)	A_1,A_2	B_1,B_2	Open	Open	Closed
8	t_{pd-}							

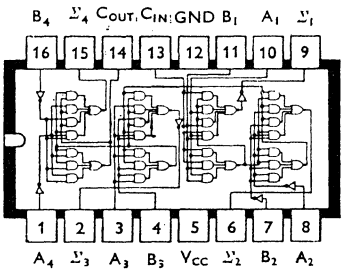
TYPICAL CHARACTERISTICS

Carry propagation delay . . . . . 29 ns
Power dissipation . . . . . 390 mW
Input loading factor (inputs A_1, B_1, A_3, B_3, C_{IN}) . . . . . 4 unit loads
Input loading factor (inputs A_2, B_2, A_4, B_4) . . . . . 1 unit load
Maximum fan out Σ_1 Σ_2 Σ_3 and Σ_4 . . . . . 10 unit loads
Maximum fan out C_{OUT} . . . . . 5 unit loads

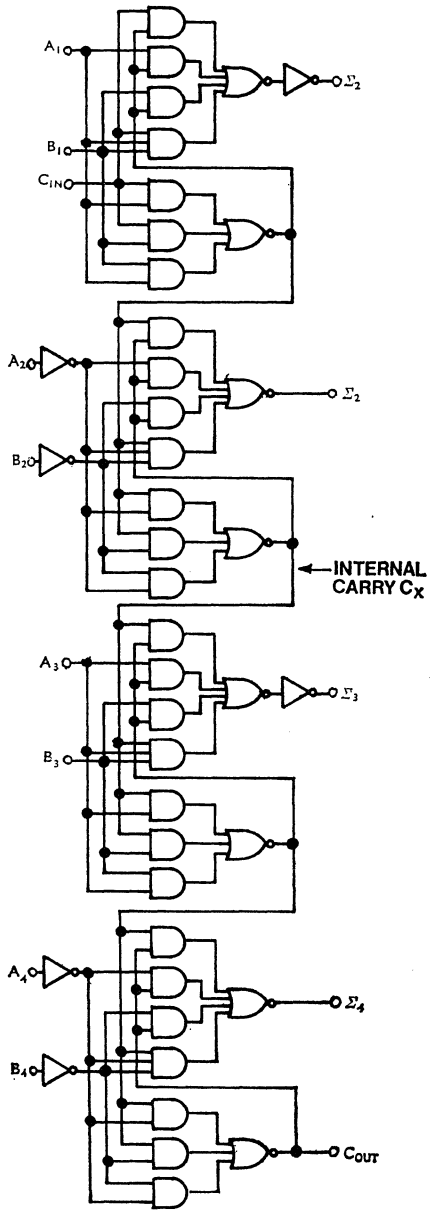
DESCRIPTION

The ITT7483 is a 4 bit binary full adder suitable for parallel add applications. Although the circuit functions using a serial carry technique the overall carry propagation delay is typically less than 30 ns. The sum and carry outputs are the standard totem pole output circuit but with a fan out of 5 on the carry and the full fan out of 10 on each sum output.

Pin configuration (top view)



Logic diagram



First Addition

Inputs				C_{in}=0			C_{in}=1		
A_1	B_1	A_2	B_2	Σ_1	Σ_2	C_x	Σ_1	Σ_2	C_x

Second Addition

Inputs				C_x=0			C_x=1		
A_3	B_3	A_4	B_4	Σ_3	Σ_4	C_{OUT}	Σ_3	Σ_4	C_{OUT}
0	0	0	0	0	0	0	1	0	0
1	0	0	0	1	0	0	0	1	0
0	1	0	0	1	0	0	0	1	0
1	1	0	0	0	1	0	1	1	0
0	0	1	0	0	1	0	1	1	0
1	0	1	0	1	1	0	0	0	1
0	1	1	0	1	1	0	0	0	1
1	1	1	0	0	0	1	1	0	1
0	0	0	1	0	1	0	1	1	0
1	0	0	1	1	1	0	0	0	1
0	1	0	1	1	1	0	0	0	1
1	1	0	1	0	0	1	1	0	1
0	0	1	1	0	0	1	1	0	1
1	0	1	1	1	0	1	0	1	1
0	1	1	1	1	0	1	0	1	1
1	1	1	1	0	1	1	1	1	1

Truth Table

The truth table considers only half of the operation of this full adder – the sum of two bits with the carry input (A_1, A_2 with B_1, B_2). Using the truth table the sum of the first two bits with the carry input (C_{IN}) can be determined giving the first two bits of the sum output (Σ_1 and Σ_2) and an internal carry (C_x). This internal carry is added to the last two bits of the binary input signal (A_3, A_4 with B_3, B_4) to give the last two bits of the sum output (Σ_3 and Σ_4) and the carry output (C_{OUT}). By using the truth table again for the second addition the outputs can be determined for any condition of the inputs.

PARAMETER	LIMITS				CONDITIONS
	Min.	Typ.at 25°C	Max.	Units	V_{CC}
I_{CCH}					
7483		78	128	mA	Max. V_{IN}=4.5V
5483		78	110	mA	Max. V_{IN}=4.5V

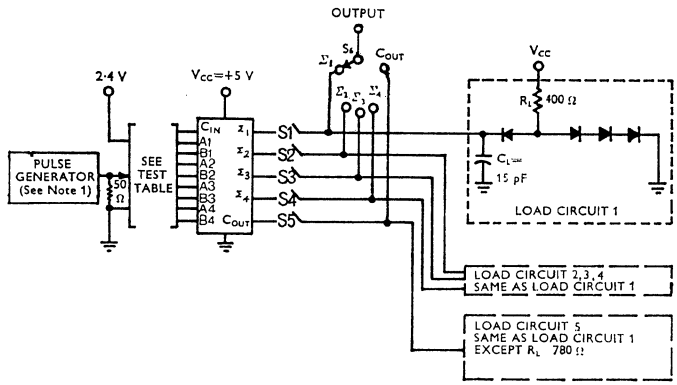
Information on the absolute maximum ratings and the other D.C. characteristics of this device (which are common to other integrated circuits in this series) is stated in the general information section.
The maximum limit of short circuit output current at C_{OUT} is −70 mA.

SWITCHING CHARACTERISTICS V_{CC}=5V, T_A=25°C

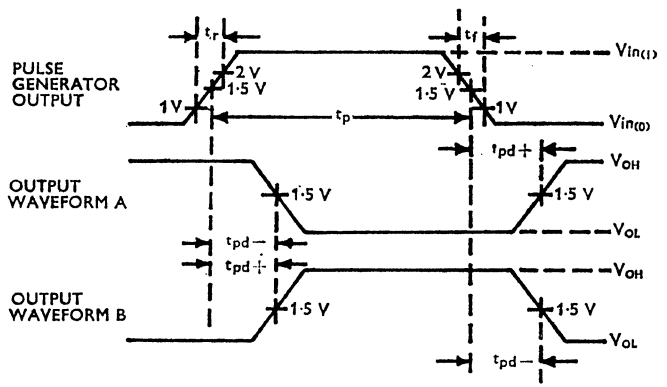
PARAMETER			LIMITS				CONDITIONS	
	From input	To output	Min.	Typ.	Max.	Unit		Test No.
t_{pd+}	C_{IN}	1			34	ns	*C_L=15 pF, R_L=400 Ω	1
t_{pd-}	C_{IN}	1			40	ns	*C_L=15 pF, R_L=400 Ω	2
t_{pd+}	C_{IN}	2			38	ns	*C_L=15 pF, R_L=400 Ω	3
t_{pd-}	C_{IN}	2			42	ns	*C_L=15 pF, R_L=400 Ω	4
t_{pd+}	C_{IN}	3			50	ns	*C_L=15 pF, R_L=400 Ω	5
t_{pd-}	C_{IN}	3			60	ns	*C_L=15 pF, R_L=400 Ω	6
t_{pd+}	C_{IN}	4			55	ns	*C_L=15 pF, R_L=400 Ω	7
t_{pd-}	C_{IN}	4			55	ns	*C_L=15 pF, R_L=400 Ω	8
t_{pd+}	C_{IN}	C_{OUT}		35	48	ns	*C_L=15 pF, R_L=780 Ω	9
t_{pd-}	C_{IN}	C_{OUT}		22	32	ns	*C_L=15 pF, R_L=780 Ω	10
t_{pd+}	A_2 or B_2	2			40	ns	*C_L=15 pF, R_L=400 Ω	11,13
t_{pd-}	A_2 or B_2	2			35	ns	*C_L=15 pF, R_L=400 Ω	12,14
t_{pd+}	A_4 or B_4	4			40	ns	*C_L=15 pF, R_L=400 Ω	15,17
t_{pd-}	A_4 or B_4	4			35	ns	*C_L=15 pF, R_L=400 Ω	16,18

*See switching test circuit and test table.

Switching test circuit



Waveforms



Notes:

1. Pulse generator output characteristics: $V_{in(1)} \geq$ 2.4 V, $V_{in(0)} \leq$ 0.4 V, t_r = 8 to 15 ns, t_f = 3 to 5 ns, P.R.F. = 1 MHz, tp = 200 ns, and $Z_{out} \backsimeq 50\ \Omega$.
2. Perform test in accordance with test table.
3. Each output is tested separately.
4. Voltage values are with respect to network ground terminal.
5. C_L includes probe and jig capacitance.
6. All diodes are IN4148.

Test Table

Parameter	Apply pulse generator output to	Output under test (S6)	Apply 2.4V to	Apply GND to	S1	S2	S3	S4	S5	Test No.
t_{pd+}	C_{IN}	Σ_1 (Waveform A)	A_1	B_1, A_2, and B_2	Closed	Open	Open	Open	Open	1
t_{pd-}										2
t_{pd+}	C_{IN}	Σ_2 (Waveform A)	A_1 and A_2	B_1 and B_2	Open	Closed	Open	Open	Open	3
t_{pd-}										4
t_{pd+}	C_{IN}	Σ_3 (Waveform A)	A_1, A_2, and A_3	B_1, B_2, and B_3	Open	Open	Closed	Open	Open	5
t_{pd-}										6
t_{pd+}	C_{IN}	Σ_4 (Waveform A)	A_1, A_2, A_3, and A_4	B_1, B_2, B_3, and B_4	Open	Open	Open	Closed	Open	7
t_{pd-}										8
t_{pd+}	C_{IN}	C_4 (Waveform A)	A_1, A_2, A_3, and A_4	B_1, B_2, B_3, and B_4	Open	Open	Open	Open	Closed	9
t_{pd-}										10
t_{pd+}	A_2	Σ_2 (Waveform A)	A_1, B_1, B_2, None	A_1, B_1, B_2, and C_{IN}	Open	Closed	Open	Open	Open	11
t_{pd-}										12
t_{pd+}	B_2	Σ_2 (Waveform B)	None	A_1, B_1, A_2, and C_{IN}	Open	Closed	Open	Open	Open	13
t_{pd-}										14
t_{pd+}	A_4	Σ_4 (Waveform B)	None	A_3, B_3, and B_4	Open	Open	Open	Closed	Open	15
t_{pd-}										16
t_{pd+}	B_4	Σ_4 (Waveform B)	None	A_3, B_3, and A_4	Open	Open	Open	Closed	Open	17
t_{pd-}										18

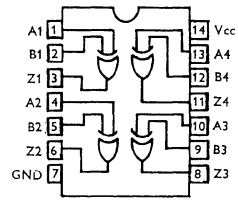
Inputs not specified are open

ITT7486
QUAD 2 INPUT EXCLUSIVE OR GATE

TYPICAL CHARACTERISTICS

Propagation Delay . . . . . 12 ns
Power Dissipation . . . . . 150 mW
Input Loading Factor . . . . . 1 unit load
Fan-out:
Logical '0' . . . . . 1 to 10 unit loads
Logical '1' . . . . . 1 to 20 unit loads

Pin Configuration



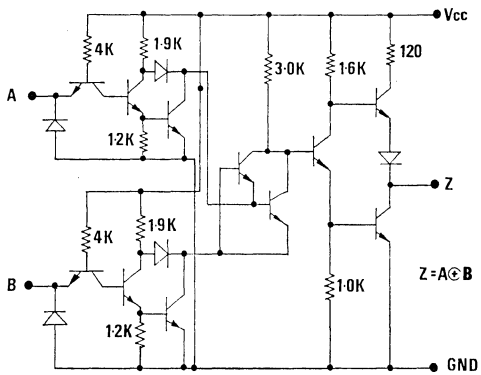
Top view

Truth Table

Inputs		Output
A	B	Z
0	0	0
0	1	1
1	0	1
1	1	0

DESCRIPTION

The 'Exclusive OR' function is correctly represented in Boolean Expressions as $Z = AB + \overline{A}\overline{B}$ but is often abbreviated to $Z = A \oplus B$. The operation is also represented in the truth table shown above, a convenient memory aid is to consider the device as a One Bit adder without carry. The fan-out of 20 provided in the logical '1' state is to facilitate the connection of unused inputs to used inputs.



Circuit diagram of one gate

Resistance values in ohms

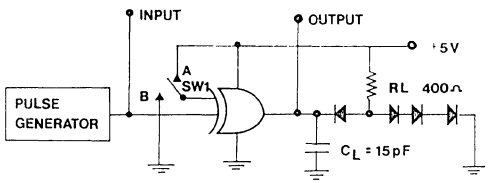
PARAMETER	LIMIT				CONDITIONS	
	Min.	Typ.at 25°C	Max.	Units	V_{CC}	
I_{CCH} supply current highest dissipation state						
74 series		30	50	mA	Max.	All inputs at logical '0'
54 series		30	43	mA	Max.	
I_{CCL} supply current lowest dissipation state						
74 series		26		mA	Max.	One input at 0 and
54 series		26		mA	Max.	one at '1' on each gate

Information on the absolute maximum ratings and the other D.C. characteristics of this device (which are common to other integrated circuits in this series) is stated in the general information section.

SWITCHING CHARACTERISTICS V_{CC}=5.0V, T_{AMB}=25°C

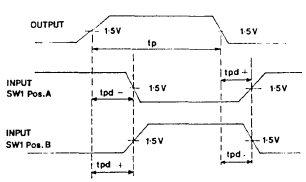
PARAMETER	LIMIT				CONDITIONS
	Min.	Typ.	Max.	Units	
t_{pd+} propagation delay time to logical '1'		15	23	ns	
other input low		15	23	ns	Use switching load
other input high		18	30	ns	circuit
t_{pd-} propagation delay time to logical '0'					
other input low		11	17	ns	Use switching load
other input high		13	22	ns	circuit

Switching load circuit



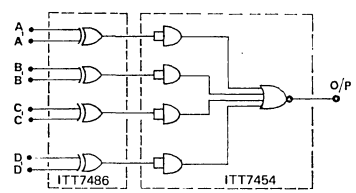
Pulse Characteristics
Amplitude = 3.5 V
t_r = 10 ns
t_f = 4 ns
R.F = 1 MHz
t_p = 500 ns

Waveforms



APPLICATION NOTE

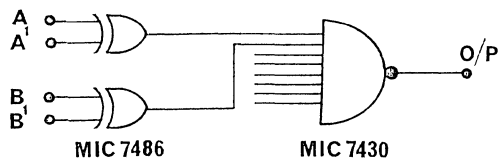
Comparator



The above circuit shows a two 4 bit number comparator which requires only the true signal of each number. When A=A^1, B=B^1, C=C^1, D=D^1 the ITT7453 output is a logical '1'.

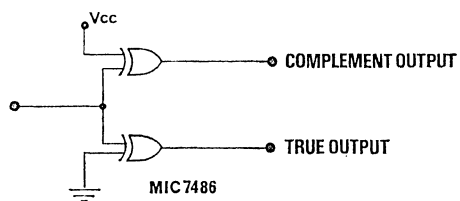
Comparator

This comparator uses the true signal of one number and the complement of the other, it can be conveniently extended to compare two 8 bit numbers. When A=A^1, B=B^1, C=C^1, D=D^1, E=E^1, F=F^1, G=G^1, H=H^1, the output will be at logical '0'.



20 MHz Phase Splitter

At high frequency it is difficult to produce a complement of a signal with inverse mark space ratio equal to that of the true signal and without phase delay. The circuit shown produces true and complement outputs with one transition of each almost simultaneous. On the other transitions there is up to a 5 ns difference depending to some extent on fan-out loading.



ITT7490
ASYNCHRONOUS DECADE COUNTER

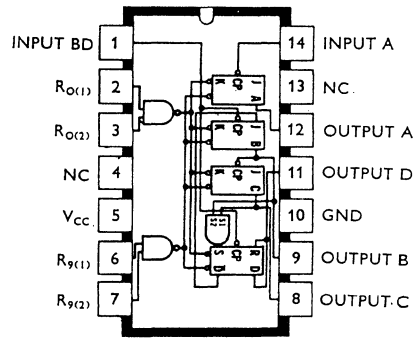
- **Divide by 2**
- **Divide by 5**
- **Divide by 10**
- **BCD or Symmetrical Divide by 10 Count**

TYPICAL CHARACTERISTICS

Propagation delay (ripple delay)	60 ns
Max. clock frequency	18 MHz
Power dissipation (over full count sequence)	135 mW
Input loading factor	
$R_{0(1)}$, $R_{0(2)}$, $R_{9(1)}$, $R_{9(2)}$	1 unit load
Clock A input	2 unit loads
Clock BD input	4 unit loads
Fan-out from each output (Note 1)	10 unit loads
Clock pulse width	50 ns min.
Reset pulse width	50 ns min.

Pin configuration

(top view)



Note 1

For a divide by 10 count, with Pin 12, O/P A, connected to pin 1, I/P BD, the full fan-out is still permissible from O/P A.

DESCRIPTION

The decade counter consists of four master slave flip-flops. Flip-flop 'A' provides a divide-by-2 function. The remaining three flip-flops are internally connected to provide a divide-by-5 counter. Counting occurs on the negative edge of the clock. Inputs $R_{0(1)}$ and $R_{0(2)}$ are gated to provide reset to zero, and inputs $R_{9(1)}$ and $R_{9(2)}$ are gated to provide reset to BCD count of nine. All inputs have input clamping diodes and outputs are standard 7400 series configuration.

Because output A is not internally connected to the succeeding flip-flops three count modes are available:

1. BCD mode is obtained by externally connecting A output (pin 12) to clock BD input (pin 1).

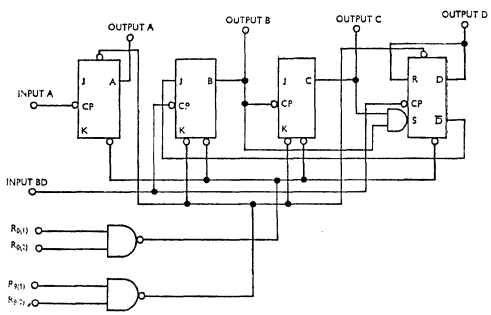
2. A symmetrical divide by 10 count is obtained by externally connecting D output (pin 11) to clock A input (pin 14).

3. The device may be used as separate divide-by-2 and divide-by-5 counters but with common reset lines.

The counters may be cascaded to provide any number count.

DECADE COUNTER

Logic Diagram



Truth Table

BCD COUNT SEQUENCE					RESET/COUNT							
Count	Outputs				Reset Inputs				Outputs			
	D	C	B	A	$R_{0(1)}$	$R_{0(2)}$	$R_{9(1)}$	$R_{9(2)}$	D	C	B	A
0	0	0	0	0	1	1	0	X	0	0	0	0
1	0	0	0	1	1	1	X	0	0	0	0	0
2	0	0	1	0	0	X	1	1	1	0	0	1
3	0	0	1	1	X	0	1	1	1	0	0	1
4	0	1	0	0	1	1	1	1	1	0	0	1*
5	0	1	0	1	X	0	0	X	Count			
6	0	1	1	0	0	X	X	0	Count			
7	0	1	1	1	0	X	0	X	Count			
8	1	0	0	0	X	0	X	0	Count			
9	1	0	0	1								

X indicates that logical '1' or logical '0' may be present.

*When resuming the count mode $R_{0(1)}$ or $R_{0(2)}$ must be switched to logical '0' before $R_{9(1)}$ or $R_{9(2)}$ are switched to logical '0' to ensure that the counter remains at BCD count of 9.

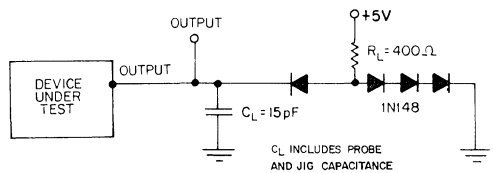
PARAMETER	LIMIT				CONDITIONS	
	Min.	Typ. at 25°C	Max.	Units	V_{CC}	
I_{CCH}						All outputs at 0
						R_0 and R_9 at 0
7490		32	53	mA	Max.	V_{IN} = 5.0V
5490		32	46	mA		
I_{CCL}						BCD count of 7
7490		21	35	mA	Max.	V_{IN} = 5.0V
5490		21	30	mA		

Information on the absolute maximum ratings and the other D.C. characteristics of this device (which are common to other integrated circuits in this series) is stated in the general information section.

SWITCHING CHARACTERISTICS V_{CC}=5.0V, T_{AMB}=25°C

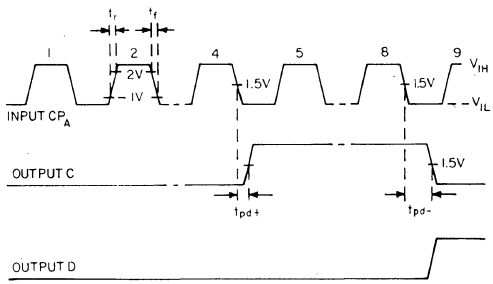
PARAMETER	LIMIT				CONDITIONS
	Min.	Typ.	Max.	Unit	
f_{max}	10	18		MHz	Load circuit on each output
t_{pd+} From input 'A' to output 'C'		60	100	ns	Load circuit on each output
t_{pd-} From input 'A' to output 'C'		60	100	ns	Load circuit on each output

Switching load circuit



Waveforms

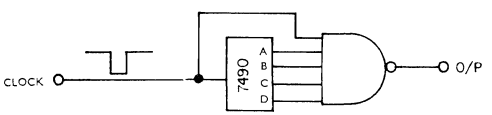
CP_A INPUT PULSE CHARACTERISTICS
Amplitude 3·5 V
tr = 10ns tf = 4 ns
P.R.F. = 1 MHz duty cycle = 50%



APPLICATION NOTES

1. Ripple Delay

In asynchronous counters ripple delay always occurs. It is defined as the time interval between the clock pulse edge at the first stage and the instant a succeeding stage changes state. When decoding the outputs of the counter false outputs can occur at the transitions from an odd count state to an even count state. The false output will always represent a lower count than the true state. When using the counter with decoding the possibility of such false outputs can be prevented by inhibiting the decode gate with the clock signal.

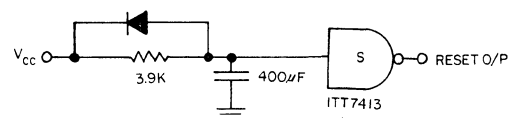


2. Count Range, Less Than Ten

Typically when feeding back outputs signals from the counter by direct connection from outputs to reset inputs $R_{0(1)}$ and $R_{0(2)}$ the counter will reset and start a new count sequence. Feedback can be obtained in this manner from all count states except 7 which will require a three input NAND gate and an inverter in the feedback loop. Under extreme worst case conditions of direct feedback it is possible that not all stages will reset; correct resetting can be ensured by using external gating for all count states. When resetting in either manner the reset count state will be on the outputs for the time it takes for resetting to occur.

3. Illegal Start Up States

On application of supply voltage each flip-flop in a counter may start up in either state. It is, therefore, possible for the counter to assume any one of the 16 possible states. With any type of counter which uses internal gating to restrict the count sequence, the 7490 being no exception, the illegal states (BCD 10 to 15), could be obtained. If this is the case, application of clock pulses will enable the counter to count out of this state, after which normal operation will follow. If, however, it is essential that such conditions are avoided arrangements should be made to provide a reset signal during initial application of supply voltage. A circuit which will generally prove satisfactory is shown below.

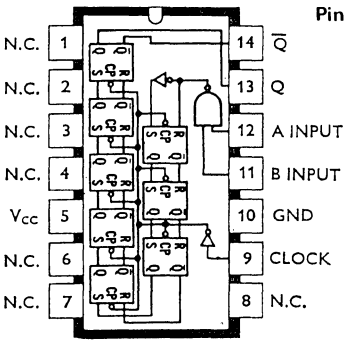


For further details see ITT7413

- **Gated Serial Input**
- **True and Complement Serial Output**

TYPICAL CHARACTERISTICS

Maximum clock frequency	18 MHz
Propagation delay	26 ns
Power dissipation	175 mW
Input loading factor	1 unit load
Fan-out	1 to 10 unit loads
Clock pulse width t_{cp}	25 ns min.
Serial input set up time t_{sp}	25 ns min.
Serial input hold time t_h	0 ns

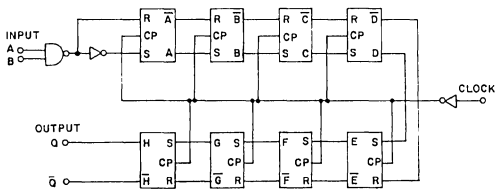


Pin configuration
(top view)

PARAMETER	LIMIT				CONDITIONS	
	Min.	Typ.at .25°C	Max.	Units	V_{CC}	
I_{CC}						
7491A	35	58		mA	Max.	All inputs
5491A	35	50		mA		at logical '0'

Information on the absolute maximum ratings and the other D.C. characteristics of this device (which are common to other integrated circuits in this series) is stated in the general information section.

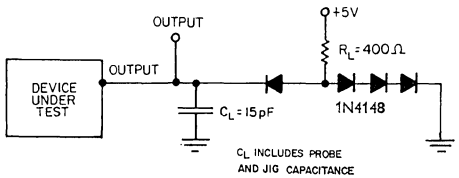
Logic diagram



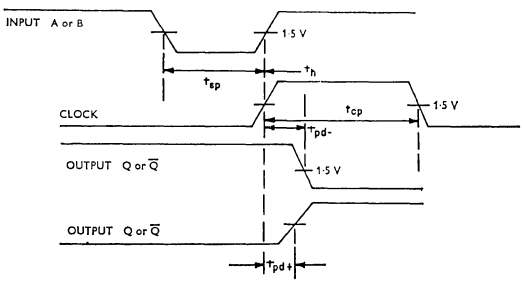
DESCRIPTION

The ITT7491A consists of eight master slave flip-flops connected to form an 8 bit shift register. The last stage has standard TTL outputs for both Q and $\overline{Q}$. Gated serial input function is provided by a 2 input NAND gate and an inverter. The common clock input has an inverting buffer to maintain a fan-in of unity. Information in the register is shifted on the positive edge of the clock. All inputs are provided with input clamping diodes. These registers may be cascaded to form any length of shift register.

Switching load circuit



Waveforms



SWITCHING CHARACTERISTICS, V_{CC} = 5.0 V, T_{AMB} = 25°C

PARAMETER	LIMIT				CONDITIONS
	Min.	Typ.	Max.	Unit	
f_{max}	10	18		MHz	Use switching load circuit on each output
t_{pd+}		24	40	ns	Clock to output
t_{pd-}		27	40	ns	Clock to output

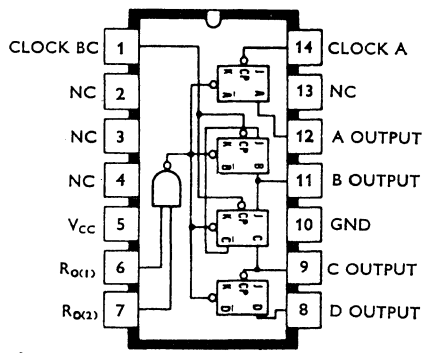
ITT7492
ASYNCHRONOUS DIVIDE BY TWELVE COUNTER

Divide by 2 • Divide by 3 • Divide by 6 • Divide by 12

TYPICAL CHARACTERISTICS

Propagation delay (ripple delay) . . . . . 60 ns
Maximum clock frequency . . . . . 18 MHz
Power dissipation (over full count sequence) . . . . . 124 mW
Input loading factor:
$R_{0(1)}$, $R_{0(2)}$ . . . . . 1 unit load
Clock A input . . . . . 2 unit loads
Clock BC input . . . . . 4 unit loads
Fan-out from each output (Note 1) $\leq$ 10 unit loads
Clock pulse width . . . . . 50 ns min.
Reset pulse width . . . . . 50 ns min.

Pin configuration (top view)



Note 1
For a divide by 12 count, with pin 12, O/P A connected to Pin 1, I/P BC, the full fan-out of 10 is still permissible from O/P A.

DESCRIPTION

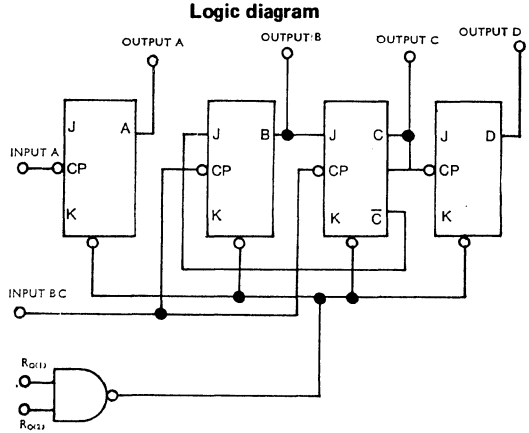
The divide-by-twelve counter consists of four master slave flip-flops. Flip-flop 'A' provides a divide-by-2 function. The remaining three flip-flops are internally connected to provide a divide-by-6 count. Counting occurs on the negative edge of the clock input. Inputs $R_{0(1)}$ and $R_{0(2)}$ are gated to provide reset to zero. All inputs have input clamping diodes and outputs are standard 74 series configuration.

Because output A is not internally connected to the succeeding flip-flops there are two count modes available:

1. Divide-by-twelve mode is obtained by externally connecting A output (pin 12) to clock BC input (pin 1). Outputs A, C and D give simultaneous division by 2, 6 and 12 respectively.
2. The device may be used as separate divide-by-2 and divide-by-6 counters but with common reset lines. Outputs C and D give simultaneous division by 3 and 6 respectively.

The counters may be cascaded to provide any number count.

Logic diagram



Truth Table

COUNT SEQUENCE

Count	Outputs			
	D	C	B	A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	1	0	0	0
7	1	0	0	1
8	1	0	1	0
9	1	0	1	1
10	1	1	0	0
11	1	1	0	1

RESET/COUNT

To Count:
Either $R_{0(1)}$ or $R_{0(2)}$ or both reset inputs must be at logical '0'.

To Reset:
Both $R_{0(1)}$ and $R_{0(2)}$ must be at logical '1'.

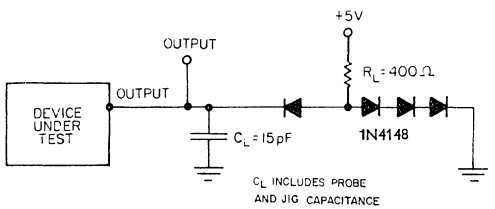
PARAMETER	LIMIT				CONDITIONS	
	Min.	Typ. at 25°C	Max.	Units	V_{CC}	
I_{CCH}						All inputs at 0, R_0 at 0
7492		31	51	mA	Max.	V_{IN} = 5.0 V
5492		31	44	mA		
I_{CCL}						Count of 9 or 11
7492		20		mA	Max.	V_{IN} = 5.0 V
5492		20		mA		

Information on the absolute maximum ratings and the other D.C. characteristics of this device (which are common to other integrated circuits in this series) is stated in the general information section.

SWITCHING CHARACTERISTICS V_{CC}=5.0V, T_{AMB}=25°C

PARAMETER	LIMIT				CONDITIONS
	Min.	Typ.	Max.	Unit	
f_{max}	10	18		MHz	Load circuit on each output
t_{pd+} From input 'A' to output 'D'		60	100	ns	Load circuit on each output
t_{pd-} From input 'A' to output 'D'		60	100	ns	Load circuit on each output

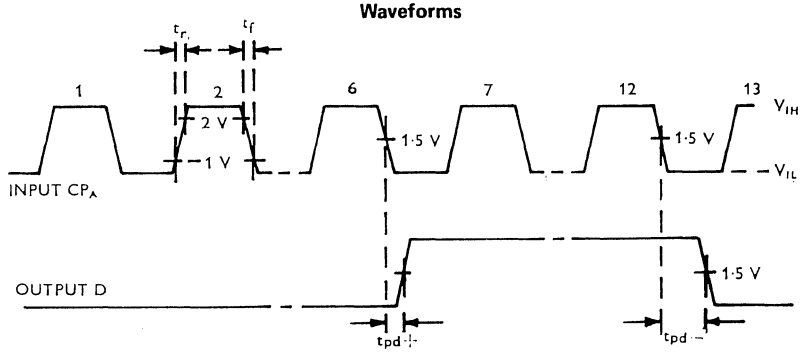
Switching load circuit



CP_A INPUT PULSE CHARACTERISTICS

Amplitude = 3.5 V
t_r = 10 ns
t_f = 4 ns
P.R.F. = 1 MHz
duty cycle = 50%

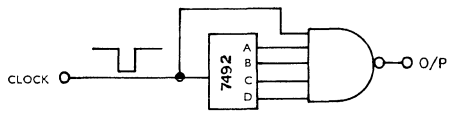
Waveforms



APPLICATION NOTES

1. Ripple Delay

In asynchronous counters ripple delay always occurs. It is defined as the time interval between the clock pulse edge at the first stage and the instant a succeeding stage changes state. When decoding the outputs of the counter, false outputs can occur at the transition from an odd count state to an even count state. The false output will always represent a lower count than the true state. When using the counter with decoding the possibility of such false outputs can be prevented by inhibiting the decode gate with the clock signal.

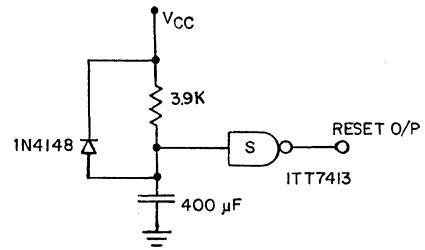


2. Count Range, Less Than Twelve

Typically when feeding back output signals from the counter by direct connection from outputs to reset inputs $R_{0(1)}$ and $R_{0(2)}$ the counter will reset and start a new count sequence. Feedback can be obtained in this manner from all count states except 9 and 11 which will require a three input NAND gate and an inverter as the feedback loop. Under extreme worst case conditions of direct feedback it is possible that not all stages will reset, correct resetting can be ensured by using external gating for all count states. When resetting in either manner the reset count will be on the outputs for the time it takes for resetting to occur.

3. Illegal Start-up States

On application of supply voltage each flip-flop in a counter may start-up in either state. It is, therefore, possible for the counter to assume any one of the 16 possible states. With any type of counter, which uses internal gating to restrict the count sequence, the 7492 being no exception, the illegal states (12 to 15), could be obtained. If this is the case, application of clock pulses will enable the counter to count off this state, after which normal operation will follow. If, however, it is essential that such conditions are avoided arrangements should be made to provide a reset signal during initial applications of supply voltage. A circuit which will generally prove satisfactory is shown below.



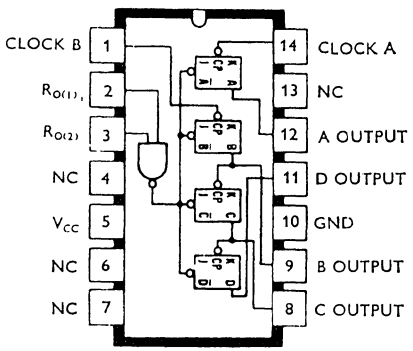
For further details see ITT7413 data sheet.

Divide by 2 ●Divide by 4 ●Divide by 8 ●Divide by 16

TYPICAL CHARACTERISTICS

Propagation delay (ripple delay) . . . . . 75 ns
Maximum clock frequency. . . . . .18 MHz
Power dissipation (over full count sequence) . . . . . 120 mW
Input loading factor:
$R_{0(1)}$, $R_{0(2)}$ . . . . . 1 unit load
Clock A and B inputs. . . . . 2 unit loads
Fan-out from each output (Note 1) . . 10 unit loads
Clock pulse width . . . . . 50 ns min.
Reset pulse width . . . . . 50 ns min.

Pin configuration (top view)



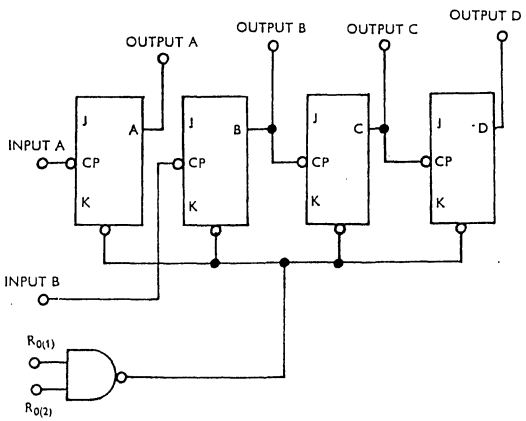
Note 1
For a divide by 16 count, with pin 12, O/P A, connected to pin 1, I/P B, the full fan-out of 10 is still permissible from O/P A.

DESCRIPTION

The 4 bit binary counter consists of four master slave flip-flops. Flip-flop 'A' provides a divide-by-2 function. The remaining three flip-flops are internally connected by provide a divide-by-8 counter. Counting occurs on the negative edge of the clock input. Inputs $R_{0(1)}$ and $R_{0(2)}$ are gated to provide reset to zero. All inputs have input clamping diodes and outputs are standard 74 series configurations.
Because O/P 'A' is not internally connected to the succeeding flip-flops, there are two count modes available:

1. Divide-by-16 mode is obtained by externally connecting A output (Pin 12) to clock B input (pin 1). Outputs A, B, C, and D give simultaneous division by 2, 4, 8 and 16 respectively.
2. The device may be used as separate divide-by-2 and divide-by-8 counters but with common reset lines.

Logic Diagram



Truth Table

COUNT SEQUENCE

Count	Outputs				Count	Outputs			
	D	C	B	A		D	C	B	A
0	0	0	0	0	8	1	0	0	0
1	0	0	0	1	9	1	0	0	1
2	0	0	1	0	10	1	0	1	0
3	0	0	1	1	11	1	0	1	1
4	0	1	0	0	12	1	1	0	0
5	0	1	0	1	13	1	1	0	1
6	0	1	1	0	14	1	1	1	0
7	0	1	1	1	15	1	1	1	1

RESET/COUNT

To Count:
Either $R_{0(1)}$ or $R_{0(2)}$ or both reset inputs must be at logical '0'.

To Reset:
Both $R_{0(1)}$ and $R_{0(2)}$ must be at logical '1'.

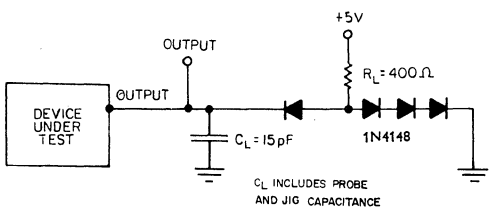
PARAMETER	LIMIT				CONDITIONS	
	Min.	Typ. at 25°C	Max.	Units	V_{CC}	
I_{CCH}						All outputs at 0, R_0 at 0
7493		31	51	mA	Max.	V_{IN} = 50V
5493		31	44	mA		
I_{CCL}						Count of 15
7493		16	25	mA	Max.	V_{IN} - 5.0V
5493		16	22	mA		

Information on the absolute maximum ratings and the other D.C. characteristics of this device (which are common to other integrated circuits in this series) is stated in the general information section.

SWITCHING CHARACTERISTICS V_{CC}=5.0V, T_{AMB}=25°C

PARAMETER	LIMIT				CONDITIONS
	Min.	Typ.	Max.	Unit	
f_{max}	10	18		MHz	Load circuit on each output
t_{pd+} From input 'A' to output 'D'		75	135	ns	Load circuit on each output
t_{pd-} From input 'A' to output 'D'		75	135	ns	Load circuit on each output

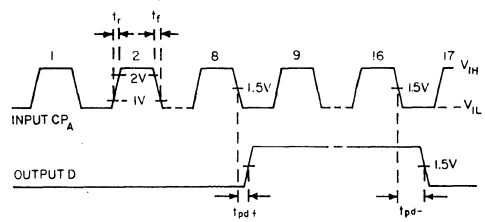
Switching load circuit



Waveforms

CP_A INPUT PULSE CHARACTERISTICS

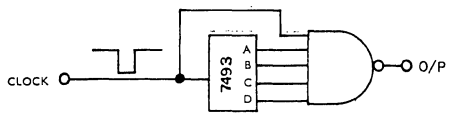
Amplitude = 3.5 V
t_r = 10 ns
t_f = 4 ns
P.R.F. = 1 MHz
duty cycle = 50%



APPLICATION NOTES

1. Ripple Delay

In asynchronous counters ripple delay always occurs. It is defined as the time interval between the clock pulse edge at the first stage and the instant a succeeding stage changes state. When decoding the outputs of the counter false outputs can occur at the transition from an odd state to an even count state. The false output will always represent a lower count than the true state. When using the counter with decoding the possibility of such false outputs can be prevented by inhibiting the decode gate with the clock signal.

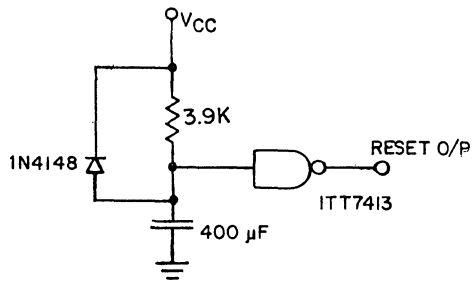


2. Count Range, Less Than Sixteen

Typically when feeding back output signals from the counter by direct connection from outputs to reset inputs $R_{0(1)}$ and $R_{0(2)}$ the counters will reset and start a new count sequence. Feedback can be obtained in this manner from all count states which have codes with only one or two logic '1' states. Others will require a three or four input NAND gate and an inverter as the feedback loop. Under extreme worst case conditions of direct feedback it is possible that not all stages will reset, correct resetting can be ensured by using external gating for all count states. When resetting in either manner the reset count state will be on the outputs for the time it takes for resetting to occur.

3. Illegal Start Up States

On application of supply voltage each flip-flop in a counter may start up in either state. It is, therefore, possible for the counter to assume any one of the 16 possible states. If, however, it is essential that start up conditions give zero count, arrangements should be made to provide a reset signal during initial application of supply voltage. A circuit which will generally prove satisfactory is shown below.



For further details see ITT7413 data sheet.

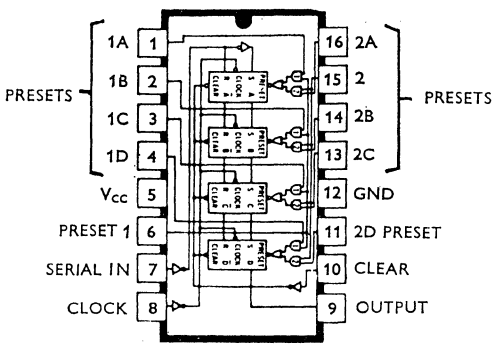
ITT7494
4 BIT SHIFT REGISTER

- **Preset Parallel Input**
- **Parallel or Serial Input**
- **Dual Source Parallel Input with Strobe**
- **Serial Output**
- **Buffered Clear, Clock and Serial Inputs**
- **Dual Source Parallel to Serial Converter**

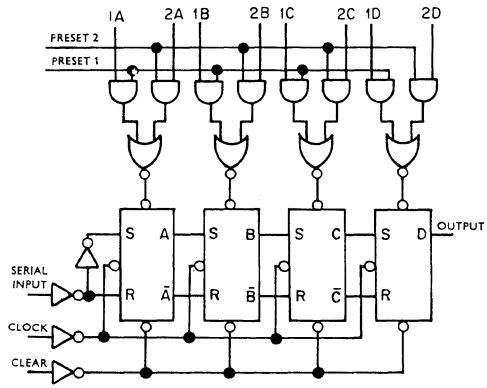
TYPICAL CHARACTERISTICS

Propagation delay . . . . . 25 ns
Power dissipation . . . . . 175 mW
Input loading factor,
all inputs except: preset 1 or 2
(A, B, C, D). . . . . 1 unit load
preset 1 and 2 (common inputs) . . 4 unit loads
Fan-out . . . . . 1 to 10 unit loads
Clock pulse width t_{cp} . . . . . 35 ns, min.
Clear pulse width t_p (clear) . . . . . 30 ns, min.
Preset pulse width t_p (preset) . . . . . 30 ns, min.
Serial input set up time:
t_{sp+} . . . . . 35 ns, min.
t_{sp-} . . . . . 25 ns, min.
Serial input hold time t_h . . . . . 0 ns

Pin configuration (top view)



Logic diagram



DESCRIPTION

The ITT7494 consists of four R-S master slave flip-flops connected to form a four bit shift register. The clock, clear and serial inputs are buffered by four inverters. The two sets of preset inputs 1A to 1D and 2A to 2D are selected by a logical '1' voltage applied to preset 1 and preset 2 inputs respectively, using four AND-OR-INVERT gates. A logical '1' voltage on the preset inputs (1A to 1D or 2A to 2D) will set the flip-flops to a logical '1' state, when selected by the preset 1 or 2 inputs, irrespective of the logic state of the clock, clear and serial inputs. Application of a logical '1' voltage to the clear input will set all four stages to logical '0' state irrespective of the logic state of the clock and serial inputs. Serial shift occurs on the positive edge of the clock, the preset 1 and 2 and clear inputs must all be at logical '0' voltage and the serial input data must be present prior to the clock edge. All inputs have clamping diodes and outputs are standard 74 series configuration.
The registers may be cascaded to provide any length register or any number of bits parallel to serial converter.

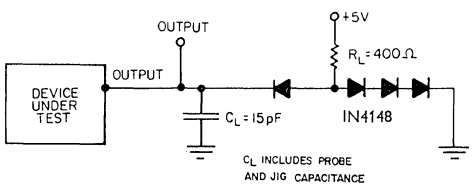
PARAMETER	LIMIT				CONDITIONS	
	Min.	Typ. at 25°C	Max.	Unit	V_{CC}	
I_{CCH}						
7494		35	58	mA	Max.	Preset and clear inputs at logical '0'
5494		35	50	mA		clock and serial inputs at logical '1'
I_{CCL}						
7494		30	50	mA	Max.	All inputs at logical '0'
5494		30	43	mA		

SWITCHING CHARACTERISTICS V_{CC}=5.0V, T_{AMB}=25°C

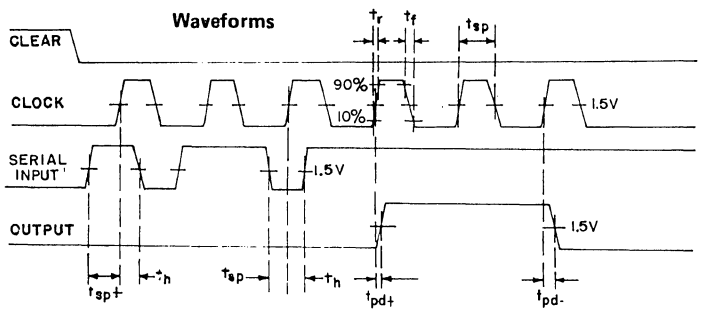
PARAMETER	LIMIT				CONDITIONS
	Min.	Typ.	Max.	Unit	
f_{max}	10			MHz	Use switching load circuit
t_{pd+} propagation delay to logical '1':					
from clock		25	40	ns	Use switching load circuit
from preset			35	ns	
t_{pd-} propagation delay to logical '0':					
from clock		25	40	ns	Use switching load circuit
from preset			40	ns	

Information on the absolute maximum ratings and the other D.C. characteristics of this device (which are common to other integrated circuits in this series) is stated in the general information section.

Switching load circuit



Waveforms



PARALLEL INPUT OPERATION

There are basically two forms of parallel input shift registers. The preset parallel input type such as the ITT7494 and ITT7496, and the clocked parallel input type such as the ITT7495.

The inputs of the preset types are taken to the flip-flop preset inputs via appropriate gating. The application of a logical '1' voltage to the input will set the flip-flop to logical '1' state, but the application of a logical '0' voltage will then have no effect. To set flip-flop to logical '0' state the clear input must be used.

The inputs of the clocked type are taken to the R S flip-flop inputs via appropriate gating. The application of a logical '1' voltage at the input prior to clocking will set the flip-flop to a logical '1' state similarly the application of a logical '0' voltage at the input will set the flip-flop to a logical '0' state.

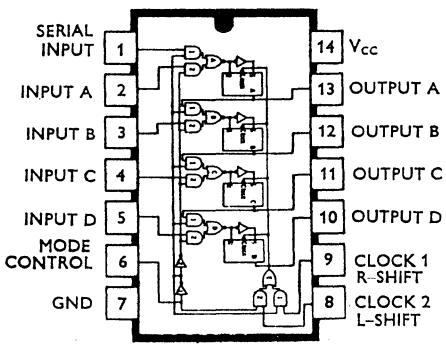
The clocked parallel input register is, therefore, most suitable for applications where the parallel data is applied for a predetermined time as is the case for the accumulator of a multiplier. The preset parallel input register is more suitable for applications where the input data arrives randomly or is present for a very short time as can be the case in some types of analogue to digital conversion systems.

- **Clocked Parallel Entry**
- **Parallel to Serial Converter**
- **Serial to Parallel Converter**
- **Mode Control with Single cr Dual Clock**

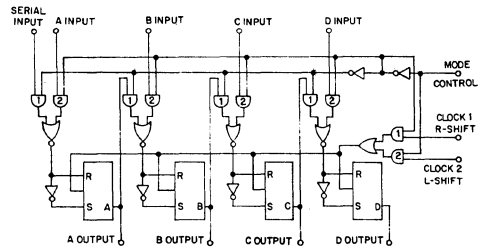
TYPICAL CHARACTERISTICS

Maximum clock frequency . . . . . 31 MHz
Propagation delay . . . . . 25 ns
Power dissipation . . . . . 200 mW
Input loading factor:
(not mode control) . . . . . 1 unit load
(mode control) . . . . . 2 unit loads
Fan-out from each output . . . . . 10 unit loads
Clock pulse width t_{cp}:
74 series . . . . . > 15 ns (nominal 10 ns)
54 series . . . . . > 20 ns (nominal 10 ns)
Set up time at data
inputs t_{sp} . . . . . > 20 ns (nominal 10 ns)
Hold time at data inputs t_h . .0 ns (nominal—10 ns)
Set up time at mode control
with respect to Clock 1
t_{sp+} . . . . . > 10 ns
t_{sp-} . . . . . > 20 ns
Set up time at mode control with respect
to Clock 2
t_{sp+} . . . . . > 20 ns
t_{sp-} . . . . . > 10 ns

Pin configuration
(top view)



Logic diagram



DESCRIPTION

The shift register consists of four master slave flip-flops. The outputs of these flip-flops, the R.S. inputs, the parallel inputs, the mode control and the serial input are all inter-connected by four AND-OR-INVERT gates and six INVERTERS. The two clock inputs are selected by the mode control via an AND-OR gate. When the mode control is at logical '0' it enables AND gates 1 and inhibits AND gate 2, thus permitting clock 1 on a negative edge to produce right shift. When mode control is at logical '1', AND gates 2 are enabled and AND gates 1 are inhibited, permitting clock 2 on a negative edge to produce parallel shift or with external connections*, left shift. If single source clocking is required the two clock inputs can be commoned. Information should be present at the R.S. inputs of the flip-flop before clocking occurs.

*For left shift make the following connections: Output D to Input C, Output C to Input B, Output B to Input A, and D input becomes the serial input.

PARA-METER	LIMITS				CONDI-TIONS
	Min.	Typ.at 25°C	Max.	Units	V_{CC}
I_{CC}					
7495		40	66	mA	Max.
5495		40	58	mA	

SWITCHING CHARACTERISTICS V_{CC}=5.0V, T_{AMB}=25°C

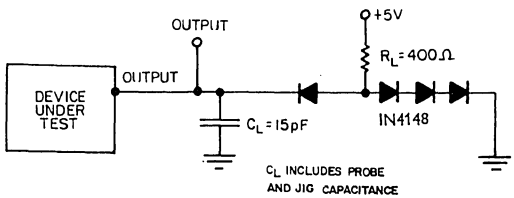
PARAMETER	LIMIT				CONDITIONS
	Min.	Typ. at 25°C	Max.	Unit	
f_{max}	20	31		MHz	Switching load circuit on each output
t_{pd-} propagation delay to logical '1' from either clock		26	35	ns	Switching load circuit on each output
t_{pd-} propagation delay to logical '0' from either clock		24	35	ns	Switching load circuit on each output

Information on the absolute maximum ratings and the other D.C. characteristics of this device (which are common to other integrated circuits in this series) is stated in the general information section.

Clock Pulse Characteristics

t_r = 10 ns; t_f = 4 ns; R.F = 1 MHz; Z_o = 50 Ω; Amplitude - 3.5 V

Switching load circuit

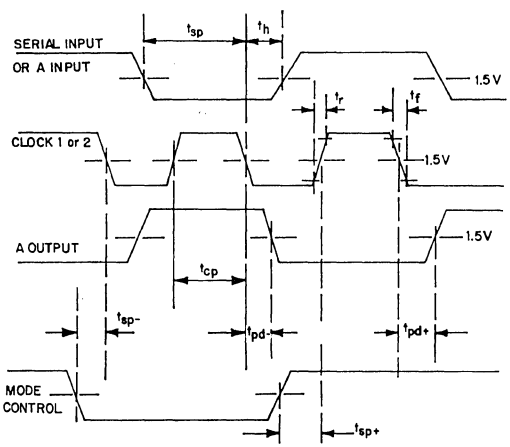


APPLICATION NOTE

Parallel Input Operation

There are basically two forms of parallel input shift registers. The preset parallel input type such as the ITT7494 and ITT7496 and the clocked parallel input type such as the ITT7495.
The inputs of the preset type are connected to the flip-flop preset inputs via appropriate gating. The application of a logical '1' voltage to the input sets the flip-flop to logical '1' state, but the application of a logical '0' voltage then has no effect. To set flip-flops to logical '0' state the clear input must be used.
The inputs of the clocked type are connected to the R.S. flip-flop inputs via appropriate gating. The application of a logical '1' voltage at the input prior to clocking sets the flip-flops to a logical '1' state similarly the application of a logical '0' voltage at the input sets the flip-flops to a logical '0' state.
The clocked parallel input register is, therefore, most suitable for applications where the parallel data is applied for a predetermined time as is the case for the accumulator of a multiplier. The preset parallel input register is more suitable for applications where the input data arrives randomly or is present for a very short time as can be the case in some types of analogue to digital conversion systems.

Waveforms



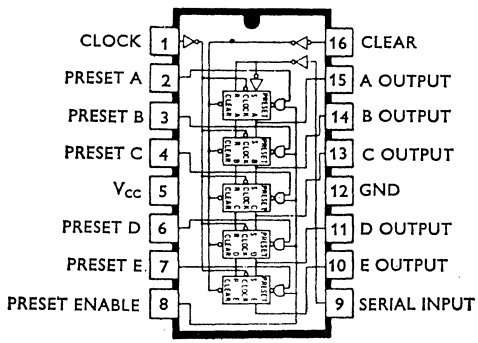
ITT7496
5 BIT SHIFT REGISTER

- **Preset Parallel Input**
- **Parallel or Serial Input**
- **Parallel and Serial Output**
- **Buffered Clear, Clock and Serial Inputs**
- **Serial to Parallel/Parallel to Serial Converter**

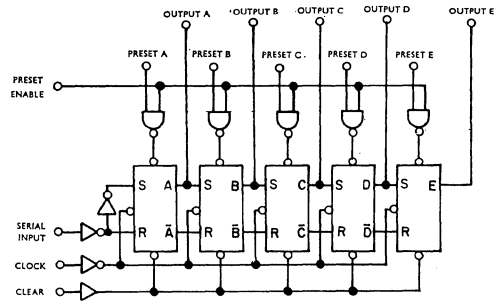
TYPICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

Propagation delay . . . . . 25 ns
Power dissipation . . . . . 215 mW
Input loading factor:
All inputs except preset . . . . . 1 unit load
Preset (pin 8) . . . . . 5 unit loads
Fan-out . . . . . 1 to 10 unit loads
Clock pulse width t_{cp} . . . . . 35 ns, min.
Clear pulse width t_p (clear) . . . . . 30 ns, min.
Preset pulse width t_p (preset) . . . . . 30 ns, min.
Serial input set time t_{sp} . . . . . 30 ns, min.
Serial input hold time t_h . . . . . 0 ns

Pin configuration (top view)



Logic Diagram



DESCRIPTION

The ITT7496 consists of five R-S master slave flip-flops connected to form a five bit shift register. The clock, clear and serial inputs are buffered by four inverters. The preset inputs A to E are connected to the flip-flop preset inputs via five two-input NAND gates. The second input of each gate is connected to the common preset input, which when at logical '1' enables all preset inputs. A logical '1' on these inputs sets the flip-flops to the logical '1' state. A logical '1' on the clear input sets all flip-flops to the logical '0' state simultaneously. Right shift in the register occurs on the positive edge of the clock pulse. The serial input data must be present prior to the clock edge. All inputs have clamping diodes and outputs are standard 74 series configuration.
The registers may be cascaded to provide any length of register.

PARAMETER	LIMIT				CONDITIONS
	Min.	Typ. at 25°C	Max.	Units	V_{CC}
I_{CCH}					Clock and clear at logical '1'
7496		43	79	mA	Max. Serial and preset input at logical '0'
5496		43	68	mA	
I_{CCL}					
7496		42	78	mA	Max. All at 0
5496		42	67	mA	

Information on the absolute maximum ratings and the other D.C. characteristics of this device (which are common to other integrated circuits in this series) is stated in the general information section.

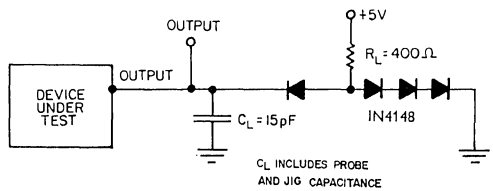
SWITCHING CHARACTERISTICS V_{CC}=5.0V, T_{AMB}=25°C

PARAMETER	LIMIT				CONDITIONS
	Min.	Typ.	Max.	Unit	
f_{max}	10			MHz	Use switching load circuit on each output
t_{pd+}					
Clock to output		25	40	ns	Use switching load circuit
Preset to output			35	ns	on each output
t_{pd-}					
Clock to output		25	40	ns	Use switching load circuit
Clear to output			55	ns	on each output

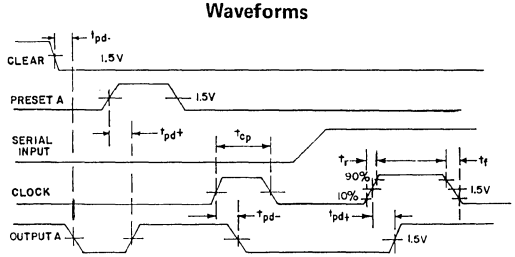
Parallel Input Operation

There are basically two forms of parallel input shift registers. The preset parallel input type such as the ITT7494 and ITT7496 and the clocked parallel input type such as the ITT7495.
The inputs of the preset type are connected to the flip-flop preset inputs via appropriate gating. The application of a logical '1' voltage to the input sets the flip-flop to logical '1' state but the application of a logical '0' voltage then has no effect. To set flip-flops to logical '0' state the clear input must be used.
The inputs of the clocked type are connected to the R-S flip-flop inputs via appropriate gating. The application of a logical '1' voltage at the input prior to clocking sets the flip-flops to a logical '1' state. Similarly the application of a logical '0' voltage at the input sets the flip-flops to a logical '0' state. Hence the clocked parallel register is most suitable for applications where the parallel data is applied for a predetermined time as is the case for the accumulator of a multiplier. The preset parallel input register is more suitable for applications where the input data arrives randomly or is present for a very short time as can be the case in some types of analogue to digital conversion systems.

Switching load circuit



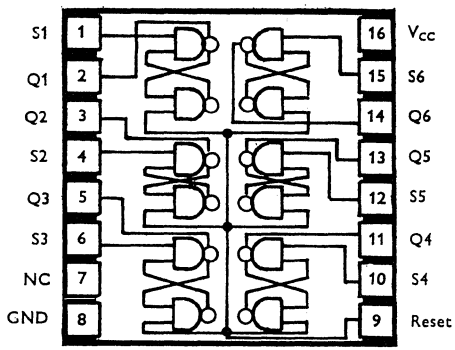
Waveforms



TYPICAL CHARACTERISTICS

Power dissipation . . . . . 150 mW
Input loading factor:
Set . . . . . 1 unit load
Reset . . . . . 5 unit loads
Maximum fan-out . . 20 unit loads (high logic level)
10 unit loads (low logic level)
Mean set time . . . . . 14 ns

Pin configuration
(top view)



DESCRIPTION

The ITT74118 consists of six cross coupled NAND gates each forming a simple bistable circuit. A reset line is common to all six latches. Information is stored within a latch when both the set line and the common reset line are held at logical '1'. The state of each bistable can be changed by taking either the set or reset to logical '0' as shown in the truth table.

Truth Table

S	Reset	Q
0	X	1
1	0	0
1	1	Store

1. X Indicates input may be logical '1' or '0'.
2. Reset is common to all latches.

D.C. CHARACTERISTICS

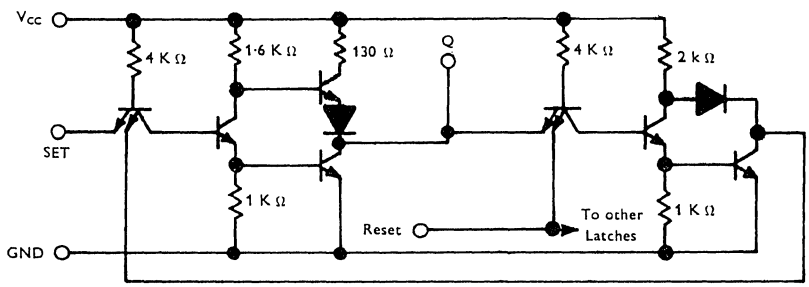
PARAMETER	LIMITS				CONDITIONS
	Min.	Typ. at 25°C	Max.	Units	V_{CC}
I_{CC} supply current		30	60	mA	50% duty cycle

Information on the absolute maximum ratings and the other D.C. characteristics of this device (which are common to other integrated circuits in this series) is stated in the general information section.

SWITCHING CHARACTERISTICS V_{CC}=5V, T_{AMB}=25°C

PROPAGATION DELAY TIME	LIMIT				CONDITIONS
	Min.	Typ.	Max.	Unit	
t_{pd+} to logical '1' level from set		18	29	ns	Fan out = 10 Standard load circuit
t_{pd-} to logical '0' level from set		10	17	ns	C_L - 15 pF R_L = 400 Ω
t_{pd-} to logical '0' level from reset		18	29	ns	

Circuit diagram



ITT74121

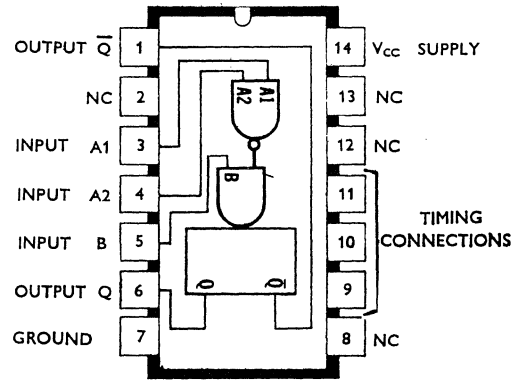
MONOSTABLE MULTIVIBRATOR

Pulse Width 30 ns to 40 s • Schmitt Trigger Input

TYPICAL CHARACTERISTICS

Propagation delay	45 ns
Power dissipation (50% duty cycle)	90 mW
Input loading factor:	
Inputs A_1 and A_2	1 unit load
Input B	2 unit loads
Maximum fan-out	10 unit loads
B input transition time	1 V/s max.
A_1, A_2 input transition time	1 V/μs max.
Input pulse width	50 ns, min.
External timing resistance R_t	1.4 K Ω min.
74 series	40 K Ω max.
54 series	30 K Ω max.
Timing capacitor C_T	1,000 μF max.
Duty cycle:	
R_T = 2 K Ω	67%
R_T = max. value	90%
Output pulse width	0.695 $C_T R_T$

Pin Configuration (top view)



DESCRIPTION

Input Pulse Requirements

A1 and A2 are negative edge trigger inputs and will trigger the monostable when either or both go low with B high. B is a positive edge Schmitt trigger input for slow edges or level detection and will trigger the monostable when B goes high with A1 or A2 low. Once fired further transitions on the inputs will have no effect on the outputs until the time period is completed. The time period may be varied with components as follows:

(a) External timing capacitor may be connected between pin 10 (positive) and pin 11. With no external capacitance an output pulse width of typically 30 ns is obtained.
(b) To use the internal timing resistor (normally 2 K Ω) connect pin 9 to pin 14.
(c) To obtain variable pulse width connect external variable resistor between pins 9 and 14.
(d) For accurate repeatable pulse widths connect an external resistor between pin 11 and pin 14 (value between 1.4 K Ω and maximum value). Leave pin 9 open-circuit.

D.C. CHARACTERISTICS

PARAMETER	LIMIT				CONDITIONS	
	Min.	Typ. at 25°C	Max.	Unit	V_{CC}	
V_{T+} positive edge threshold voltage						
At input A		1.4	2	V	Min.	Note 1
At input B		1.55	2	V	Min.	
V_{T-} negative edge threshold voltage						
At input A	0.8	1.4		V	Min.	Note 1
At input B	0.8	1.35		V	Min.	
I_{CC} supply current						
Quiescent state		13	25	mA	Max.	Note 3
Fired state		23	40	mA	Max.	

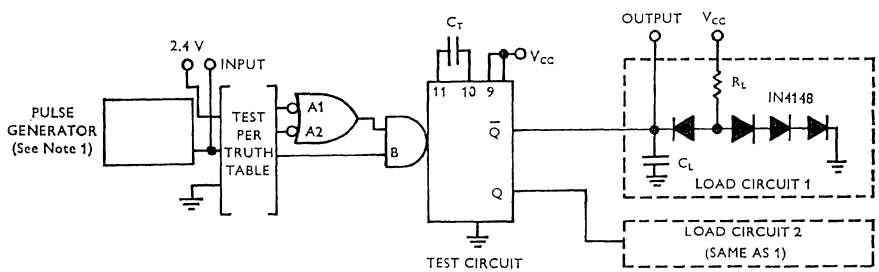
Notes

1. Use external C = 1,000 pF, R = 10 K Ω.
2. To measure I_{SC} on Q ground all inputs Pin 11 and Pin 10. Pin 10 must be grounded last. To measure I_{SC} on $\overline{Q}$ leave Pin 10 and 11 open.
3. Use external C = 1,000 pF; Ground A_1, A_2; Pulse B according to truth table.

SWITCHING CHARACTERISTICS V_{CC}=5.0V, T_{AMB}=25°C

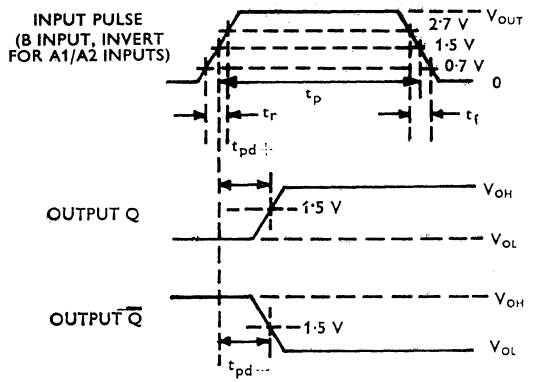
PARAMETER	LIMIT				CONDITIONS
	Min.	Typ.	Max.	Unit	
t_{pd+}					
From A_1 or A_2 to Q	25	45	70	ns	Use test circuit (1)
From B to Q	15	35	55	ns	
t_{pd-}					
From A_1 or A_2 to $\overline{Q}$	30	50	80	ns	Use test circuit (1)
From B to $\overline{Q}$	20	40	65	ns	
t_{po} output pulse width					
R_T = internal					
C_T = 0	20	30	50	ns	Use test circuit (2)
R_T = internal					
C_T = 80 pF	70	110	150	ns	
R_T = 10 K Ω					
C_T = 100 pF	600	700	800	ns	
R_T = 10 K C_T = 1 μF	6	7	8	ms	
t_{min} min. width trigger pulse B input		30	50	ns	Use test circuit (2)

Test circuit (1)

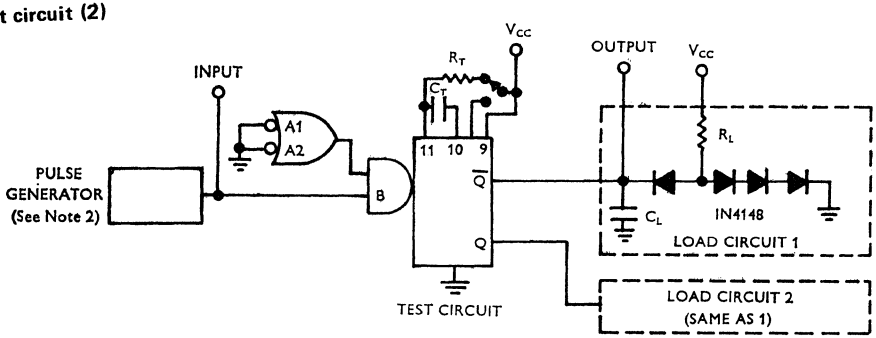


Note 1:
The pulse generator has the following characteristics:
V_{OUT} = 3.5V, t_f = 5 ns, t_r = 10 ns, t_p = 50 ns,
PRF = 1 MHz, and Z_{OUT} = 50 Ω.

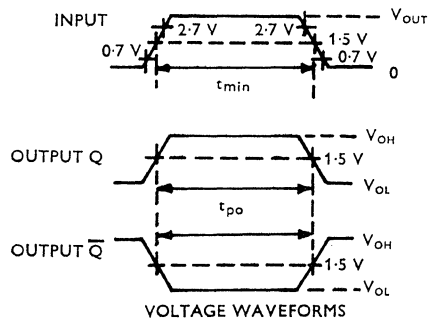
Waveforms



Test circuit (2)



Waveforms



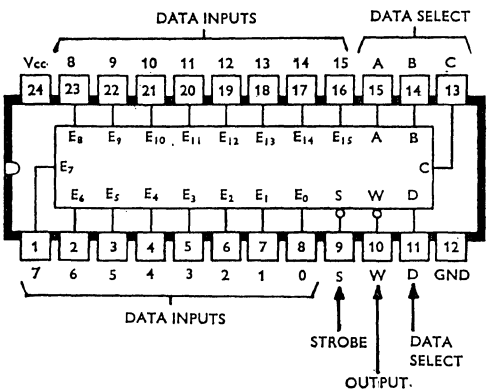
Note 2:
The pulse generator has the following characteristics:
V_{OUT} = 3.5 V, t_f = 5 ns, t_r = 10 ns, $t_p \geq 50$ ns,
PRF = 1 MHz and $Z_{OUT} \approx 50\ \Omega$.

TYPICAL CHARACTERISTICS

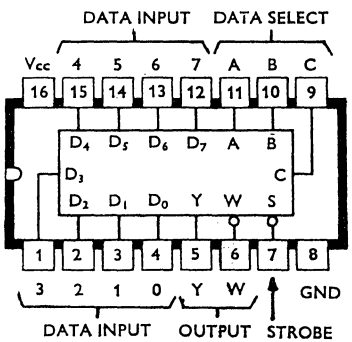
Propagation delay from
data inputs to the output . . . . . 10 ns
Power dissipation:
ITT74150 . . . . . 200 mW
ITT74151 . . . . . 145 mW
Input loading factor . . . . . 1 unit load
Maximum fan-out . . 20 unit loads (high logic level)
10 unit loads (low logic level)

Pin configurations
(top views)

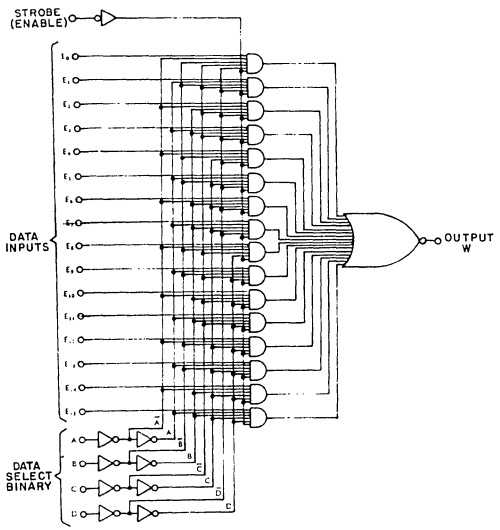
ITT74150



ITT74151



Logic diagram, ITT74150



DESCRIPTION

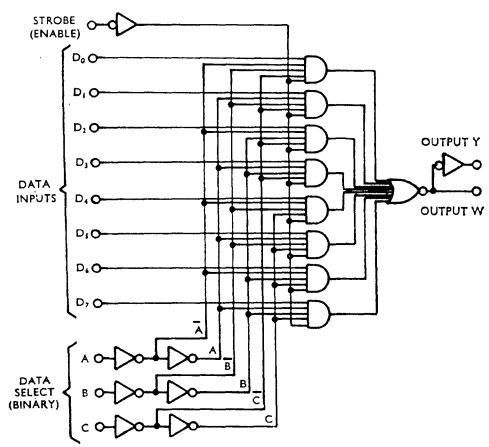
Both circuits convert parallel binary information to a serial form by means of a select signal. The ITT74150 can select one line of sixteen and route this information to the output in the inverted form. Each line is selected by a binary coded number presented to four data select lines. All the information on the data inputs can be inhibited from the output by a common strobe line when this is at a logical '1'. The output circuit is a standard TTL totem pole configuration but having twice the fan out capability in the logical '1' state. The ITT74151 is a one line of eight selector. It is identical in operation to the ITT74150 (apart from handling less bits) but has an additional output which provides non inversion of the input data.

Truth Table, ITT74150

Inputs																				Output
D	C	B	A	Strobe	E_0	E_1	E_2	E_3	E_4	E_5	E_6	E_7	E_8	E_9	E_{10}	E_{11}	E_{12}	E_{13}	E_{14}	E_{15}	W
X	X	X	X	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1
0	0	0	0	0	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1
0	0	0	0	0	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0
0	0	0	1	0	X	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1
0	0	0	1	0	X	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0
0	0	1	0	0	X	X	0	X	X	X	X	X	X	X	X	X	X	X	X	X	1
0	0	1	0	0	X	X	1	X	X	X	X	X	X	X	X	X	X	X	X	X	0
0	0	1	1	0	X	X	X	0	X	X	X	X	X	X	X	X	X	X	X	X	1
0	0	1	1	0	X	X	X	1	X	X	X	X	X	X	X	X	X	X	X	X	0
0	1	0	0	0	X	X	X	X	0	X	X	X	X	X	X	X	X	X	X	X	1
0	1	0	0	0	X	X	X	X	1	X	X	X	X	X	X	X	X	X	X	X	0
0	1	0	1	0	X	X	X	X	X	0	X	X	X	X	X	X	X	X	X	X	1
0	1	0	1	0	X	X	X	X	X	1	X	X	X	X	X	X	X	X	X	X	0
0	1	1	0	0	X	X	X	X	X	X	0	X	X	X	X	X	X	X	X	X	1
0	1	1	0	0	X	X	X	X	X	X	1	X	X	X	X	X	X	X	X	X	0
0	1	1	1	0	X	X	X	X	X	X	X	0	X	X	X	X	X	X	X	X	1
0	1	1	1	0	X	X	X	X	X	X	X	1	X	X	X	X	X	X	X	X	0
1	0	0	0	0	X	X	X	X	X	X	X	X	0	X	X	X	X	X	X	X	1
1	0	0	0	0	X	X	X	X	X	X	X	X	1	X	X	X	X	X	X	X	0
1	0	0	1	0	X	X	X	X	X	X	X	X	X	0	X	X	X	X	X	X	1
1	0	0	1	0	X	X	X	X	X	X	X	X	X	1	X	X	X	X	X	X	0
1	0	1	0	0	X	X	X	X	X	X	X	X	X	X	0	X	X	X	X	X	1
1	0	1	0	0	X	X	X	X	X	X	X	X	X	X	1	X	X	X	X	X	0
1	0	1	1	0	X	X	X	X	X	X	X	X	X	X	X	0	X	X	X	X	1
1	0	1	1	0	X	X	X	X	X	X	X	X	X	X	X	1	X	X	X	X	0
1	1	0	0	0	X	X	X	X	X	X	X	X	X	X	X	X	0	X	X	X	1
1	1	0	0	0	X	X	X	X	X	X	X	X	X	X	X	X	1	X	X	X	0
1	1	0	1	0	X	X	X	X	X	X	X	X	X	X	X	X	X	0	X	X	1
1	1	0	1	0	X	X	X	X	X	X	X	X	X	X	X	X	X	1	X	X	0
1	1	1	0	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0	X	1
1	1	1	0	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1	X	0
1	1	1	1	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0	1
1	1	1	1	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1	0

When used to indicate an input condition, X = Logical '1' or Logical '0'

Logic diagram, ITT74151



Truth Table, ITT74151

Inputs												Outputs	
C	B	A	Strobe	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	Y	W
X	X	X	1	X	X	X	X	X	X	X	X	0	1
0	0	0	0	0	X	X	X	X	X	X	X	0	1
0	0	0	0	1	X	X	X	X	X	X	X	1	0
0	0	1	0	X	0	X	X	X	X	X	X	0	1
0	0	1	0	X	1	X	X	X	X	X	X	1	0
0	1	0	0	X	X	0	X	X	X	X	X	0	1
0	1	0	0	X	X	1	X	X	X	X	X	1	0
0	1	1	0	X	X	X	0	X	X	X	X	0	1
0	1	1	0	X	X	X	1	X	X	X	X	1	0
1	0	0	0	X	X	X	X	0	X	X	X	0	1
1	0	0	0	X	X	X	X	1	X	X	X	1	0
1	0	1	0	X	X	X	X	X	0	X	X	0	1
1	0	1	0	X	X	X	X	X	1	X	X	1	0
1	1	0	0	X	X	X	X	X	X	0	X	0	1
1	1	0	0	X	X	X	X	X	X	1	X	1	0
1	1	1	0	X	X	X	X	X	X	X	0	0	1
1	1	1	0	X	X	X	X	X	X	X	1	1	0

D.C. CHARACTERISTICS

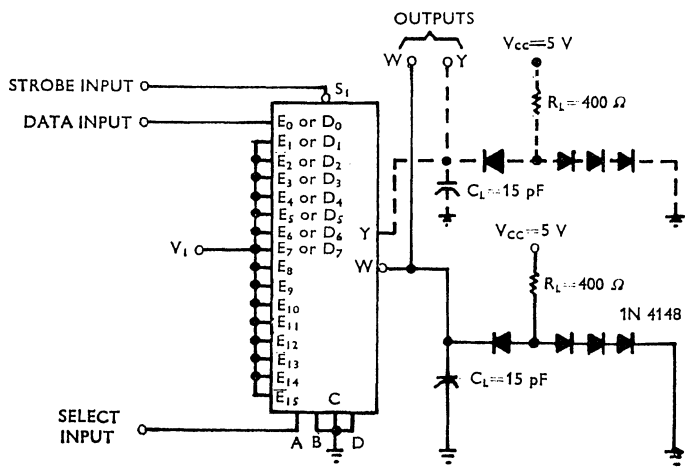
PARAMETER		LIMITS				CONDITIONS	
		Min.	Typ. at 25°C	Max.	Units	V_{CC}	
I_{CCH}	ITT74150		40	68	mA	Max.	V_{strobe} = 0 V, V_{IN} = 4.5 V
	ITT74151		29	48	mA	Max.	(All data inputs logical '1')
I_{CCL}	ITT74150		35	60	mA	Max.	V_{IN} = 0
	ITT74151		22	38	mA	Max.	(All data inputs logical '0')

Information on the absolute maximum ratings and the other D.C. characteristics of these devices (which are common to other integrated circuits in this series) is stated in the general information section.

SWITCHING CHARACTERISTICS V_{CC}=5V, T_{AMB}=25°C, FOR THE ITT74150

PARAMETER			LIMITS				CONDITIONS
	From	To	Min.	Typ.	Max.	Units	
t_{pd+}	A, B, C, or D	W		23	35	ns	V_{CC} = 5V See test circuit
t_{pd-}	A, B, C, or D	W		22	33	ns	V_{CC} = 5V See test circuit
t_{pd+}	Strobe	W		15.5	24	ns	V_{CC} = 5V See test circuit
t_{pd-}	Strobe	W		21	30	ns	V_{CC} = 5V See test circuit
t_{pd+}	E_0 to E_{15}	W		13	20	ns	V_{CC} = 5V See test circuit
t_{pd-}	E_0 to E_{15}	W		8.5	14	ns	V_{CC} = 5V See test circuit

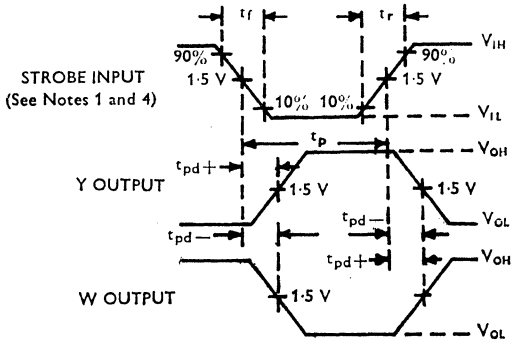
Test circuit for ITT74150 and ITT74151



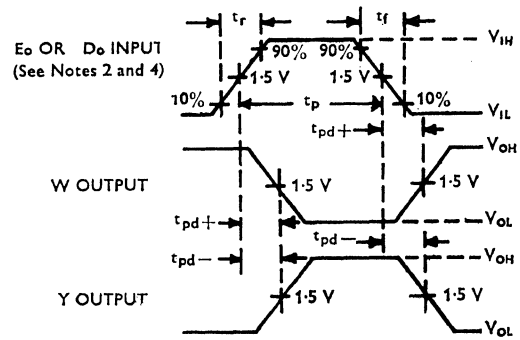
SWITCHING CHARACTERISTICS V_{CC}=5V, T_{AMB}=25°C, FOR THE ITT74151

PARAMETER			LIMITS				CONDITIONS
	From	To	Min.	Typ.	Max.	Units	
t_{pd+}	A, B or C	Y		35	52	ns	V_{CC}=5.0V See test circuit
t_{pd-}	A, B or C	Y		20	30	ns	V_{CC}=5.0V See test circuit
t_{pd+}	Strobe	Y		35	52	ns	V_{CC}=5.0V See test circuit
t_{pd-}	Strobe	Y		19	30	ns	V_{CC}=5.0V See test circuit
t_{pd+}	D_0 to D_7	Y		19	29	ns	V_{CC}=5.0V See test circuit
t_{pd-}	D_0 to D_7	Y		16	24	ns	V_{CC}=5.0V See test circuit

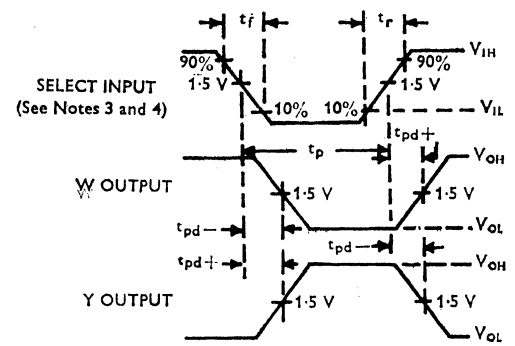
Waveforms for ITT74150 and ITT74151



STROBE-TO-OUTPUT VOLTAGE WAVEFORMS



DATA INPUT-TO-OUTPUT VOLTAGE WAVEFORMS



SELECT INPUT-TO-OUTPUT VOLTAGE WAVEFORMS

Notes:

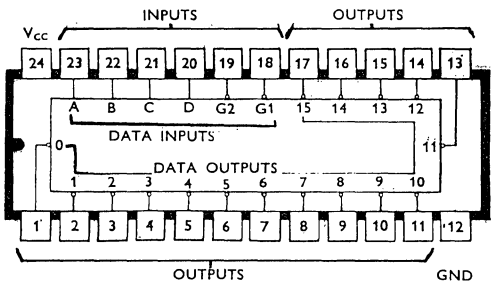
1. When measuring strobe to output times select input is at a logical 0, E_0 or D_0 is at a logical 1, V_1 = 4.5 V.
2. When measuring data input to output times strobe and select inputs are at a logical 0, and V_1 = 4.5 V.
3. When measuring select input to output times strobe input is at a logical 0, data input is at a logical 1, and V_1 = 0.
4. The input pulse has the following characteristics: $V_{in(1)}$ = 3 V, $V_{in(0)}$ = 0 V. t_r = t_f = 10 ns, PRF = 1 MHz, duty cycle = 50%, and generator $Z_{out} \approx 5\ \Omega$
5. C_L includes probe and jig capacitance
6. All diodes are 1N4148

- **4-Line-to-16-Line Decoder**
- **Demultiplexing Capability**

TYPICAL CHARACTERISTICS

Propagation delay (through 3 levels of logic) . . . . . 23 ns
Power dissipation . . . . . 170 mW
Input loading factor . . . . . 1 unit load
Maximum fan-out . . . . . 10 unit loads (low state)
. . . . 20 unit loads (high state)

Pin configurations
(top view)



DESCRIPTION

The ITT74154 can be used as a 4-line-to-16-line decoder or a 1-line-to-16-line demultiplexer.

In use as a decoder, one of the 16 output NAND gates assumes its low state when enabled by the strobe inputs G_1, G_2, and the appropriate binary combination from the four binary-coded inputs A, B, C and D.

The output gates are inhibited by a high strobe input. Therefore to demultiplex, data is entered on a strobe input with the other strobe input low and the four other inputs addressing the appropriate data output line.

The most significant input, D, produces a useful inhibit function when the ITT74154 is used as a 1-line-to-8-line demultiplexer or a 4-line to 8-line decoder.

Be selecting appropriate outputs, any BCD code can be decoded using a ITT74154 element. See truth table and application note for further details.

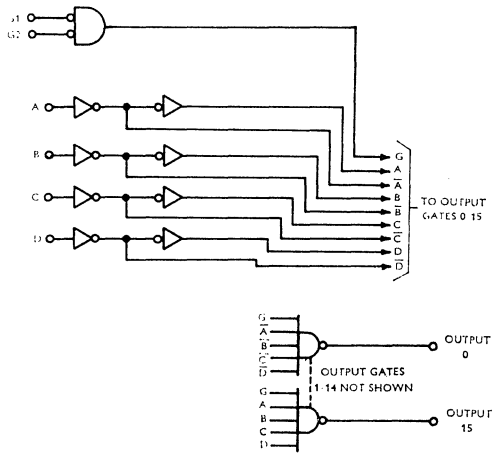
Buffers are incorporated on the inputs to reduce input loading.

Truth Table

INPUTS						OUTPUTS															
G1	G2	D	C	B	A	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	L	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H
L	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H
L	L	H	L	L	L	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H
L	L	H	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H
L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
L	L	H	H	L	L	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H
L	L	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L
L	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	L	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H

H=high, L=low, X=irrelevant

Logic diagram



PARAMETER	LIMIT				CONDITIONS
	Min.	Typ.at 25°C	Max.	Unit	V_{CC}
I_{CC}					
74154		34	56	mA	Max.
54154		34	49	mA	Max.

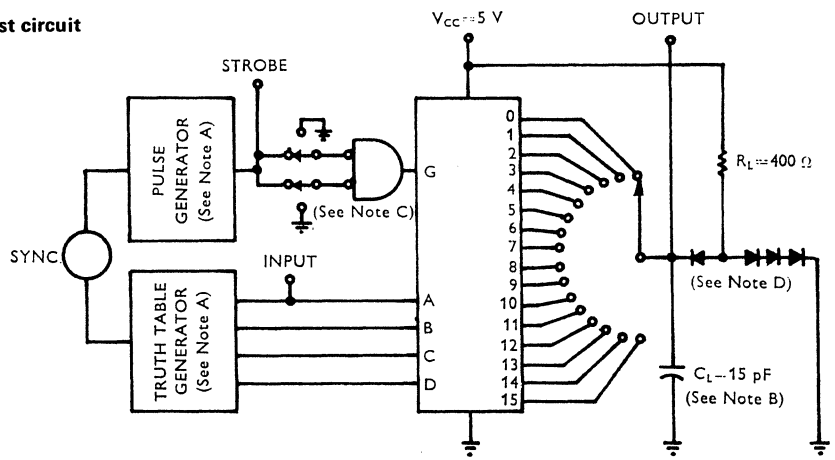
For $-I_{SC}$ maximum limit = 57 mA, for 74154

Information on the absolute maximum ratings and the other D.C. characteristics of this device (which are common to other integrated circuits in this series) is stated in the general information section.

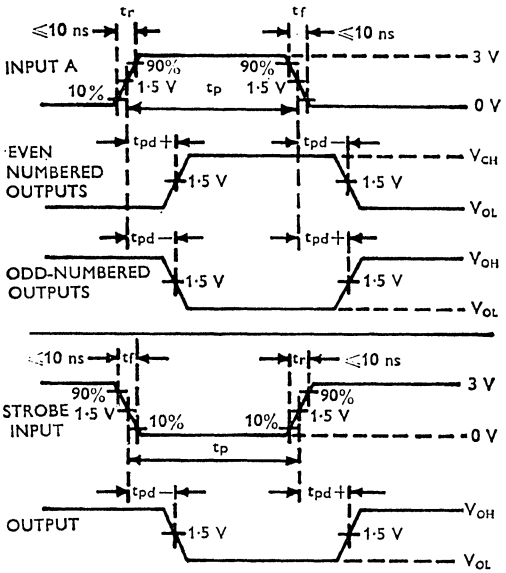
SWITCHING CHARACTERISTICS V_{CC}=5V, T_A=25°C

PARAMETER	LIMIT				CONDITIONS
	Min.	Typ.	Max.	Unit	
t_{pd+} from A, B, C, or D inputs through 3 levels of logic		24	36	ns	SEE TEST CIRCUIT
t_{pd-} from A, B, C, or D inputs through 3 levels of logic		22	33	ns	
t_{pd+} from either strobe input		20	30	ns	
t_{pd-} from either strobe input		18	27	ns	

Test circuit



Waveforms



Notes:

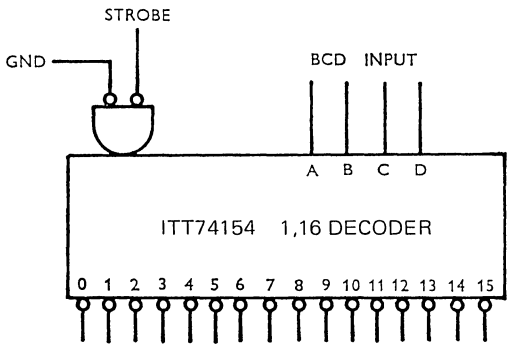
A. The truth table generator and the pulse generator have the following characteristics: P.R.F.=1 MHz, Z_{out}=50 Ω, t_p=100 ns.

B. C_L includes probe and jig capacitance.

C. When measuring select input to output times the strobe inputs are grounded. When measuring strobe input to output times, the untested strobe input is grounded. Select inputs determining output under test through truth table generator.

D. All diodes are 1N4149.

APPLICATION NOTE



Output Selection BCD Code

Decimal Digit	8421	5421	Excess 3	Gray
0	0	0	3	0
1	1	1	4	1
2	2	2	5	3
3	3	3	6	2
4	4	4	7	6
5	5	8	8	7
6	6	9	9	5
7	7	10	10	4
8	8	11	11	12
9	9	12	12	13

DECODE ANY BCD CODE

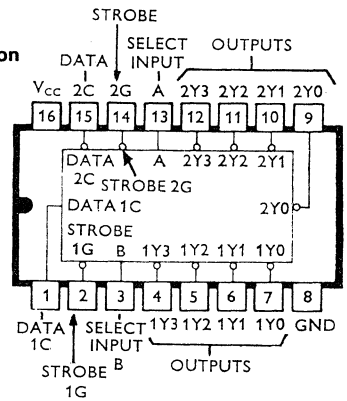
Decode any BCD code using a 74154 element. Any 4 bit BCD code may be decoded by selecting outputs, examples are shown in the table.

TYPICAL CHARACTERISTICS

Power dissipation . . . . . 125 mW
Typical propagation delay . . . . . 16 ns
Input loading factor . . . . . 1 unit load
Maximum fan-out 74155/56 . . . . . 10 unit loads
Maximum fan-out 74155 only . . . . . 20 unit loads (high logic state)

Pin configuration (both devices)

(top view)



DESCRIPTION

Both ITT74155 and ITT74156 have the same logic function. They can either be connected as a 2-line-to-4-line decoder using the select inputs. A and B, or as a 3-line-to-8-line decoder by using inputs A, B, and a common shorted connection 1C to 2C. The outputs only respond to the data select inputs when either the strobe and/or data inputs go from logical '1' to '0'. In which case the appropriate output will change from logical '1' to '0'.

If the data is applied to strobe/data inputs, the select inputs address the data to the appropriate output. Both devices form either a dual 1-line-to-4-line demultiplexer with common address input or a 1-line-to-8-line demultiplexer.

When using this device it should be noticed that the two functional halves of this circuit are logically coupled from the select inputs, but are independent from the strobe or data inputs.

The ITT74155 has totem pole outputs, while the ITT74156 has standard open collector outputs, so that several circuits can be easily 'Wired-ORed' for demultiplexing from more lines.

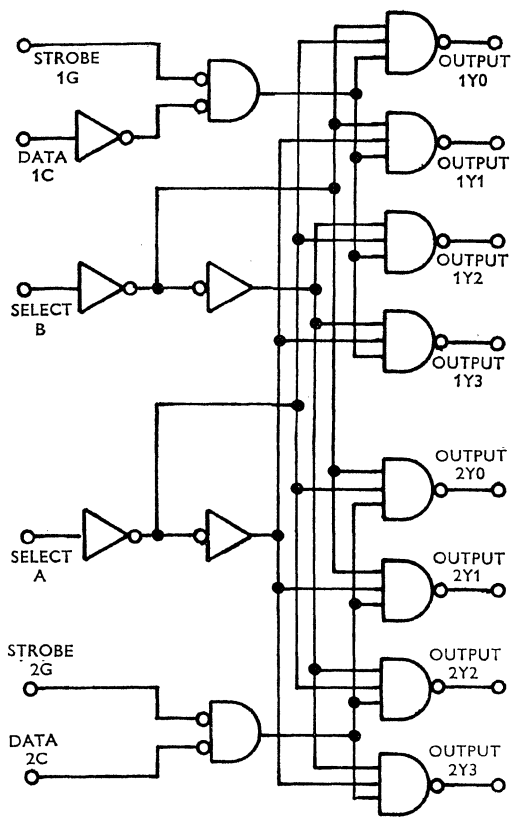
See truth tables for more detailed operation of these devices.

PARAMETER	LIMIT				CONDITIONS
	Min.	Typ.at 25°C	Max.	Unit	V_{CC}
I_{CC}					
74155		25	40	mA	Max.
74156		25	35	mA	Max.

Maximum limit for $-I_{SC}$ parameter is –57 mA for ITT74155. No $-I_{SC}$ parameter for ITT74156.

Information on the absolute maximum ratings and the other D.C. characteristics of these devices (which are common to other integrated circuits in this series) is stated in the general information section.

Logic diagram



SWITCHING CHARACTERISTICS V_{CC}=5V, T_A=25°C

PARAMETER			LIMIT				CONDITIONS
	From input	To output	Min.	Typ. at 25°C	Max.	Unit	
t_{pd+}	A, B, 2C						
74155	1G or	Y		13	20	ns	
74156	2G			15	23	ns	
t_{pd-}	A, B, 2C						
74155	1G or	Y		18	27	ns	
74156	2G			20	30	ns	
t_{pd+}							
74155	A or B	Y		21	32	ns	INPUTS
74156				23	34	ns	AS PER
t_{pd-}							TRUTH
74155	A or B	Y		21	32	ns	TABLE
74156				23	34	ns	
t_{pd+}							
74155	1C	Y		16	24	ns	
74156				18	27	ns	
t_{pd-}							
74155	1C	Y		20	30	ns	
74156				22	33	ns	

Truth Tables

(X = Don't Care, H = Logical 1 State, L = Logical 0 State)

(A) 2-4 Line Decoder or 1-4 Line Demultiplexer

2G = X, 2C = X

INPUTS				OUTPUTS			
Select B	Select A	Strobe 1G	Data 1C	1Y0	1Y1	1Y2	1Y3
X	X	H	X	H	H	H	H
L	L	L	H	L	H	H	H
L	H	L	H	H	L	H	H
H	L	L	H	H	H	L	H
H	H	L	H	H	H	H	L
X	X	X	L	H	H	H	H

1G = X, 1C = X

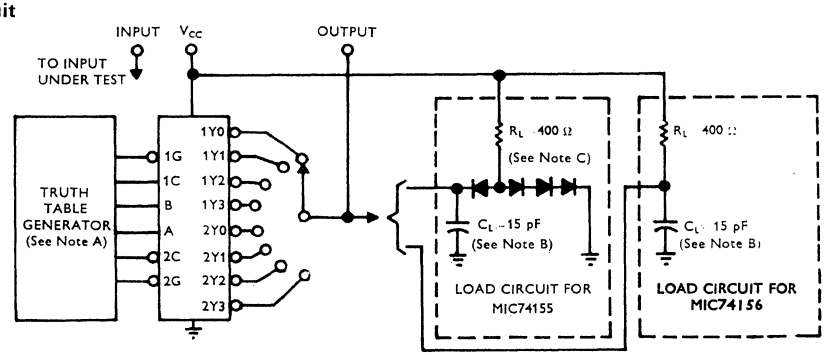
INPUTS				OUTPUTS			
Select B	Select A	Strobe 2G	Data 2C	2Y0	2Y1	2Y2	2Y3
X	X	H	X	H	H	H	H
L	L	L	L	L	H	H	H
L	H	L	L	H	L	H	H
H	L	L	L	H	H	L	H
H	H	L	L	H	H	H	L
X	X	X	H	H	H	H	H

(B) 3-8 Line Decoder or 1-8 Line Demultiplexer

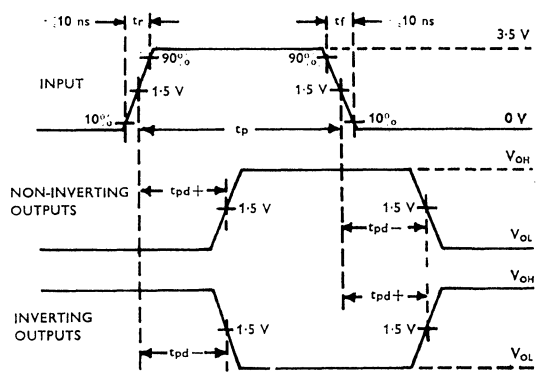
INPUTS				OUTPUTS							
Select			Strobe or Data	(0)	(1)	(2)	(3)	(4)	(5)	(6)	(7)
C*	B	A	G†	2Y0	2Y1	2Y2	2Y3	1Y0	1Y1	1Y2	1Y3
X	X	X	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	H
L	H	L	L	H	H	L	H	H	H	H	H
L	H	H	L	H	H	H	L	H	H	H	H
H	L	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	L	H	H
H	H	L	L	H	H	H	H	H	H	L	H
H	H	H	L	H	H	H	H	H	H	H	L

*Connect inputs 1C and 2C together.
†Connect inputs 1G and 2G together.

Test Circuit



Waveforms



NOTES:
A. The truth table generator has the following characteristics: PRF = 1 MHz, $Z_{out} \approx 50\ \Omega$, tp = 100 ns.
B. C_L includes probe and jig capacitance.
C. All diodes are IN4149.

TYPICAL CHARACTERISTICS

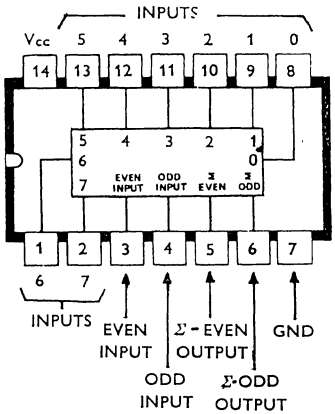
Propagation delay (depending upon input states) . . . . . 36 ns
Power dissipation . . . . . 170 mW
Input loading factor:
Data inputs . . . . . 1 unit load
Odd or even inputs . . . . . 2 unit loads
Maximum fan-out . . 20 unit loads (high logic state)
10 unit loads (low logic state)

Truth Table

INPUTS			OUTPUTS	
ΣOF 1's AT 0 THRU 7	EVEN	ODD	Σ EVEN	Σ ODD
EVEN	1	0	1	0
ODD	11	0	0	1
EVEN	0	1	0	1
ODD	0	1	1	0
X	1	1	0	0
X	0	0	1	1

X = 'Don't care'

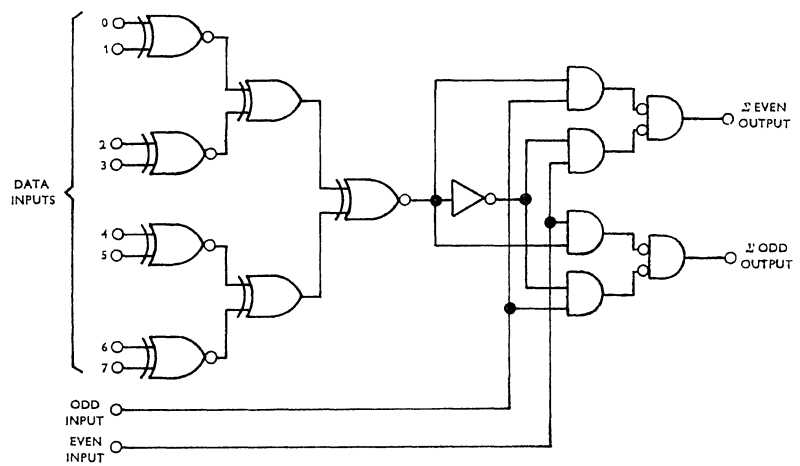
Pin configuration
(top view)



DESCRIPTION

This device is specifically designed for error checking systems. The ITT74180 sums the 8 bits of binary information at the data inputs and gives outputs depending upon whether the sum is even or odd. Additional inputs 'even' and 'odd' can reverse the sense of the summing and also enables the ITT74180 to be cascaded to increase the word length of the data.

Logic diagram

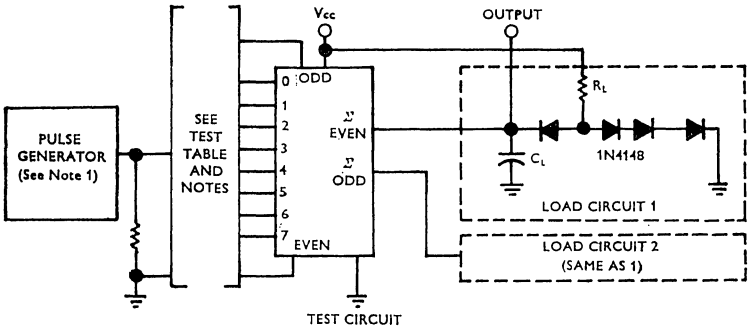


PARAMETER	LIMIT				CONDITIONS	
	Min.	Typ. at 25°C	Max.	Unit	V_{CC}	
I_{CC} supply current						
74 series		34	56	mA	Max.	Data input open with
54 series		34	49	mA	Max.	even and odd inputs both zero or both 2.4V

Information on the absolute maximum ratings and the other D.C. characteristics of this device (which are common to other integrated circuits in this series) is stated in the general information section.

SWITCHING CHARACTERISTICS V_{CC}=5V, T_{AMB}=25°C

PROPAGATION DELAY TIME			LIMIT				CONDITIONS
	From (input)	To (output)	Min.	Typ.	Max.	Unit	
t_{pd+}	Data	Σ Even		40	60	ns	
t_{pd-}	Data	Σ Even		25	38	ns	
t_{pd+}	Data	Σ Odd		32	48	ns	
t_{pd-}	Data	Σ Odd		45	68	ns	Fan-out = 10
t_{pd+}	Data	Σ Even		32	48	ns	Standard load circuit
t_{pd-}	Data	Σ Even		45	68	ns	C_L=15 pF, R_L=
t_{pd+}	Data	Σ Odd		40	60	ns	400 Ω and see test
t_{pd-}	Data	Σ Odd		25	38	ns	table
t_{pd+}	Even or Odd	Σ Even or Σ Odd		13	20	ns	
t_{pd-}	Even or Odd	Σ Even or Σ Odd		7	10	ns	

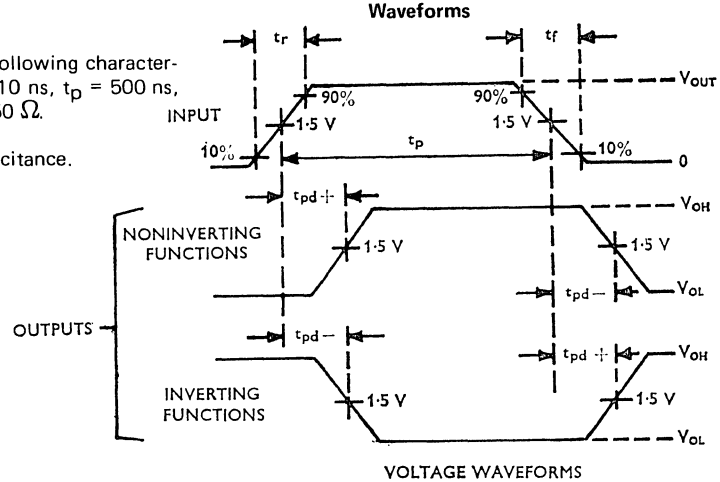


Switching load circuit

NOTES:

1. The pulse generator has the following characteristics: V_{OUT} = 3V, $t_r = t_f$ = 10 ns, t_p = 500 ns, PRF = 1 MHz, and Z_{OUT} 50 Ω.
2. Inputs not specified are open.
3. C_L includes probe and jig capacitance.

Waveforms

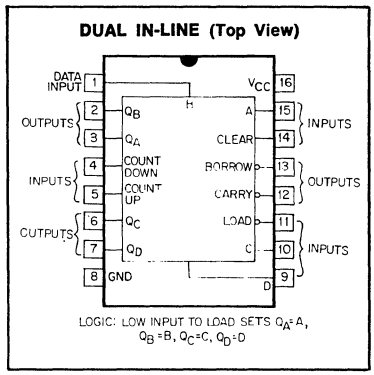


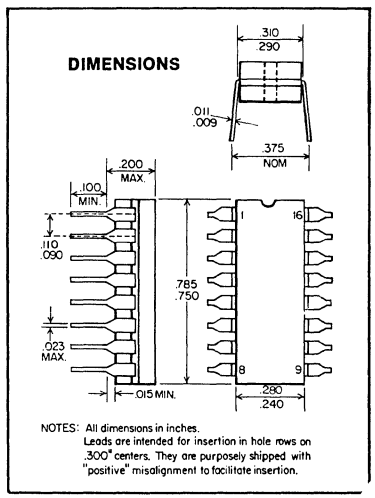
VOLTAGE WAVEFORMS

Test Table

INPUT	CONDITIONS	OUTPUT	INPUT	CONDITIONS	OUTPUT
PULSE	GND	TESTED	PULSE	GND	TESTED
0	ODD	ΣEVEN	2	ODD	ΣODD
1	ODD	ΣEVEN	3	ODD	ΣODD
2	ODD	ΣEVEN	4	ODD	ΣODD
3	ODD	ΣEVEN	5	ODD	ΣODD
4	ODD	ΣEVEN	6	ODD	ΣODD
5	ODD	ΣEVEN	7	ODD	ΣODD
6	ODD	ΣEVEN	EVEN	NONE	ΣEVEN
7	ODD	ΣEVEN	ODD	0	ΣEVEN
0	ODD	ΣODD	EVEN	0	ΣODD
1	ODD	ΣODD	ODD	NONE	ΣODD

SYNCHRONOUS 4-BIT UP-DOWN COUNTER (dual clock with clock)





- **Cascading Circuitry Provided Internally**
- **Guaranteed fanout of 10 TTL loads over the full temperature range and supply voltage ranges.**
- **High capacitive drive capability.**
- **Individual Preset to Each Flip Flop.**
- **Typical power dissipation of 325 mW**
- **The input/output characteristics provide easy interfacing with DTL930, TTL9000, TTL7400 and MSI families.**
- **Input clamp diodes limit high speed line termination effects**
- **Fully Independent Clear Input**
- **Typical Maximum Input Count Frequency . . . . 25 MHz**

The MSI ITT54/74192 is a synchronous up/down decade counter with separate up/down clocks, parallel load (asynchronous) facility, two terminal count outputs for multi-decade operation, and an asynchronous overriding master reset.

The MSI ITT54/74193 is a synchronous up/down 4-bit binary counter with separate up/down clocks, parallel load (asynchronous) facility, terminal count outputs for multi-decade operations, and an asynchronous overriding master reset.

Counting is synchronous, with the outputs changing state after the low to high transition of either the count-up clock (CPu) or count-down clock (CP_D). The direction of counting is determined by which clock input is pulsed while the other clock input is high. (Incorrect counting will occur if both the count-up clock and count-down clock inputs are pulsed simultaneously.) The counter will respond to a clock pulse on either input by changing to the next appropriate state of a binary sequence.

The counter has a parallel load (asynchronous) facility which permits the counter to be reset. Whenever the data enable ($\overline{PL}$) input is low, the information present on the parallel data inputs (P_A, P_B, P_C, P_D,) will be loaded into the counter and appear on the outputs independent of the conditions of the clock inputs. When the data enable input goes lows, this information is stored in the counter and when the counter is clocked it changes to the next appropriate state in the counts sequence. The data inputs are inhibited when the data enable is high and have no effect on the counter.

The terminal count-up ($\overline{TC}_U$) and terminal count-down ($\overline{TC}_D$) outputs (Carry and Borrow respectively) allow multistage binary counter operations without additional logic. The counters are cascaded by feeding the terminal count-up output to the count-up clock input and the terminal count-down output to the count-down input of the following counter.

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

CHARACTERISTICS		UNITS
Storage Temperature	−65°C to +150	°C
Temperature (Ambient) Under Bias	−55°C to +125	°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7	Volts
Voltage Applied to Outputs for high output state	−0.5V to V_{CC}	value
Input Voltage (D.C.)	−0.5V to +5.5	Volts

RECOMMENDED OPERATING CONDITIONS

	ITT54192, ITT54193			ITT74192, ITT74193			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Normalized fan-out from each output, N			10			10	
Input count frequency, f_{count}	0		25	0		25	MHz
Width of any input pulse, t_w	20			20			ns
Data setup time, t_{setup} (see Figure 7 and Note 2)	20			20			ns
Data hold time, t_{hold} (see Note 3)	0			0			ns
Operating free-air temperature range, T_A	-55	25	125	0	25	70	°C

NOTES: 2. Setup time is the interval immediately preceding the positive-going edge of the load pulse during which interval the data to be recognized must be maintained at the input to ensure its recognition.

3. Hold time is the interval immediately following the positive-going edge of the load pulse during which interval the data to be recognized must be maintained at the input to ensure its recognition.

ELECTRICAL CHARACTERISTICS OVER RECOMMENDED OPERATING FREE-AIR TEMPERATURE RANGE (unless otherwise noted)

SYMBOL	CHARACTERISTICS	TEST FIGURE	ITT54192, ITT54193 MIN	TYP‡	MAX	ITT74192, ITT74193 MIN	TYP‡	MAX	UNITS	CONDITIONS†
V_{IH}	High-level input voltage	1 and 2	2			2			V	
V_{IL}	Low-level input voltage	1 and 2			0.8			0.8	V	
V_{OH}	High-level output voltage	1	2.4			2.4			V	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = -400 μA
V_{OL}	Low-level output voltage	2			0.4			0.4	V	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 18 mA
I_{IH}	High-level input current	3			40 1			40 1	μA mA	V_{CC} = MAX, V_I = 2.4 V V_{CC} = MAX, V_I = 5.5 V
I_{IL}	Low-level input current	4			-1.6			-1.6	mA	V_{CC} = MAX, V_I = 0.4 V
I_{OS}	Short-circuit output current‡‡	5	-20		-65	-18		-65	mA	V_{CC} = MAX
I_{CC}	Supply current	6		65	89		65	102	mA	V_{CC} = MAX

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type. ‡All typical values are at V_{CC} = 5 V, T_A = 25°C. ‡‡Not more than one output should be shorted at a time.

SWITCHING CHARACTERISTICS, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER§	FROM INPUT	TO OUTPUT	TEST FIGURE	MIN	TYP	MAX	UNITS	CONDITIONS
f_{max}				25	32		MHz	C_L = 15 pF, R_L = 400 Ω
t_{setup}			7		14	20	ns	
t_{PLH} t_{PHL}	Count-up	Carry	8		17 16	26 24	ns	
t_{PLH} t_{PHL}	Count-down	Borrow	8		16 16	24 24	ns	
t_{PLH} t_{PHL}	Either Count	Q	8		25 31	38 47	ns	
t_{PLH} t_{PLH}	Load	Q	7		27 29	40 40	ns	
t_{PHL}	Clear	Q	7		22	35	ns	

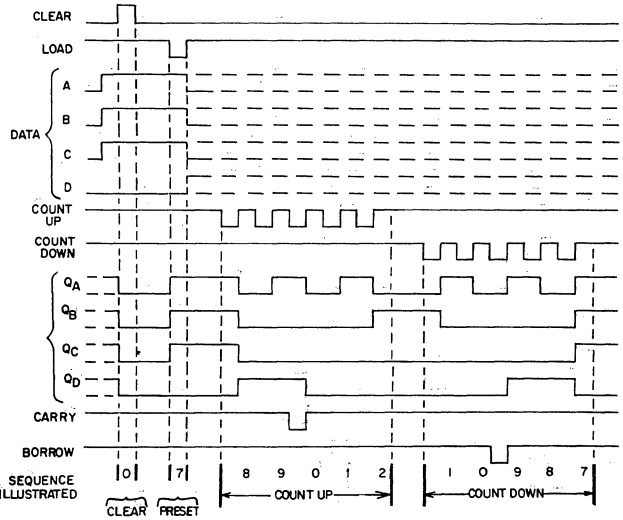
§f_{max} = maximum clock frequency t_{PLH} = propagation delay time, low-to-high-level output t_{PHL} = propagation delay time, high-to-low-level output

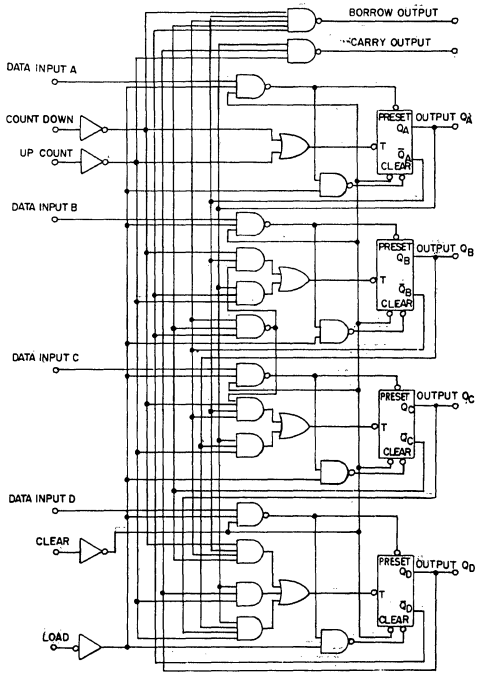
ITT54/74192
ITT54/74193

ITT54-74192 DECADE COUNTERS

TYPICAL CLEAR, LOAD, AND COUNT SEQUENCES

1. Clear outputs to zero.
2. Load (preset) to BCD seven.
3. Count up to eight, nine, carry, zero, one, and two.
4. Count down to one, zero, borrow, nine, eight, and seven.

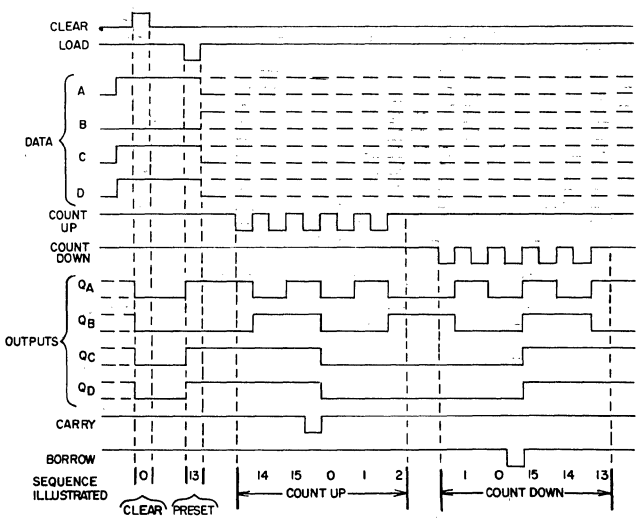


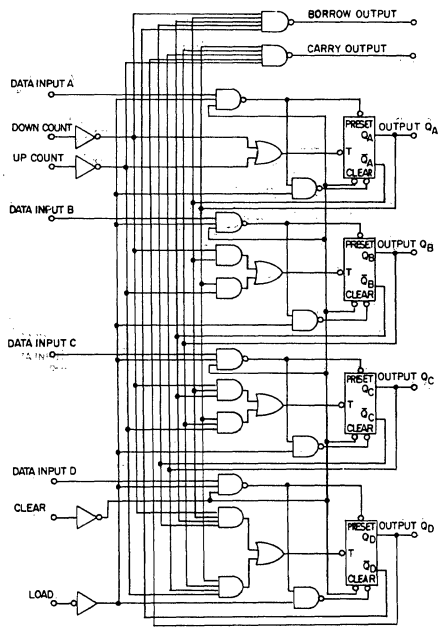


ITT54-74193 BINARY COUNTERS

TYPICAL CLEAR, LOAD, AND COUNT SEQUENCES

1. Clear outputs to zero.
2. Load (preset) to BVD thirteen.
3. Count up to fourteen, fifteen, carry, zero, one, and two.
4. Count down to one, zero, borrow, fifteen, fourteen, and thirteen.





NOTES: A. Clear overrides load, data, and count inputs.
B. When counting up, count-down input must be high; when counting down, count-up input must be high.

PARAMETER MEASUREMENT INFORMATION

D-C TEST CIRCUITS*

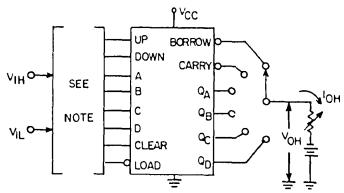


FIGURE 1 – V_{IH}, V_{IL}, V_{OH}
Each output is tested separately.

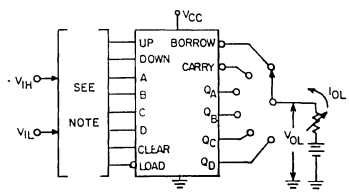


FIGURE 2 – V_{IH}, V_{IL}, V_{OL}
Each output is tested separately.

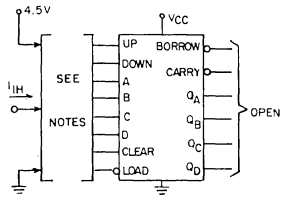


FIGURE 3 – I_{IH}

NOTES: A. Each input is tested separately.
B. Apply V_I to input under test, and ground other inputs except when testing data inputs, apply 4.5 V to clear and load inputs.

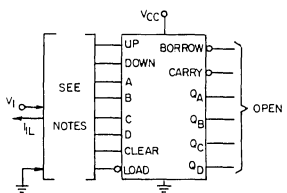


FIGURE 4 – I_{IL}

NOTES: A. Each input is tested separately.
B. Apply V_I to input under test and ground other inputs.

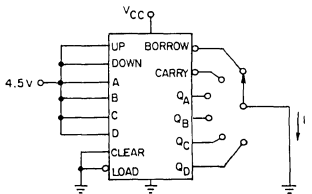


FIGURE 5 – I_{OS}
Each output is tested separately in the high-level state.

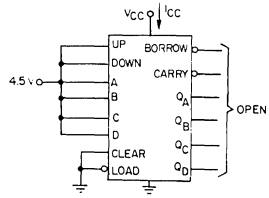
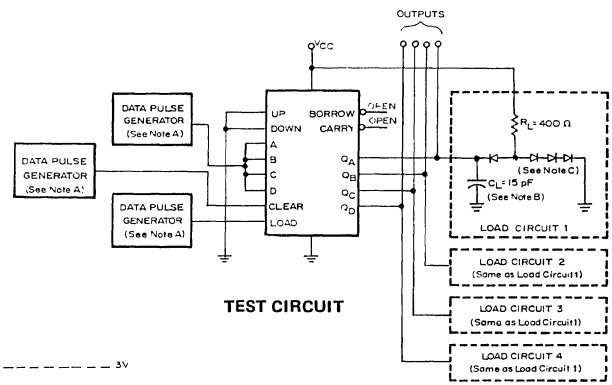


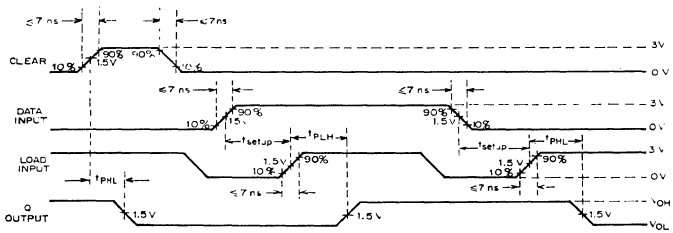
FIGURE 6 – I_{CC}

* Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

SWITCHING CHARACTERISTICS



TEST CIRCUIT



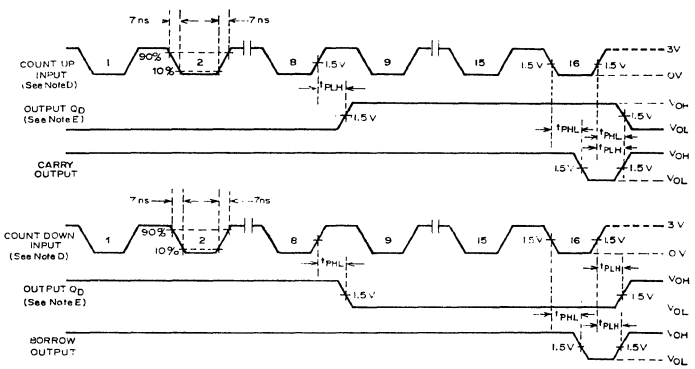
VOLTAGE WAVEFORMS

NOTES: A. The pulse generators have the following characteristics: $Z_{out} \approx 50\ \Omega$; for the data pulse generator, PRR = 500 kHz, duty cycle = 50%; for the load pulse generator, PRR = 1 MHz, duty cycle = 50%.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N3064.

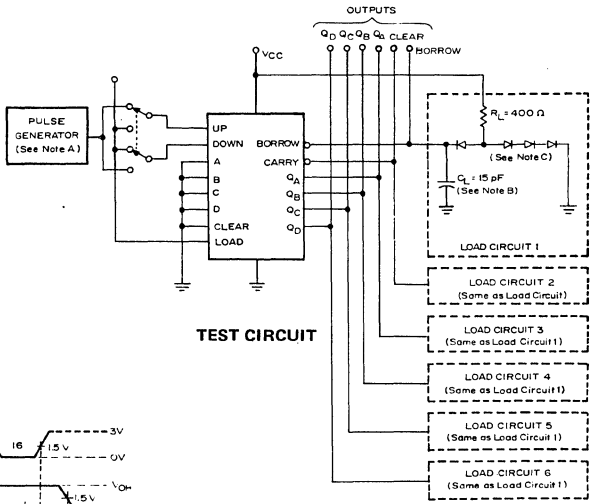
FIGURE 7 – CLEAR, SETUP, AND LOAD TIMES

PARAMETER MEASUREMENT INFORMATION

SWITCHING CHARACTERISTICS



VOLTAGE WAVEFORMS



TEST CIRCUIT

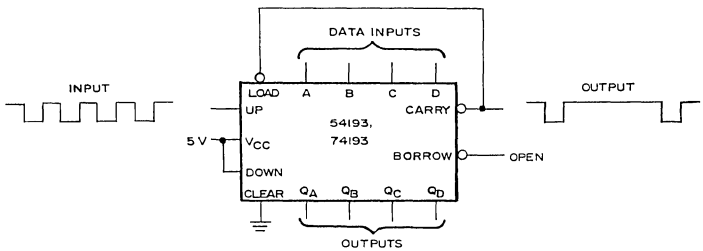
NOTES: A. The pulse generator has the following characteristics: PRR = 1 MHz, $Z_{out} \approx 50\,\Omega$, duty cycle = 50%.
B. C_L includes probe and jib capacitance.
C. All diodes are 1N3064.
D. Count-up and count-down pulses shown are for the SN54193/SN74193 binary counters. Count cycle for SN54192 decade counter is 1 through 10.
E. Waveforms for outputs Q_A, Q_B, and Q_C are omitted to simplify the drawing.

FIGURE 8 – PROPAGATION DELAY TIMES

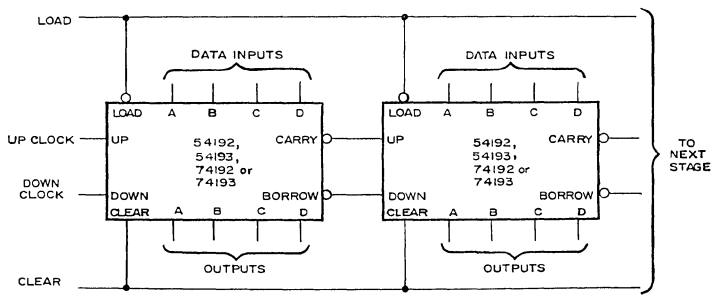
TYPICAL APPLICATION DATA

MODULO-N DIVIDER

The ITT54193/ITT74193 can be used to divide an incoming count frequency by any integral number (N) from one to 16. This is done by modifying the count frequency occurring at the carry output by presetting the data inputs to 16 minus N. By connecting the carry output to the load input, the counter will count to the maximum state (15) and the data inputs will then be enabled on the succeeding clock pulse. The counter outputs are then preset to the levels applied at the data inputs and the count sequence is repeated.



The ITT54192/ITT74192 may be used in the same manner to perform division by any number from 1 to 10.



CASCADING Circuitry is provided internally for cascading these counters. The mode of cascading shown below is ripple borrow/carry. No external components are required.

GENERAL INFORMATION ITT 54H/74H SERIES TTL FAMILY

This series is designed to be used in conjunction with the 54/7400 Series TTL in system locations requiring minimum propagation delays. They form a TTL family (Transistor-Transistor Logic) guaranteed to operate over the following ambient temperature ranges:

54H Series −55°C to 125°C
74H Series 0°C to 75°C

All devices operate over a frequency range between D.C. and typically 30 and 50 MH_Z, and are fully compatible with all 54H/74H series TTL and 930 series DTL.

Clamping diodes are provided at the inputs to enhance the inherent high noise immunity when driving transmission lines. Most outputs are of totem pole configuration to give good drive capability, i.e., high fan-out, especially into large capacitive loads. Other outputs include an open-circuit collector connection.

All functions are available in ceramic dual-in-line or plastic dual-in-line packages.

FEATURES

High speed – typical propagation delay (gate) of 6 ns.

@ C_L = 25pF

Guaranteed noise margin—greater than 400 mV.
Low power dissipation– 23 mW per gate at 50% duty cycle.
Worst case fan-out of 10.
Low output impedance.
Logic levels guaranteed over range of supply voltage and operating temperature

Compatible with other DTL, TTL logic series.

INDEX FOR STANDARD 7400H SERIES

For the military range, replace 74H in the type number by 54H.
Prefix the type number by ITT and end with J which indicates the ceramic dual-in-line package.
For example: ITT5484J is a 16 BIT MEMORY device in 54 series logic with a ceramic dual-in-line package.

TYPE	DESCRIPTION
74H00	Quad 2 i/p NAND
74H01	Quad 2 i/p NAND (open-collector 5-5 V rating)
74H04	Hex inverter
74H05	Hex inverter (open-collector 5-5 V rating)
74H10	Triple 3 i/p NAND
74H20	Dual 4 i/p NAND
74H30	8 i/p NAND
74H40	Quad 2 i/p NAND buffer
74H50	Expandable dual 2 wide, 2 i/p A.O.I.
74H51	Dual 2 wide, 2 i/p A.O.I.
74H53	Expandable 4 wide, 2 i/p A.O.I.
74H54	4 wide, 2 i/p A.O.I.
74H60	Dual 4 i/p expander
74H72	J-K master-slave flip-flop
74H73	Dual J-K master-slave flip-flop
74H74	Dual D-type edge-triggered flip-flop
74H76	Dual J-K master-slave flip-flop with preset and clear

FUNCTIONAL INDEX

	FUNCTION	TYPE
Gates	NAND	74H00
		74H01*
		74H10
		74H20
		74H30
		74H40
	Inverter	74H04
		74H05*
	And-Or-Invert (A.O.I.)	74H50
		74H51
		74H53
		74H54
	Expander	74H60*
Flip-flops		74H72
		74H73
		74H76
	D-type	74H74

INTRODUCTION TO TTL

The TTL circuit configurations are designed so that the uniform logic and noise margin levels apply to all the standard devices in the families. Thus many parameters and their limits are common. In addition the operating conditions are identified for each family. Once these standard operating conditions are understood it becomes possible for the designer to use the family by simply referring to the logic and connection diagrams on each data sheet. All common information is included in the remainder of this section.

For ease in reading, the data only refers to the 74H series family but it is equally applicable to the 54H series. Where there are exceptions these are clearly indicated on the individual data sheets concerned.

LOGIC DEFINITION

Positive logic is used throughout the data sheets. This is defined as follows.

Logical '0' = Low voltage; typically 0.2 V but ⟨ 0.8 V
Logical '1' = High voltage; typically 3.3 V but ⟩ 2.0 V

Current flowing into a device terminal is defined as positive.

D.C. CHARACTERISTICS COMMON TO ALL DEVICES

(except where otherwise stated)

D.C. tests are carried out under the specified conditions. All inputs and outputs are tested for all possible logic states. Worst state load currents and voltages are applied and the test limits are applicable over the full temperature range.

	Min.	Max.	Unit
Supply voltage, V_{CC}:			
74H series	4.75	5.25	V
54H series	4.5	5.5	V
Operating temperature:			
74H series	0	75	°C
54H series	−55	125	°C

D.C. noise margin typically greater than 1V.

ABSOLUTE MAXIMUM RATINGS

(above which the useful life of the device may be impaired)

Continuous supply voltage V_{CC} (Note 1) 7V
Input voltage. . . . . 5.5 V
Voltage between inputs . . . . . 5.5 V
Continuous input current . . . . . −10 mA
Standard output voltage . . . . . −0.5 to 5.5 V
Storage temperature . . . . . −65°C to 150°C

Note I
This rating is reduced to 5.5 V if unused inputs are connected directly to V_{CC}.

STANDARD CHARACTERISTICS

(limits apply over the full range of operating temperature and for standard totem pole output except where otherwise stated).

Where characteristics for devices differ from the table these are shown in the data sheets.

PARAMETER	LIMIT (Note 8)				CONDITIONS	
	Min.	Typ.	Max.	Unit	V_{CC}	
V_{IH}	2.0			V	Min.	V_{OL}⟨0.4V or V_{OH} ⟩ 2.4V (Note 1)
V_{IL}			0.8	V	Min.	V_{OL} ⟨ 0.4V or V_{OH} ⟩ 2.4V (Note 2)
V_{OL} (standard output)		0.22	0.4	V	Min.	I_{OL}= 20mA, V_{IH}=2V or V_{IL}=0.8V (Note 3)
V_{OL} (buffer output) V_{OH}	2.4	3.3		V	Min.	V_{IL}=0.8V or V_{OH}=2.0V (Note 4)
I_{CEX} open collector only			250	μA	Min.	V_{IL}=0.8V, V_{IH}=2V, V_{OUT}=max. o/p voltage rating
$-I_F$			2.0	mA	Max.	V_F=0.4V (Note 5)
I_R			50	μA	Max.	V_R=2.4V, input loading-1 unit load (Note6)
I_R			1.0	mA	Max.	V_R=5.5 V irrespective of input loading
$-I_{SC}$						
54H series	40		100	mA	Max.	V_{OUT}=0 V (Note 7)

Note 1

Condition at outputs dependent on the truth table of the device. For example, for gates and buffers, $V_{OL} \leq 0.4$ V applies, and for flip-flops, either $V_{OL} \leq 0.4$ V or $V_{OH} \geq 2.4$ V applies at each output. Output conditions do not apply for 74H60.

Note 2

Conditions at outputs dependent on the truth table of the device, for example; for gates and inverters $V_{OH} > 2.4$ V. Output conditions do not apply for devices with open collector output. This parameter does not apply for 7413, 74121.

Note 3

Conditions V_{IH} and V_{IL} depend on device truth table.

Note 4

This parameter for totem pole output devices only. V_{IL} and V_{IH} apply according to the truth table. $I_{OH} = -500\ \mu A$ for devices with Fan-out = 10; $I_{OH} = -1.0$ mA for 54H/74H74; $I_{OH} = -1.5$ mA for 54H/74H40.

Note 5

Limits apply for an input loading of 1 unit load; for other input loadings multiply limits by number of unit loads. For flip-flops, see appropriate data for test conditions.

Note 6

All other inputs at 0 V for 74H72, 74H73, 74H76. For 74H74 consult data sheet. Limits to be multiplied by the input loading of the device.

Note 7

For all devices not more than one output to be shorted at any time. Open collector devices: no parameter for $-I_{SC}$.

Note 8

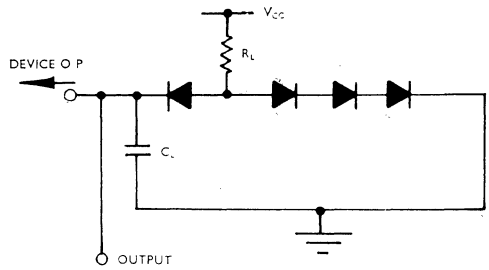
Typical limits are at ambient temperature, $T_A = 25°C$ and $V_{CC} = 5$ V.

A.C. TESTS

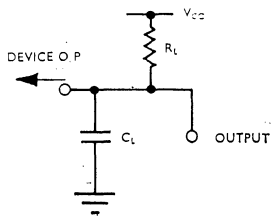
Testing of propagation delays is carried out using the typical switching load circuits shown below. These load circuits are designed to simulate full fan-out loading. An oscilloscope with high impedance probes and having a bandwidth of at least 100 MHz is suitable for these measurements.

TYPICAL SWITCHING TEST LOAD CIRCUITS

For totem pole outputs:



For open collector outputs:

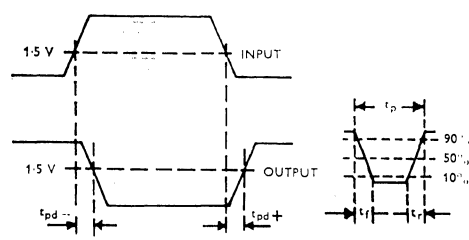


Diodes are type 1N4148 or equiv.

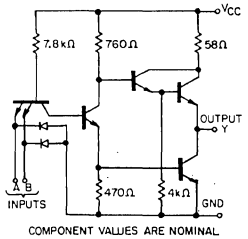
The values of C_L and R_L are quoted in the data sheets. Value of C_L includes probe and jig capitance.

The characteristics of the pulse generator used at the input of the device are stated in the data sheets. Typical characteristics are: $V_{OUT} = 3$ V; Rise time, tr, =Fall time, t_f,=less than 7 ns; $Z_o = 50$; Pulse Repetition Frequency, P.R.F. = 1 MHz; Pulse width for gate, $t_p = 500$ ns.

Waveforms



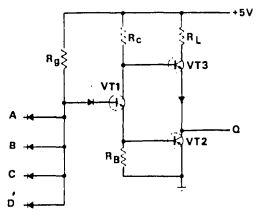
CIRCUIT DIAGRAM OF MIC74H00 GATE



COMPONENT VALUES ARE NOMINAL

The d.c. operation of this circuit is more readily understood if the multiemitter transistor (MET) connecting the inputs is considered equivalent to a diode AND gate in series with an offset diode connected to the base of transistor VT1. This is shown in Fig. 2, the emitter-base junctions of the MET forming the input diodes and the collector-base junction forming the offset diode.

Fig. 2. Simplified analogy of TTL gate.



When all the inputs are positive a logic '1' current flows from the positive supply through R_B into the base of VT1 which heavily conducts and turns VT2 'ON' into the saturated state. Since both VT1 and VT2 are saturated, there is insufficient voltage across the base emitter terminals of VT3 to render it conducting. The output voltage is about +0.2 V, (i.e. saturation voltage of VT2). The collector current of VT2 will consist of the total 'sinking' current from the gates connected to the output terminal. When the base current drive to VT2 is high, VT2 can remain saturated even with a large collector current, with adverse circuit tolerances and temperature variations. This permits a fan-out of up to 10. With a multiemitter transistor, more current flows from a positive held input than with a conventional D.T.L. gate (the leakage current of the reverse biassed input diode) since the MET is biassed in the inverted mode and the functions of emitter and collector are reversed. However, the MET is designed to have a very low inverse gain and I_R is kept to a minimum. I_R will equal the emitter base leakage current plus the product of inverse current gain and I_G.

2. LOW OR OFF STATE

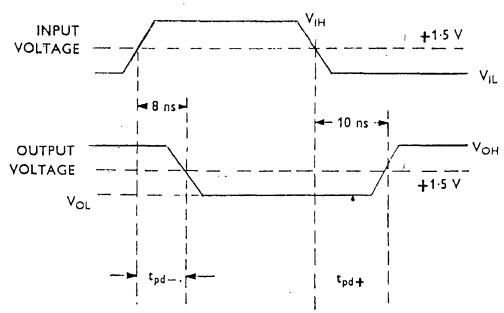
The opposite state shown in Fig. 1B is achieved if the voltage of any number of inputs is reduced below a threshold level of about + 1.5 volts. Fig. 1B shows the conditions when input A is at +0.2 volts (a typical output voltage of a previous gate). No base current flows into VT1 since the collector of the MET is at too low a potential, with respect to its base.

Therefore, no current will flow through VT1 and VT2 other than leakage current (which can be neglected in this analysis). The transistor VT3 will conduct to provide sufficient output current to maintain following gates connected to the output terminal at 3.3 V positive in logic 1. The fan-out is high (10) under worst case conditions because of the low output impedance of VT3.

3. CHANGEOVER BETWEEN STATES

The transistor action of the MET considerably improves the switching speed when compared with a DTL gate. In switching from the ON to the OFF state the MET saturates and rapidly removes the charge stored in VT1 turning it off. Then VT2 begins to turn off and VT3 turns on as the collector potential of VT1 rises. VT3 assists VT2 to turn off and pulls the output terminal rapidly positive, charging any load capacitance. The diode D1 helps to prevent VT2 and VT1 from conducting simultaneously and RL limits the current through VT3 to a safe value during the switch over if the output terminal is accidentally shorted.

Fig. 3. Propagation delay waveforms.



Switching from the OFF to the ON state is more rapid than ON to OFF since none of the transistors VT1, VT2 and MET are saturated in the OFF condition. The switch to the ON condition is particularly fast owing to additional drive by transistor VT1 in turning on VT2. Fig. 3 shows the typical switching times from this gate.

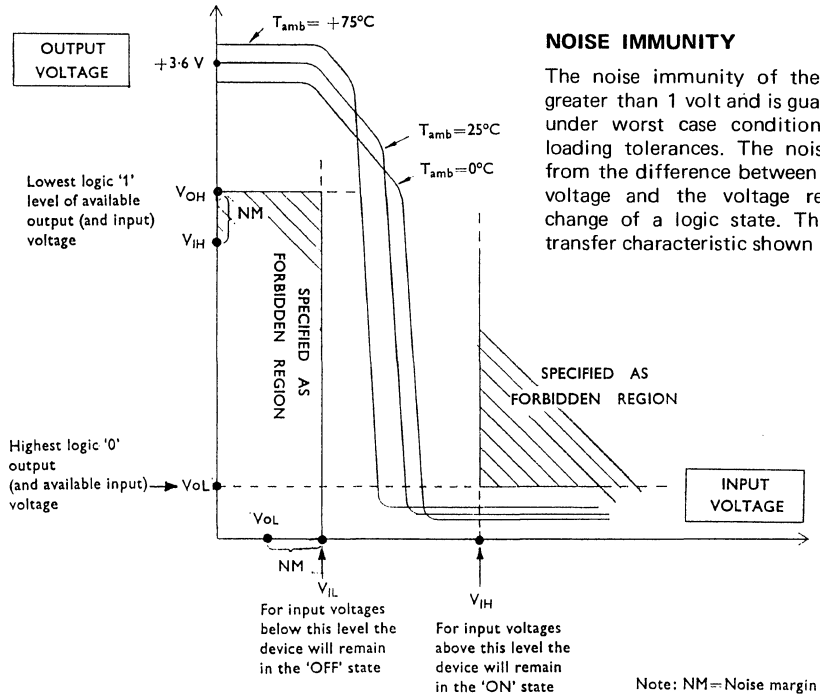


Fig. 4. Typical transfer characteristic showing noise margins

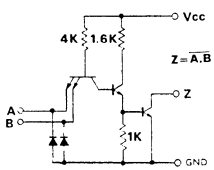
NOISE IMMUNITY

The noise immunity of the TTL gate is typically greater than 1 volt and is guaranteed 0.4 V minimum under worst case conditions for temperature and loading tolerances. The noise immunity is derived from the difference between extreme limits of input voltage and the voltage required to ensure the change of a logic state. This is illustrated by the transfer characteristic shown in Fig. 4.

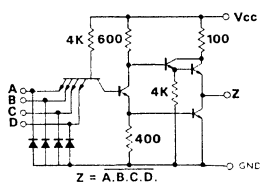
GATES DIFFERING FROM THE STANDARD CIRCUIT

Typical variations from the standard NAND gate circuit configuration are shown in the following circuit diagrams.

Open collector (e.g. 74H01)



NAND buffer (e.g. 74H40)



ITT74H00	Quad 2 input NAND gate
ITT74H01	Quad 2 input NAND gate
ITT74H04	Hex inverter
ITT74H05	Hex inverter (open collector)
ITT74H10	Triple 3 input NAND gate
ITT74H20	Dual 4 input NAND gate
ITT74H30	Single 8 input NAND gate
ITT74H40	Dual 4 input NAND buffer

DESCRIPTION

ITT74H400, ITT74H10, ITT74H20, ITT74H30, ITT74H40 are standard totem pole output gate devices.

ITT74H01 is open collector output device featuring:

Wired or capability
Output rating 5.5V - Suffix "A" denotes 15V

ITT74H40 is a NAND buffer featuring a FAN OUT OF 30.

The circuits of all these devices are the same as those shown in the general information section,

TYPICAL CHARACTERISTICS

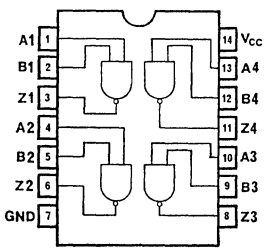
Device type		Propagation delay ns	Power dissipation per package (50% duty cycle) mW
Quad 2 input NAND	74H00	6	.90
Triple 3 input NAND	74H10	6	67.5
Dual 4 input NAND	74H20	6.5	45
Single 8 input NAND	74H30	8	22.5
Open collector 2 input NAND	74H01	9	82
Hex inverter	74H04	6.5	140
Open collector Hex inverter	74H05	9	140
Dual 4 input NAND buffer	74H40	7.5	85

Input loading factor . . . . . 1 unit load

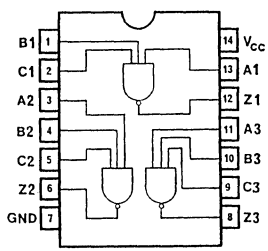
Fan out (for totem pole outputs):
Standard gates . . . . . 1 to 10 unit loads
Buffer gates . . . . . 1 to 30 unit loads

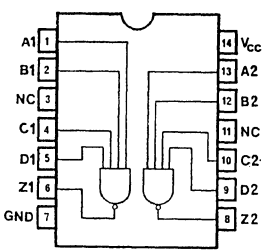
Output voltage rating for
open collector outputs 5.5V

74H400, 74H01

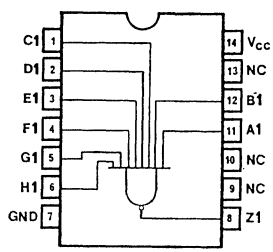


74H10

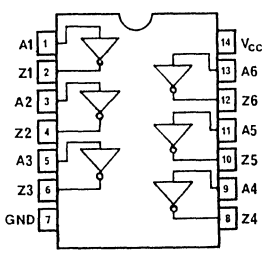




74H20, 74H40



74H30



74H04, 74H05

D.C. CHARACTERISTICS

Information on the absolute maximum ratings and the other D.C. characteristics of these devices (which are common to other integrated circuits in this series) is stated in the general information section.

PARAMETER	LIMIT				CONDITIONS	
	Min.	Typ.	Max.	Unit	V_{CC}	
I_{CCL}						
74H00, 01		26	40	mA	Max.	V_{IN} on all inputs=5.0V
74H10		19.5	30	mA		
74H20		13	20	mA		
74H30		6.5	10	mA		
74H04, 05		40	58	mA		
74H40		25	40	mA		
I_{CCH}						
74H00, 01		10	16.8	mA	Max.	V_{IN} on all inputs=0 V
74H01		6.8	10	mA		
74H10		7.5	12.6	mA		
74H20		5	8.4	mA		
74H30		2.5	4.2	mA		
74H40		10.4	16	mA		
74H04, 05		16	26	mA		
Exceptions to common characteristics:						
$-I_{SC}$ (Buffers) 54/74H40	40		125	mA	Max.	*$V_{OUT} = V_{IN} = 0V$

SWITCHING CHARACTERISTICS

Switching test circuits as shown in the general information section.

Note

Other inputs of the gate under test taken to 2.4 V,

Characteristics of pulse from generator at a device input:

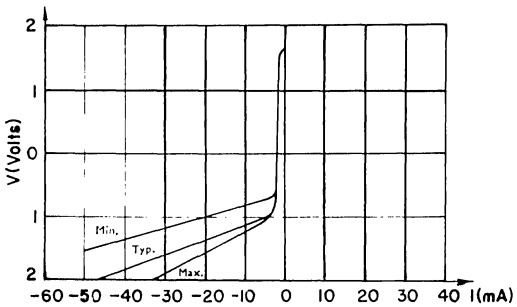
$t_r = 7$ ns, $t_f = 7$ ns, $t_p = 500$ ns, P.R.F. = 1 MHz, $Z_o = 50$, Amplitude = 3.0 V

Parameter		Min.	Typ.	Max.	Units	Conditions
t_{pd+}						
	74H00, 10		5.9	10	ns	See test circuits in introduction, C_L = 25 pF, R_L = 280
	74H20		6	10	ns	
	74H30		6.8	10	ns	
	74H01		10	15	ns	R_L = 280 , C_L = 25 pF
	74H04		6	10	ns	R_L = 280 , C_L = 25 pF
	74H05, 05A		10	15	ns	R_L = 280 , C_L = 25 pF
	74H40		8.5	12	ns	R_L = 93 , C_L = 15 pF
t_{pd-}						See test circuit:
	74H00, 10		6.3	10	ns	R_L = 280 , C_L = 25 pF
	74H01		7.5	12	ns	R_L = 280 , C_L = 25 pF
	74H04		6.5	10	ns	R_L = 280 , C_L = 25 pF
	74H05		7.5	12	ns	R_L = 280 , C_L = 25 pF
	74H20		7	10	ns	R_L = 280 , C_L = 25 pF
	74H30		8.9	12	ns	R_L = 280 , C_L = 25 pF
	74H40		6.5	12	ns	R_L = 280 , C_L = 25 pF

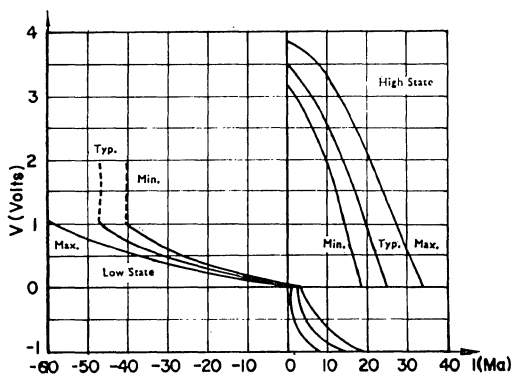
*Only one output to be short-circuited at any time.

TYPICAL CHARACTERISTICS OF STANDARD NAND GATES

Typical and 95% Limit Input Characteristics (at 5 V and 0°C to 75°C)



Typical and 95% Limit Output Characteristics (at 5 V and 0°C to 75°C)



APPLICATION NOTES

Wired-Or Function

The purpose of the 5.5 V open collector devices is primarily to perform the 'wired-OR' function which can not be implemented by the standard active pull up output circuit. The open collector devices require an external resistor between output and V_{CC}. The choice of resistor value is a compromise between fan out requirements, the number of commoned outputs, power dissipation and speed. Limiting values of R_X are given by the following inequalities.

$$R_X > \frac{V_{CC}(max.) - V_{OL}(max.)}{(10-N)\, I_F}$$

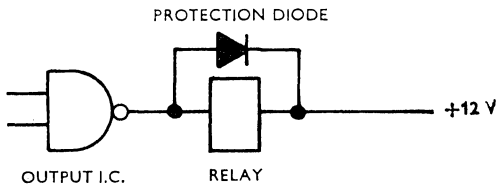
$$R_X < \frac{V_{CC}(min.) - V_{OH}(min.)}{M.I_{CEX} + N.I_R}$$

Where M=Number of outputs commoned together in the 'Wired-OR' function; N=Fan out required.

High Voltage Output

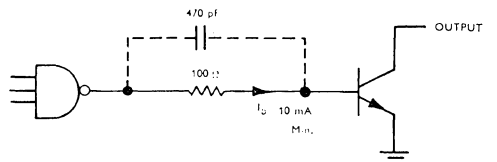
A typical use of the high voltage open collector device:

Miniature relay drives – A protection diode is required to prevent turn off transients damaging the output transistor (as shown).



Output Interfacing

When interfacing between TTL logic and lamps, relays etc. a discrete driving transistor is normally used. If there are several such interface transistors being driven from one multiple gate TTL device a problem is encountered in determining the value of base resistor to be used, to ensure maximum base drive without risk of over dissipating the ICC, when all outputs are high. The circuit shown below is suitable for use with the ITT devices and gives minimum base current of 10 mA.



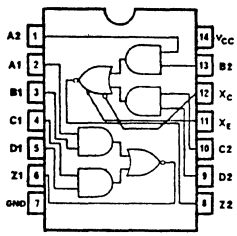
Standard 74 Series Gate

The inclusion of the 470 pF capacitor will give a considerable improvement in speed of this circuit. If the transistor used is a sN2369A propagation delay times from the gate inputs to output of 10ns can be achieved.

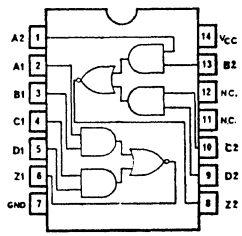
TYPICAL CHARACTERISTICS

Propagation delay . . . . . 6.5 ns
Power dissipation . . . . . 58 mW (74H50, 74H51)
(50% duty cycle) . . . . 42 mW (74H53, 74H54)
Input loading factor . . . . . 1 unit load
Fan-out . . . . . 1 to 10 unit loads

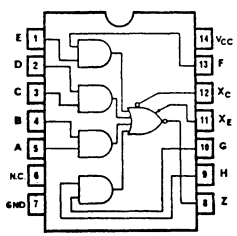
Pin configuration (top views)



ITT74H50

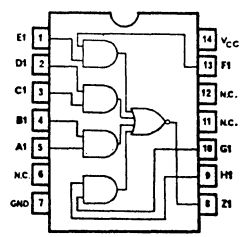


ITT74H51



ITT74H53

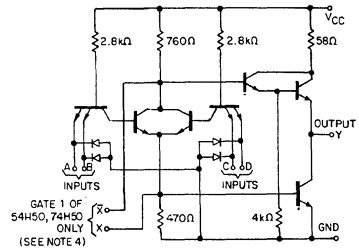
Make no external connection to pins 11 and 12



ITT74H54

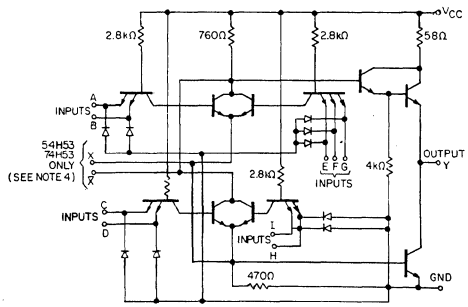
If expander is not used leave pins 11 and 12 open

Circuit diagram of one gate (ITT74H50 and ITT74H51)



NOTES: 1. Component values are nominal.
2. For expanding, both inputs are used together.
3. X and $\bar{X}$ pins are left open when not using expander.
4. Inputs X and $\bar{X}$ are functional on 54H50 and 74H50 circuits only. Make no external connection to X and $\bar{X}$ pins of the 54H51/74H51.
5. A total of four 54H60/74H60 expander gates may be connected to the expander inputs.

Circuit diagram of ITT74H53 and ITT74H54



NOTES. 1. Component values are nominal
2. For expanding, both inputs are used together
3. X and $\bar{X}$ pin are left open when not using expander.
4. Inputs X and $\bar{X}$ are functional on 54H53/7453 circuits only.
5. A total of four 54H60/74H60 expander gates may be connected to the expander inputs.

PARAMETER	LIMIT				CONDITIONS	
	Min.	Type at 25°C	Max.	Units	V_{CC}	
I_{CCH}						
ITT74H50, ITT74H51		15.2	24	mA	Max.	V_{IN} on all inputs
ITT74H53, ITT74H54		19.4	14	mA	Max.	5.0 V
I_{CCL}		4.0	8.0	mA	Max.	V_{IN} on all inputs 0V
ITT74H50, ITT74H51		8.2	12.8			
ITT74H53, ITT74H54		7.1	11			

Information on the absolute maximum ratings and the other D.C. characteristics of these devices (which are common to other integrated circuits in this series) is stated in the general information section.

D.C. CHARACTERISTICS OF ITT5450/3 EXPANDER INPUTS AT −55°C

PARAMETER	LIMIT				CONDITIONS
	Min.	Type	Max.	Unit	V_{CC}
I_X expander current			5.85	mA	Min. $V_{\overline{X}}$ = 1.4 V
V_{BE} base emitter voltage of output transistor			1.0	V	Min. I_{OL} = 20 mA, R_{CE} = 0, I_E = 700 μA (Note 1)
V_{OH} output high voltage	2.4	3.3		V	Min. I_{OH} = −500 μA, I_E = 320 μA, I_C = −320 μA (Note 1)
V_{OL} output low voltage		0.22	0.4	V	Min. I_{OL} = 20 mA, I_E = 470 μA, R_{CE} = 68 (Note 1)

D. C. CHARACTERISTICS OF ITT74H50/3 EXPANDER INPUTS AT 0°C

PARAMETER	LIMIT				CONDITIONS
	Min.	Type	Max.	Unit	V_{CC}
I_X expander current			6.3	mA	Min. $V_{\overline{X}}$ = 1.4 V
V_{BE} base emitter voltage of output transistor			1.0	V	Min. I_{OL} = 20 mA, R_{CE} = 0, I_E = 1.1 mA (Note 1)
V_{OH} output high voltage	2.4	3.3		V	Min. I_{OH} = −500 μA, I_E = 570 μA, I_C = −570 μA (Note 1)
V_{OL} output low voltage		0.22	0.4	V	Min I_{OL} = 20 mA, I_E = 600 μA, R_{CE} = 63 (Note 1)

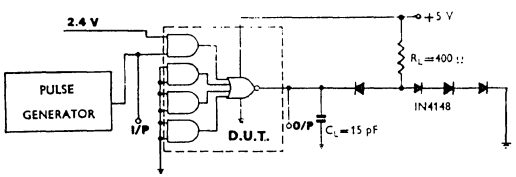
Note 1

V_{CE}, I_E, I_C and R_{CE} refer to voltage, current and resistance on X_E and X_C terminals.

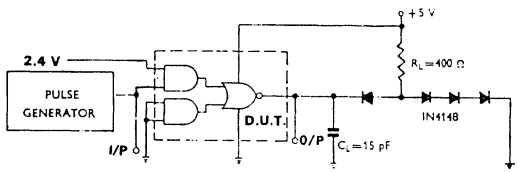
SWITCHING CHARACTERISTICS (V_{CC} = 5.0 V, T_{AMB} = 25°C)

PARAMETER	LIMIT				CONDITIONS
	Min.	Type	Max.	Unit	
t_{pd}^+		7	11	ns	See test circuits, expander pins open
t_{pd}^-		6.2	11	ns	See test circuits, expander pins open
t_{pd}^+		7.4		ns	See test circuits, $C_{\overline{X}}$ = 15 pF
t_{pd}^-		11.4		ns	See test circuits, $C_{\overline{X}}$ = 15 pF

Switching test circuit for ITT74H53/4



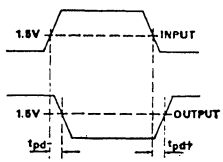
Switching test circuit for ITT74H50/1



Pulse Characteristics

t_f =	= 7 ns
t_r	= 7 ns
t_c	= 500 ns
P.R.F.	= 1 MHz
Z_o	− 50
Amplitude	= 3 V

Waveforms

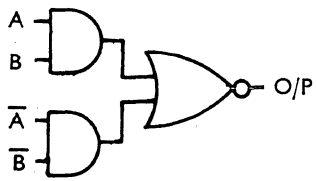


USE OF EXPANDER

The expander points are provided so that the input of the ITT74H50 or the ITT74H53 can be increased by a maximum of four 4-input NAND gates. Both X_C and X_E expander points must be used to connect to the X_C and X_E outputs of the ITT74H60 expander.

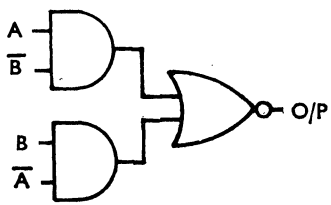
USE AS AN EXCLUSIVE OR GATE

The connections as an exclusive OR gate are shown below with inputs A and B.



A	B	O/P
0	0	0
1	0	1
0	1	1
1	1	0

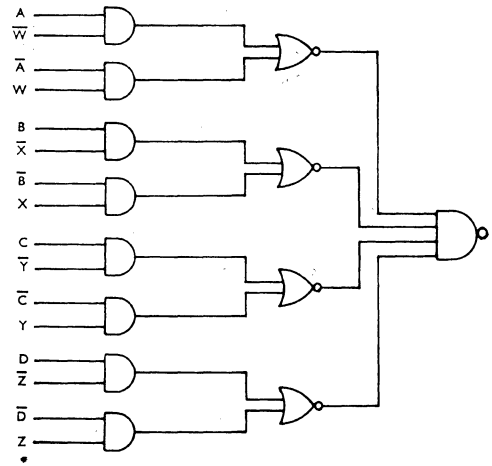
The inverse of exclusive OR function can also be obtained



A	B	O/P
0	0	1
1	0	0
0	1	0
1	1	1

ITT7450 and ITT7451 USED AS A COMPARATOR

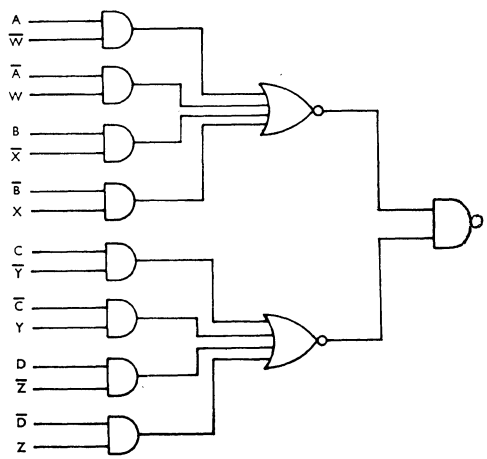
Two binary numbers ABCD and WXYZ.



When ABCD = WXYZ O/P = 0
when ABCD ⟩ or ⟨ WXYZ O/P = 1

ITT7453 and ITT7454 USED AS A COMPARATOR

Two binary numbers ABCD and WYXZ.



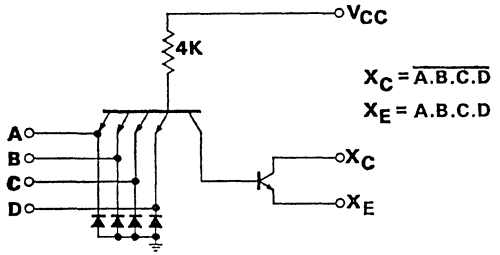
When ABCD - WXYZ O/P = 0
when ABCD ⟩ or ⟨ WXYZ O/P = 1

TYPICAL CHARACTERISTICS

Output capacitance,
V_{CC} and Gnd terminal open . . . . . 1.3 pF
Power dissipation (50% duty cycle) . . . 12.5 mW
Input loading factor . . . . . 1 unit load

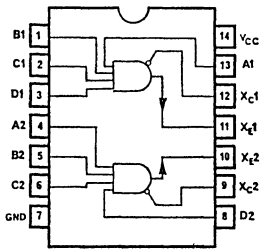
Circuit diagram of one expander

Resistance values in ohms



The ITT74H60 expander is intended for use with the ITT74H50 or ITT74H53 AND-OR-INVERT gates. Not more than four expander gates (two packages) should be connected to any AND-OR-INVERT gate. The X_C and X_E outputs of the expander should be connected respectively to X_C and X_E expander inputs of the AND-OR-INVERT gates. Inter-connecting leads should be kept as short as possible.

Pin configuration



PARAMETER	LIMIT				CONDITIONS	
	Min.	Type at 25°C	Max.	Units	V_{CC}	
V_{ON} on state voltage 74H60			0.4	V	Min	V_E = 1 V, V_{IH} = 2.0 V I_{ON} = 7.4 mA T_{AMB} = 0°C
54H60			0.4	V	Min	I_{ON} = 5.85 mA T_{AMB} = −55°C
V_{ON} on state voltage 74H60			0.4	V	Max	V_E = 0.6 V, V_{IH} = 2.0 V I_{ON} = 7.4 mA T_{AMB} = +70°C
54H60			0.4	V	Max	I_{ON} = 7.85 mA T_{AMB} = +125°C
I_{OFF} off-state output current– 74H60			570	μA	Min.	V_C=v.5V, V_{IL}=0.8V
54H60			320			R_E/GND = 575 Ω T_{AMB} = Min.
I_{ON} on-state output current–						
74H60	−600			μA	Max.	V_{IH}=2.0V, V_E=1.0V
54H60	−470			μA		T_{AMB}=Min.
$-I_F$ input forward current			2.0	mA	Max.	V_F=0.4V
I_R input reverse current			50	mA	Max.	V_R=5.5V

INPUT EXPANDER

PARAMETER	LIMIT				CONDITIONS	
	Min.	Type	Max.	Units	V_{CC}	
I_{CCH} supply current for highest dissipation (off state)		3	4.5	mA	Max.	V_{IN} on all inputs OV, V_E=0.85V
I_{CCL} supply current for lowest dissipation (on state)		1.9	3.5	mA	Max.	V_{IN} on all inputs 5.0V, V_E=-.85V

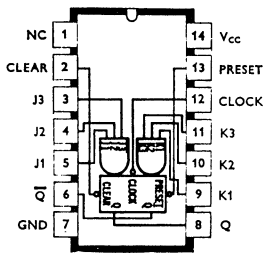
Information on the absolute maximum ratings and the other D.C. characteristics of this device (which are common to other integrated circuits in this series) is stated in the general information section.

TYPICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

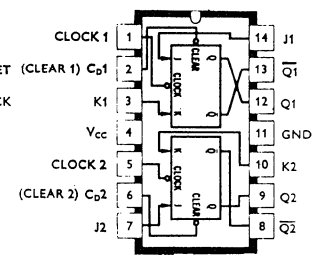
Maximum clock frequency	25 MHz
Propagation delay	18 ns
Power dissipation:	
Single type	80 mW
Dual type	160 mW
Input loading factor:	
J and K clock inputs	1 unit load
Direct and clock inputs	2 unit loads
Fan-out	1 to 10 unit loads
Clock pulse width t_{cp}	12 ns
Clear pulse width t_c	12 ns, 74H72, 74H73 t_{cp}, 74H76
Preset pulse width t_p	16 ns. 74H72, 74H76
Input set up time t_{sp}	t_{cp}
Input hold time t_h	0 ns

Pin configurations

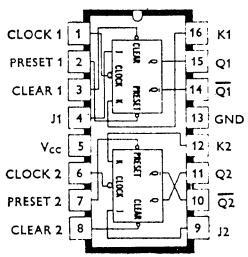
ITT7472



ITT7473



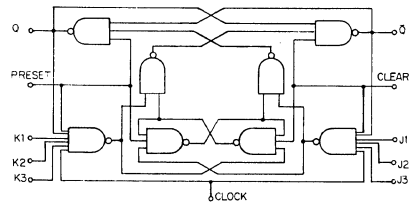
ITT7476



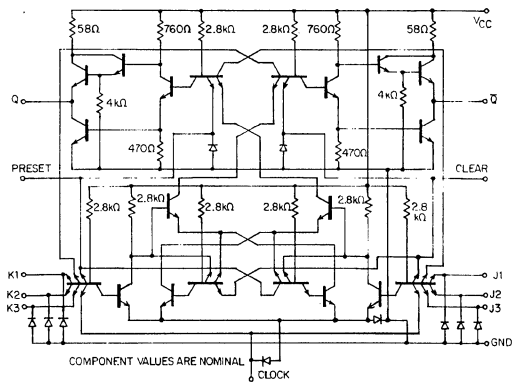
Truth Table

SYNCHRONOUS			ASYNCHRONOUS			
t_n	t_n+1		Preset	Clear	Q	$\overline{Q}$
D Input	Q	$\overline{Q}$	0	0	1	1
0	0	1	1	0	0	1
1	1	0	0	1	1	0
			1	1	No Control	

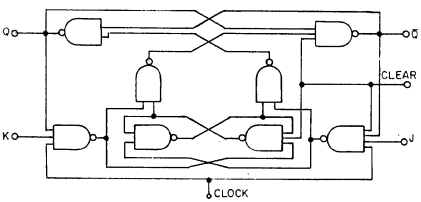
Logic diagram



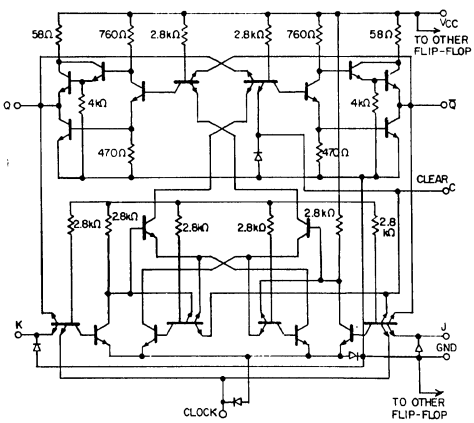
Circuit diagram 74H72



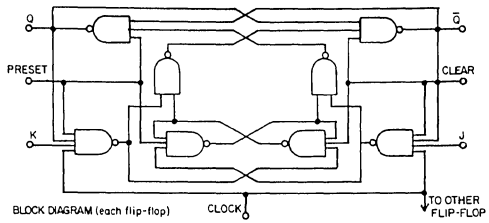
Logic diagram



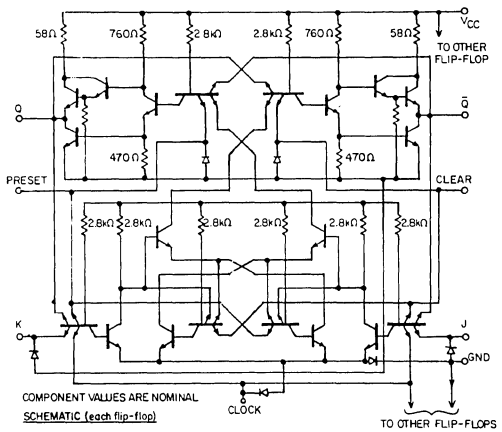
Circuit diagram ITT74H73



Logic diagram



Circuit diagram 74H76



DESCRIPTION

These devices consist of gated Master and slave bistables. The ITT74H72 with preset, clear and triple J and K inputs. The ITT74H73 with clear and single J and K inputs. The ITT74H76 with preset, clear and single J and K inputs. The direct inputs of clock J or K inputs. The clock input operates as follows, on a positive going transistion first the slave bistable is isolated from the master, then information is transferred from the J and K inputs to the master bistable. On a negative going transition first the J and K inputs are disabled then the information is transferred to the slave bistable. Operation will be according to the truth table if J and K information is present before and during the period that the clock is high. Because of the internal feedback from the Q and $\bar{Q}$ outputs to the J and K input AND gates one or other of the gates will have a logical '0' on one internal input. The external inputs cannot affect that gate. The other input AND gate will have a logical '1' on its internal input, if one of the external inputs goes to a logical '1' at any time while the clock is high the master bistable will change state and the Q and $\bar{Q}$ outputs will follow on the negative transition of the clock.

PARAMETER	LIMIT				CONDITIONS
	Min.	Type at 25°C	Max.	Units	V_{CC}
$-I_F$ input forward current					
All J and K inputs and clock			2.0	mA	Max. V_F=0.4V
Preset, clear			4.0	mA	Max. (Note 1)
I_R					
J and K inputs and clock			50	μA	Max. V_R = 2.4 V
Preset, and clear			100	μA	Max. V_R = 2.4 V
I_{CC} supply current		16	25	mA	Max.
Single type		32	50	mA	
All dual types					

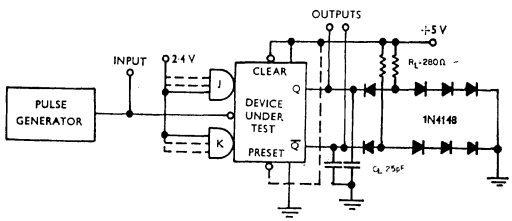
Note 1
Test with all other inputs at 4.5 V. Use preset or clear to set device to appropriate logic stste. Clock to be tested for both logic states. When testing J or K inputs all other inputs including internal inputs to the appropriate input AND gate must be at logical '1'.

Information on the absolute maximum ratings and the other D.C. characteristics of this device (which are common to other integrated circuits in this series) is stated in the general information section.

SWITCHING CHARACTERISTICS V_{CC}=5.0V, T_{AMB}=25°C

PARAMETER	LIMIT				CONDITIONS
	Min.	Typ.	Max.	Unit	
f_{max} maximum input clock frequency	25	30		MHz	Use test circuit 1.
t_{pd}+ propagation delay time to logical '1'					
Clear or preset to output		6	13	ns	Use test circuit 2.
Clock to output	6	14	21	ns	Use test circuit 1.
t_{pd}- propagation delay time to logical '0'					
Clear or preset to output		12	24	ns	Use test circuit 2.
Clock to output	10	22	27	ns	Use test circuit 1.

Test Circuit 1

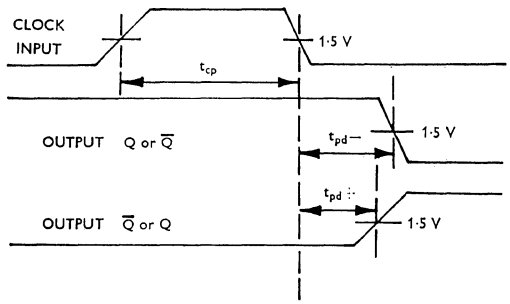


C_L includes probe and jig capacitance

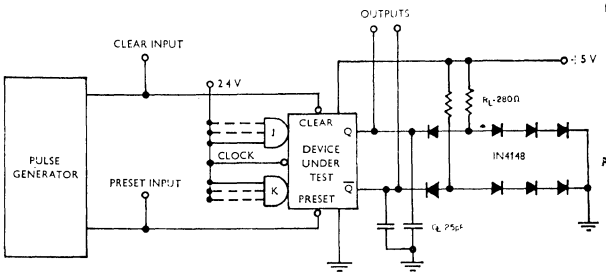
Pulse Characteristics

t_r = 7 ns
t_f = 7 ns
t_{cp} = 20 ns
R.F. = 1 MHz
Amplitude = 3 V

Waveforms



Test circuit 2)

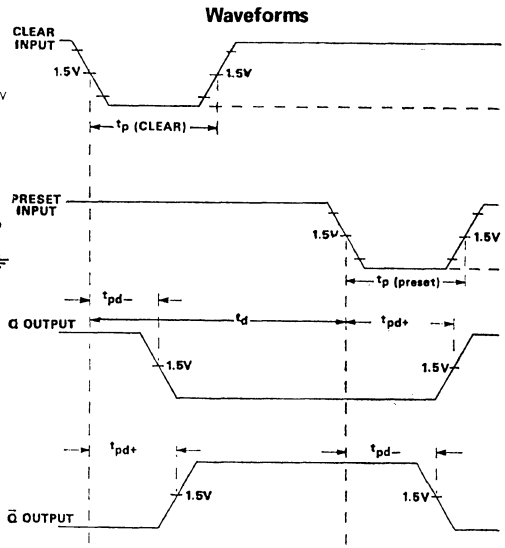


C_L includes probe and jig capacitance

Pulse Characteristics

Same as Test Circuit 1, except t_p = 16 ns.

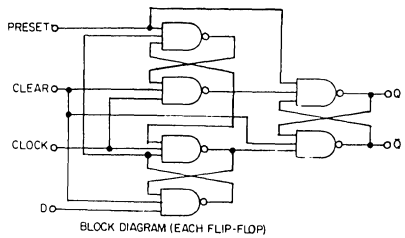
Waveforms



TYPICAL CHARACTERISTICS AND OPERATING CONDITIONS

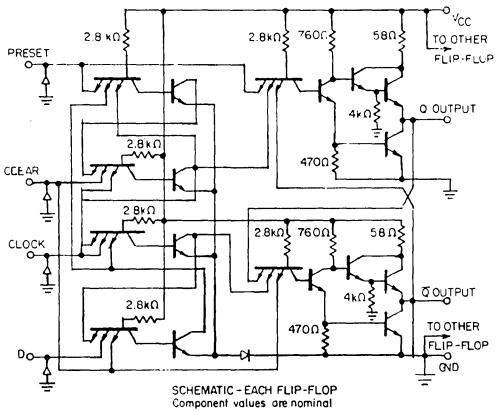
Maximum clock frequency	35 MHz
Propagation delay	11 ns
Power dissipation	150 mW
Input loading factor:	
Preset or data	1 unit load
Clear or clock	2 unit loads
Fan out	1 to 10 unit loads
Clock pulse width t_{cp}	15 ns min.
Preset or clear pulse width t_p	25 ns min.

Logic diagram



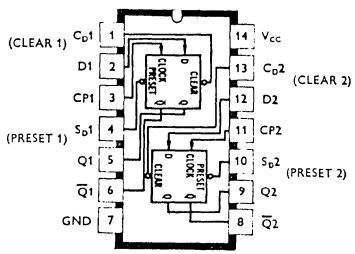
BLOCK DIAGRAM (EACH FLIP-FLOP)

Circuit diagram of one flip-flop



SCHEMATIC - EACH FLIP-FLOP
Component values are nominal

Pin configuration
(top view)



Truth Table

SYNCHRONOUS			ASYNCHRONOUS			
t_n		t_n+1	Preset	Clear	Q	Q̄
D Input	Q	Q̄	0	0	1	1
0	0	1	1	0	0	1
1	1	0	0	1	1	0
			1	1	No Control	

DESCRIPTION

The ITT74H74 is an edge triggered D type flip-flop in which the transfer of the D input data takes place during the positive transition of the clock input. When the clock input is above or below the transfer threshold the 'D' input is inhibited. The transfer threshold is not directly related to the transition time of the positive going edge. Preset and clear inputs operate irrespective of the logic state of the clock or D input.

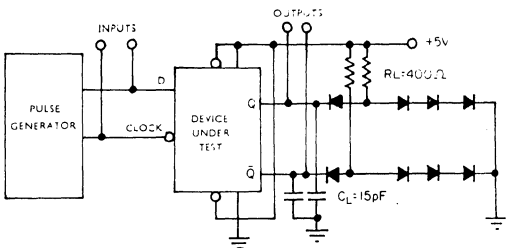
PARAMETER		LIMIT			CONDITIONS	
	Min.	Typ. at 25°C	Max.	Unit	V_{CC}	
$-I_F$ Preset or D input			2.0	mA	Max.	V_F=0.4V
Clear or clock			4.0	mA	Max.	V_F=0.4V
I_R D input			50	µA	Max.	V_R=2.4V
Preset or clock			100	µA	Max.	V_R=2.4V
All inputs			1	mA	Max.	V_R-5.5V
Clear			150	µA	Max.	V_R=2.4V
I_{CC} 54H74		30	42	mA	Max.	All inputs high
74H74		30	50	mA		

Information on the absolute maximum ratings and the other D.C. characteristics of this device (which are common to other integrated circuits in this series) is stated in the general information section.

SWITCHING CHARACTERISTICS V_{CC}=5.0V, T_{AMB}=25°C

PARAMETER	LIMIT				CONDITIONS
	Min.	Typ.	Max.	Unit	
f_{max} maximum input clock frequency	35	43		MHz	Use test circuit 1
t_{sp} minimum input set up time		10		ns	**Use test circuit 1 ("Low" Data)**
		15		ns	**Use test circuit 1 ("High" Data)**
t_h minimum input hold time	0			ns	Use test circuit 1
t_{pd+} clear or preset to output			20	ns	Use test circuit 2
t_{pd+} clock to output	4	8.5	15	ns	Use test circuit 1
t_{pd-} clear or preset to output			30	ns	Use test circuit 2
t_{pd-} clock to output	7	13	20	ns	Use test circuit 1

Test Circuit 1

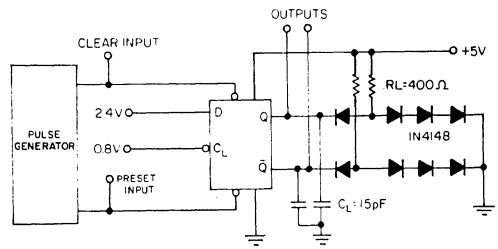


Pulse Characteristics

t_r = 7 ns
t_f = 7 ns
t_{cp} = 20 ns
t_p (D input) = 60 ns
R.F. clock = 1 MHz
R.F D input = ½ R.F clock
Amplitude = 3 V

C_L includes probe and jig capacitance

Test Circuit 2

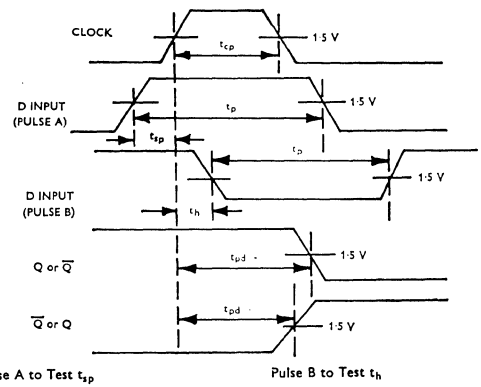


Pulse Characteristics

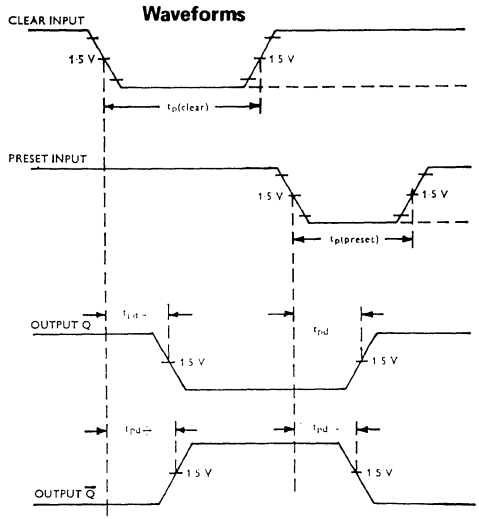
t_r = 7 ns
t_f = 7 ns
t_p = 25 ns
R.F. = 1 MHz
Amplitude = 3 V

C_L includes probe and jig capacitance

Waveforms



Waveforms



HIGH SPEED SATURATED TRANSISTOR-TRANSISTOR LOGIC CIRCUITS

- **Single power supply requirements: 5 volts optimum, 4.5 to 5.5 volts range**
- **High speed: typical gate propagation delay time of 7 ns**
- **High DC noise margin: typically one volt**
- **Added input diodes and low output impedance provides minimum AC noise susceptibility**
- **Fan Out: 10TTL loads**
- **Power dissipation: 11mw per NAND gate at a 50% duty cycle**
- **Compatible with ITT DTL family and other DTL and TTL circuits**
- **NAND gate pin configurations are compatible with DTL**

The ITT MIC9000 Series of TTL circuits is designed to be used in any digital system where good noise immunity, high speed, medium power and high fan-out performance is required. The line is characterized by a broad number of functions available in a variety of packages. The basic elements of the family are active low level output AND gates commonly known as NAND gates.

Typical high level noise immunity of every device in the family is 1.9 V and typical low level noise immunity is 0.9 V. Worst case immunity is 400 mV over the entire temperature range. Power dissipation is typically 11 mW per gate function at a 50% duty cycle, and the average propagation delay is 7 nanoseconds per gate function. A single 5 V ±10 per cent power supply is used with the circuits.

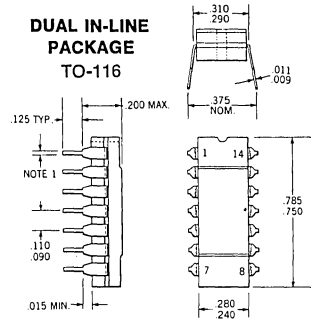
The gates were designed to provide low output impedance in both high and low states which results in good capacitive drive capability and good immunity to crosstalk. The output impedance in the low state is about 10 ohms and in the high state, about 20 ohms. To further enhance noise immunity, all inputs of all devices incorporate diode clamps which considerably reduces the ringing which can result from long lines and impedance mismatches. The binary elements are of a JK, DC master slave design and will toggle at 40 MHz, except for the 9000 element. The 9000 has capacitors purposely incorporated in the design to increase its set-up time and provide it with considerable immunity to long clock skew. Due to the longer set-up time the 9000 toggle frequency is 20 MHz. A common JK input is incorporated on all binary elements to provide data entry inhibit/enable. The input to the clock on each element is buffered to reduce the clock input loading.

The V_{CC} and ground terminals of all devices are located on diagonal corners of the package which allows two degrees of freedom in routing of power and ground leads on the PC boards. Special care has been taken in establishing pin-outs for the flip-flop so as to minimize cross-overs when laying out common dynamic functions with these elements. Simple loading rules are incorporated so that the fan-in and fan-out capability of each device will be quickly established.

The MIC9000 series TTL is compatible with DTL and MSI devices as well as the more complex functions which will be available in the future.

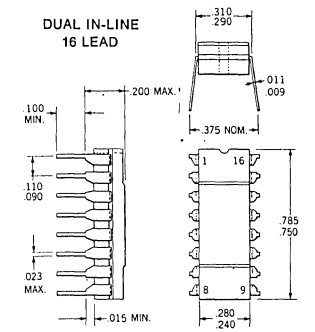
DIMENSIONS

DUAL IN-LINE PACKAGE TO-116

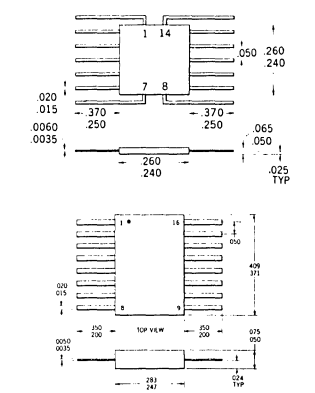


NOTE: 1. Board drilling dimensions should equal your practice for a conventional .020 inch diameter lead.

DUAL IN-LINE 16 LEAD



DIMENSIONS — FLAT PACK TO-86



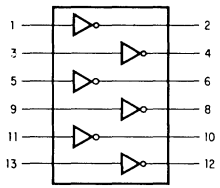
16 LEAD—check factory for availability

NOTE: All dimensions in inches

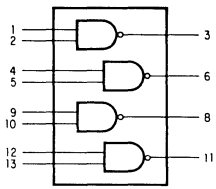
MIC9000 SERIES TTL INTEGRATED CIRCUITS

NAND GATES

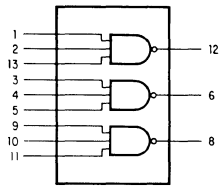
9016



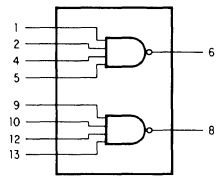
9002



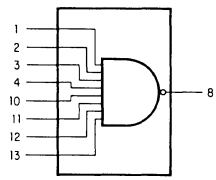
9003



9004

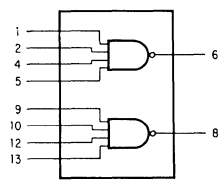


9007



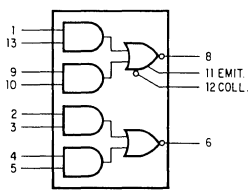
BUFFER

9009

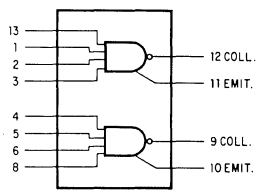


AND-OR-INVERT GATES AND EXTENDER

9005

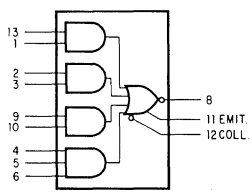


9006



(extender for use with 9005 & 9008)

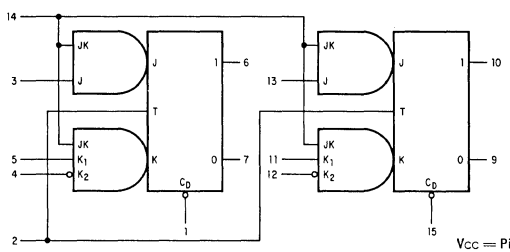
9008



V_{CC} = Pin 14
Gnd = Pin 7

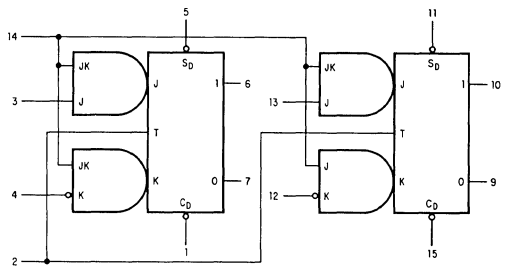
DUAL FLIP-FLOPS

9020



V_{CC} = Pin 16
Gnd = Pin 8

9022



SPECIAL ORDERING CODE

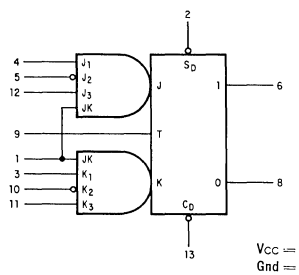
Temperature Range:
−55°C to +125°C, add −1 to MIC number.
0°C to +75°C, add −5 to MIC number.

Case Style:
.250" x .250" Flat Pack, add "B" following last digit.
Ceramic Dual In-Line, add "D" following last digit.

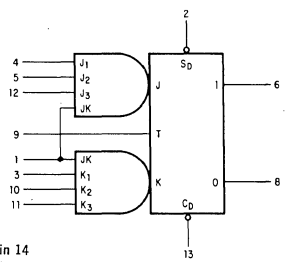
Example:
MIC 9002-1D is −55° to +125°C. Temperature range in Ceramic Dual-In-Line package.
Flat-pack and Dual-In-Line packages have same pin configuration.

SINGLE FLIP-FLOPS

9001



9000



V_{CC} = Pin 14
Gnd = Pin 7

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

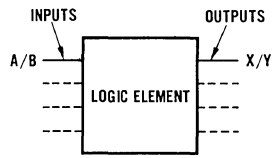
Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias (MIC9000-1)	−55°C to +125°C
Temperature (Ambient) Under Bias (MIC9000-5)	0°C to +75°C
V_{CC} Pin Potential to Ground (See Note 1)	−0.5V to +8.0V
Input Voltage (D.C.) (See Note 2)	−0.5V to +5.5V
Input Current (See Note 2)	−30 mA to +5.0 mA
Output Voltage, Output Normally High	0 V to +V_{CC} value
Current Into Output Terminal, Output Low (except 9009)	50 mA
Current Into Output Terminal, Output Low 9009	100 mA

NOTE 1
The maximum V_{CC} value of 8.0 volts is not the primary factor in determining the maximum V_{CC} which may be applied to a number of interconnected devices. The voltage at a high output is approximately 2 V_{BE}'s below the V_{CC} voltage, so the primary limit on the V_{CC} is that the voltage at any input may not go above 5.5 V unless the current is limited, so this effectively limits the system V_{CC} to approximately 7.0 volts.

NOTE 2
Because of the input clamp diodes, excess current can be drawn out of the inputs if the D.C. input voltage is more negative than −0.5 V. The diode is designed to clamp off large negative A.C. swings associated with fast fall times and long lines. This maximum rating is intended only to limit the steady state input voltage and current.

LOADING RULES

In this data sheet the following notation has been chosen to indicate the input loading and output drive for all logic elements.



Where A=high logic level input load factor
B=low logic level input load factor
X=high logic level output drive factor
Y=low logic level output drive factor

When checking for loading violations it is only necessary to insure that the sum of the high logic level input load factors at any node does not exceed the high logic level output drive factor at that node. The same is true for the low level load and drive factors. These rules apply only within the TTL MIC9000 series.

Multiplying the factor with the appropriate current per unit load gives the input loading or output drive in terms of current. For the TTL circuits of this data sheet, current per unit is −1.6 mA maximum at the low logic level and is 60 μA maximum at the high logic level.

In the case where unused inputs of an AND gate are shorted to a driven input, the high logic level input load factor for the inputs will be the number of inputs shorted together times the high logic input load factor for one input. The low logic level input load factor for the inputs will be the same as that for a single input.

UNUSED INPUTS

Proper termination of unused inputs will result in maximum operating speed. Substantial degradation of turn-on delay may occur if unused inputs are left open.

The following are acceptable ways to terminate unused inputs:

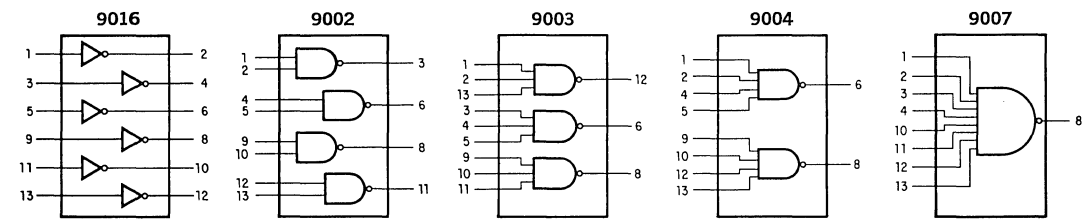
1. Tie the input to a used input on the same gate. The TTL 9000 series has made special provision for this method by offering extra high level drive factor on all outputs.
2. Tie the input to V_{CC} through a resistor. This resistor should be chosen to keep the input current within absolute maximum ratings for any possible extreme of the V_{CC} supply. More than one input may be terminated through one resistor.
3. Tie inputs to a separate supply between 4.5 and 2.4 V, if one should be available.
4. Tie the inputs to the output of an unused gate. The unused gate must provide a constant high level output.

NAND GATES — 9002, 9003, 9004 AND 9007

HEX INVERTER — 9016

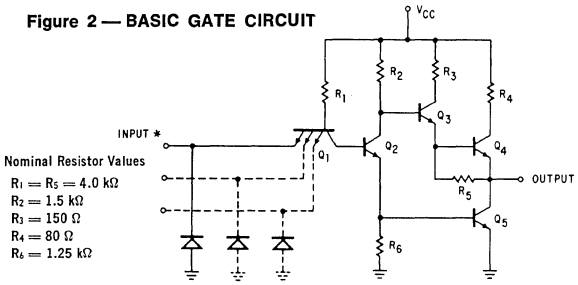
The 9002, 9003, 9004 and 9007 are active low level output AND gates commonly known as NAND gates. The 9016 is a hex inverter with input and output characteristics identical to the 9002, 9003, 9004 and 9007. The variety of gate combinations provides the system designer the utmost in logic flexibility and reduces package count.

Figure 1 — LOGIC SYMBOL AND PIN CONFIGURATIONS



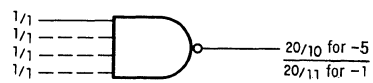
V_{CC} = PIN 14, GND = PIN 7

Figure 2 — BASIC GATE CIRCUIT



*Number of inputs depends on the gate.

Figure 3 — LOADING FACTORS



ELECTRICAL CHARACTERISTICS 9002, 9003, 9004, 9007 AND 9016 (T_A = −55°C to 125°C, V_{CC} = 5.0 V ± 10%)

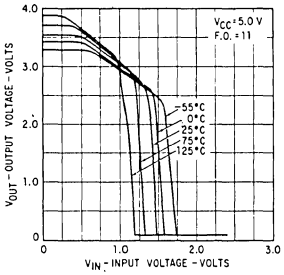
SYMBOL	CHARACTERISTIC	LIMITS −55°C MIN.	LIMITS −55°C MAX.	LIMITS 25°C MIN.	LIMITS 25°C TYP.	LIMITS 25°C MAX.	LIMITS 125°C MIN.	LIMITS 125°C MAX.	UNITS	CONDITIONS
V_{OH}	Output High Voltage	2.4		2.4	2.7		2.4		Volts	V_{CC} = 4.5 V I_{OH} = −1.32 mA Inputs at V_{IL} (see below)
V_{OL}	Output Low Voltage		0.4		0.21	0.4		0.4	Volts	V_{CC} = 5.5 V I_{OL} = 17.6 mA V_{IH} = 5.5 V
										V_{CC} = 4.5 V I_{OL} = 13.6 mA Inputs at V_{IH} (see below)
V_{IH}	Input High Voltage	2.0		1.7			1.4		Volts	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.8			0.9		0.8	Volts	Guaranteed input low threshold for all inputs
I_F	Input Load Current		−1.6		−1.1	−1.6		−1.6	mA	V_{CC} = 5.5 V V_F = 0.4 V
			−1.24		−0.87	−1.24		−1.24		V_{CC} = 4.5 V 5.5 V on other inputs
I_R	Input Leakage Current				10	60		60	μA	V_{CC} = 5.5 V V_R = 4.5 V GND on other inputs
I_{PD}	V_{CC} Current, Gate On (each gate)		5.5		3.5	5.5		5.5	mA	V_{CC} = 5.0 V Inputs high
	V_{CC} Current, Gate Off (each gate)		1.6		1.07	1.6		1.6		V_{CC} = 5.0 V Inputs at gnd
t_{pd+}	Switching Speed				3.0	10			ns	V_{CC} = 5.0 V, See t_{pd} test circuit
t_{pd-}	Switching Speed				3.0	12			ns	C_L = 15 pF

ELECTRICAL CHARACTERISTICS 9002, 9003, 9004, 9007 AND 9016 (T_A = 0°C to 75°C, V_{CC} = 5.0 V ± 5%)

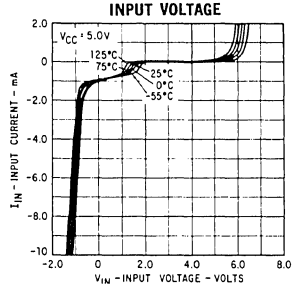
SYMBOL	CHARACTERISTIC	LIMITS 0°C MIN.	LIMITS 0°C MAX.	LIMITS 25°C MIN.	LIMITS 25°C TYP.	LIMITS 25°C MAX.	LIMITS 75°C MIN.	LIMITS 75°C MAX.	UNITS	CONDITIONS
V_{OH}	Output High Voltage	2.4		2.4	2.9		2.4		Volts	V_{CC} = 4.75V I_{OH} = −1.2 mA Inputs at V_{IL} (see below)
V_{OL}	Output Low Voltage		0.45		0.21	0.45		0.45	Volts	V_{CC} = 5.25 V I_{OL} = 16.0 mA V_{IH} = 5.25 V
										V_{CC} = 4.75 V I_{OL} = 14.1 mA Inputs at V_{IH} (see below)
V_{IH}	Input High Voltage	1.9		1.8			1.6		Volts	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.85			0.85		0.85	Volts	Guaranteed input low threshold for all inputs
I_F	Input Load Current		−1.6		−1.0	−1.6		−1.6	mA	V_{CC} = 5.25 V V_F = 0.45 V
			−1.41		−0.91	−1.41		−1.41		V_{CC} = 4.75 V 5.25 V on other inputs
I_R	Input Leakage Current				10	60		60	μA	V_{CC} = 5.25 V V_R = 4.5 V GND on other inputs
I_{PD}	V_{CC} Current, Gate On (each gate)		6.1		3.6	6.1		6.1	mA	Inputs high V_{CC} = 5.0 V
	V_{CC} Current, Gate Off (each gate)		1.7		1.07	1.7		1.7		Inputs at gnd V_{CC} = 5.0 V
t_{pd+}	Switching Speed				3.0	13			ns	V_{CC} = 5.0 V, See t_{pd} test circuit
t_{pd-}	Switching Speed				3.0	15			ns	C_L = 15 pF

TYPICAL INPUT AND OUTPUT CHARACTERISTICS 9002, 9003, 9004, 9007 AND 9016

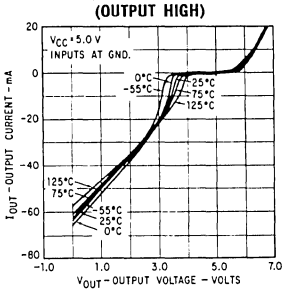
OUTPUT VOLTAGE VERSUS INPUT VOLTAGE



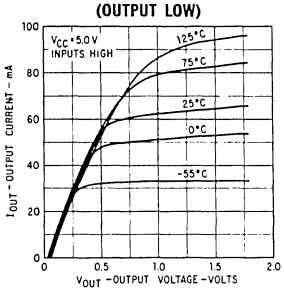
INPUT CURRENT VERSUS INPUT VOLTAGE



OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (OUTPUT HIGH)

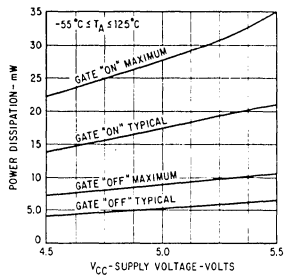


OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (OUTPUT LOW)

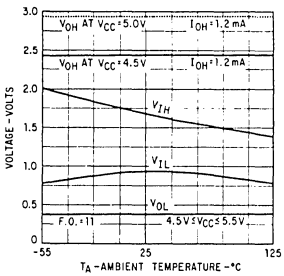


POWER DISSIPATION, LOGIC LEVELS AND NOISE IMMUNITY

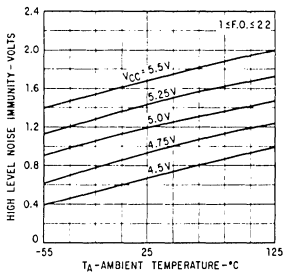
POWER DISSIPATION VERSUS SUPPLY VOLTAGE



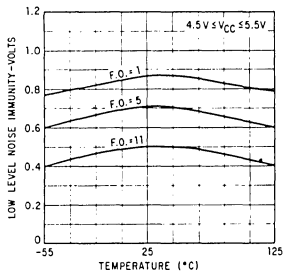
WORST CASE LOGIC LEVELS VERSUS AMBIENT TEMPERATURE



WORST CASE HIGH LEVEL NOISE IMMUNITY VERSUS AMBIENT TEMPERATURE



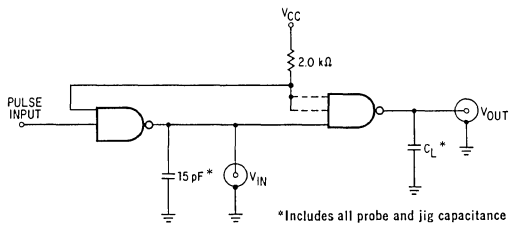
WORST CASE LOW LEVEL NOISE IMMUNITY VERSUS AMBIENT TEMPERATURE



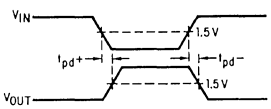
SWITCHING CHARACTERISTICS

f ≃ 1.0 MHz
Amp ≃ 4.0 V
Width ≃ 200 ns
$t_r = t_f \leq 10$ ns

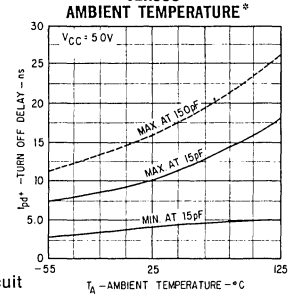
tpd TEST CIRCUIT



SWITCHING WAVEFORM

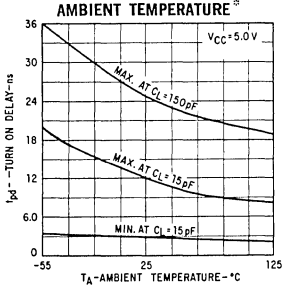


WORST CASE TURN OFF DELAY VERSUS AMBIENT TEMPERATURE*



*See t_{pd} test circuit

WORST CASE TURN ON DELAY VERSUS AMBIENT TEMPERATURE*



NAND BUFFER — 9009

The 9009 is a power gate capable of sinking and sourcing large currents for high fanout applications. Logically it is the same as the 9004.

LOGIC DIAGRAM AND PIN CONFIGURATION
Figure 5

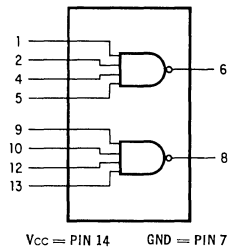
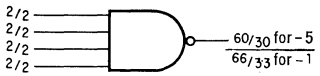
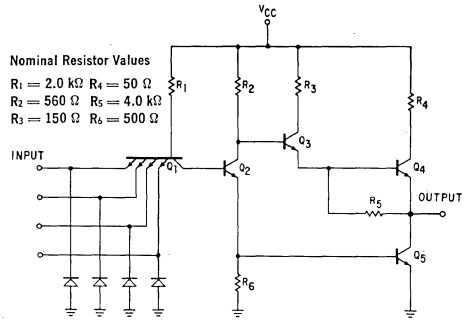


Figure 4 LOADING FACTORS



CIRCUIT DIAGRAM (One Gate)
Figure 6



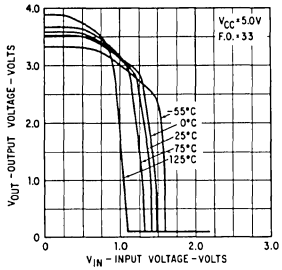
ELECTRICAL CHARACTERISTICS 9009

SYMBOL	CHARACTERISTIC	LIMITS −55°C MIN.	LIMITS −55°C MAX.	LIMITS 25°C MIN.	LIMITS 25°C TYP.	LIMITS 25°C MAX.	LIMITS 125°C MIN.	LIMITS 125°C MAX.	UNITS	CONDITIONS
V_{OH}	Output High Voltage	2.4		2.4	2.7		2.4		Volts	V_{CC} = 4.5 V I_{OH} = −3.96 mA Inputs at V_{IL} (see below)
V_{OL}	Output Low Voltage		0.4		0.21	0.4		0.4	Volts	V_{CC} = 5.5 V I_{OL} = 52.8 mA V_{IH} = 5.5 V
										V_{CC} = 4.5 V I_{OL} = 40.8 mA Inputs at V_{IH} (see below)
V_{IH}	Input High Voltage	2.0		1.7			1.4		Volts	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.8			0.9		0.8	Volts	Guaranteed input low threshold for all inputs
I_F	Input Load Current		3.2		2.15	3.2		3.2	mA	V_{CC} = 5.5 V V_F = 0.4 V
			−2.48		−1.74	−2.48		−2.48		V_{CC} = 4.5 V 5.5 V on other inputs
I_R	Input Leakage Current				20	120		120	μA	V_{CC} = 5.5 V V_R = 4.5 V GND on other inputs
I_{PD}	V_{CC} Current, Gate On (each gate)		12.9		8.6	12.9		12.9	mA	V_{CC} = 5.0 V Inputs high
	V_{CC} Current, Gate Off (each gate)		3.2		2.15	3.2		3.2		V_{CC} = 5.0 V Inputs grounded
t_{pd+}	Switching Speed			4.0		15			ns	V_{CC} = 5.0 V, See t_{pd} test circuit
t_{pd-}	Switching Speed			3.0		10			ns	C_L = 15 pF

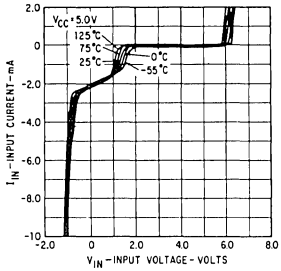
SYMBOL	CHARACTERISTIC	LIMITS 0°C MIN.	LIMITS 0°C MAX.	LIMITS 25°C MIN.	LIMITS 25°C TYP.	LIMITS 25°C MAX.	LIMITS 75°C MIN.	LIMITS 75°C MAX.	UNITS	CONDITIONS
V_{OH}	Output High Voltage	2.4		2.4	2.9		2.4		Volts	V_{CC} = 4.75 V I_{OH} = −3.6 mA Inputs at V_{IL} (see below)
V_{OL}	Output Low Voltage		0.45		0.21	0.45		0.45	Volts	V_{CC} = 5.25 V I_{OL} = 48.0 mA V_{IH} = 5.25 V
										V_{CC} = 4.75 V I_{OL} = 42.3 mA Inputs at V_{IH} (see below)
V_{IH}	Input High Voltage	1.9		1.8			1.6		Volts	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.85			0.85		0.85	Volts	Guaranteed input low threshold for all inputs
I_F	Input Load Current		−3.2		−2.0	−3.2		−3.2	mA	V_{CC} = 5.25 V V_F = 0.45 V
			−2.82		−1.82	−2.82		−2.82		V_{CC} = 4.75 V 5.25 V on other inputs
I_R	Input Leakage Current				20	120		120	μA	V_{CC} = 5.25 V V_R = 4.5 V GND on other inputs
I_{PD}	V_{CC} Current, Gate On (each gate)		14.6		8.6	14.6		14.6	mA	Inputs high V_{CC} = 5.0 V
	V_{CC} Current, Gate Off (each gate)		3.4		2.15	3.4		3.4		Inputs at gnd V_{CC} = 5.0 V
t_{pd+}	Switching Speed			3.0		17			ns	V_{CC} = 5.0 V, See t_{pd} test circuit
t_{pd-}	Switching Speed			2.0		13			ns	C_L = 15 pF

TYPICAL INPUT AND OUTPUT CHARACTERISTICS 9009

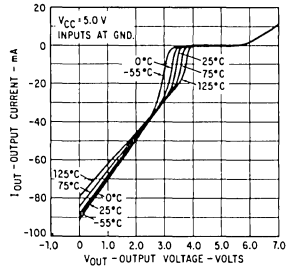
OUTPUT VOLTAGE VERSUS INPUT VOLTAGE



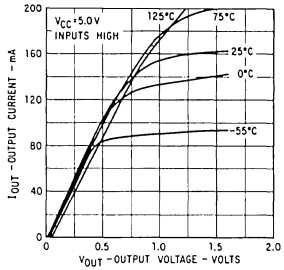
INPUT CURRENT VERSUS INPUT VOLTAGE



OUTPUT CURRENT VERSUS OUTPUT VOLTAGE

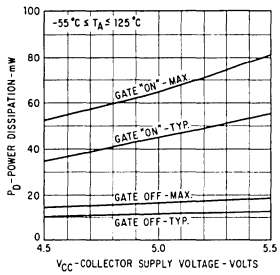


OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (OUTPUT LOW)

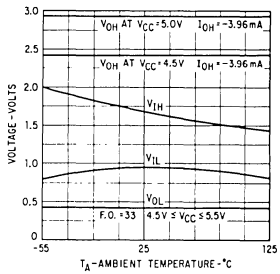


POWER DISSIPATION, LOGIC LEVELS AND NOISE IMMUNITY

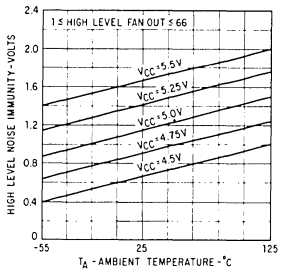
POWER DISSIPATION VERSUS SUPPLY VOLTAGE



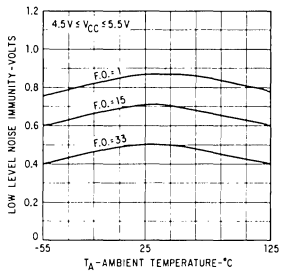
WORST CASE LOGIC LEVELS VERSUS AMBIENT TEMPERATURE



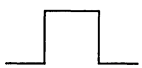
WORST CASE HIGH LEVEL NOISE IMMUNITY VERSUS AMBIENT TEMPERATURE



WORST CASE LOW LEVEL NOISE IMMUNITY VERSUS AMBIENT TEMPERATURE

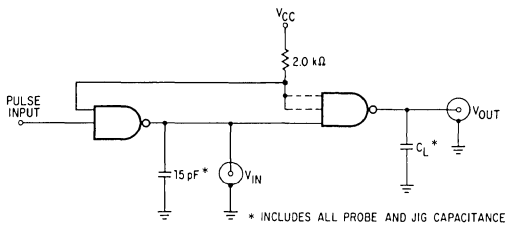


SWITCHING CHARACTERISTICS

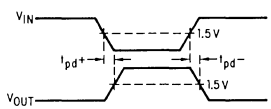


f ≃ 1.0 MHz
Amp ≃ 4.0 V
Width ≃ 200 ns
$t_r = t_f \leq 10$ ns

tpd TEST CIRCUIT

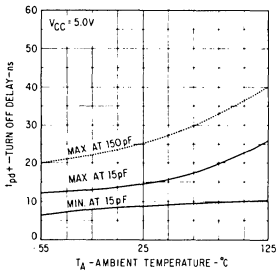


SWITCHING WAVEFORM

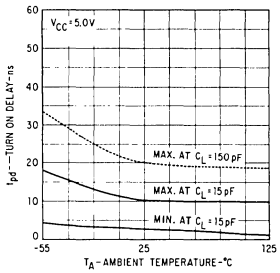


9009-1

WORST CASE TURN OFF DELAY VERSUS AMBIENT TEMPERATURE*

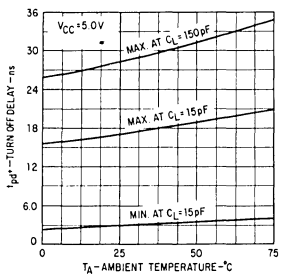


WORST CASE TURN ON DELAY VERSUS AMBIENT TEMPERATURE

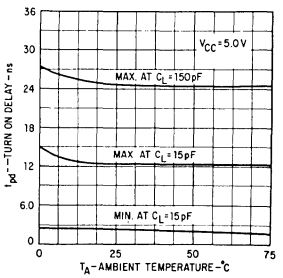


9009-5

WORST CASE TURN OFF DELAY VERSUS AMBIENT TEMPERATURE*



WORST CASE TURN ON DELAY VERSUS AMBIENT TEMPERATURE*



* See t_{pd} test circuit.

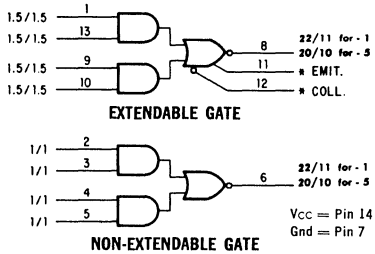
EXTENDABLE AND-OR-INVERT GATES — 9005, 9008
EXTENDER — 9006

The TTL 9005 and 9008 are AND-OR-INVERT gates which may be OR extended with the use of the 9006. For noise immunity and operating level curves, refer to the gate section.

LOGIC DIAGRAMS AND LOADING FACTORS

The numbers by each input and output give the input loading and output drive capability. For complete explanation see Page 2 and 3.

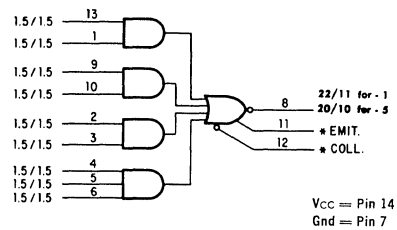
9005



V_{CC} = Pin 14
Gnd = Pin 7

*Four Extenders (9006) may be tied to these terminals

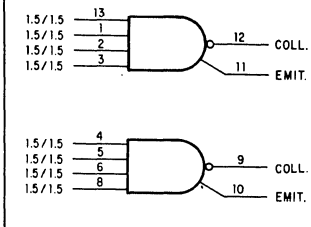
9008



V_{CC} = Pin 14
Gnd = Pin 7

*Four Extenders (9006) may be tied to these terminals

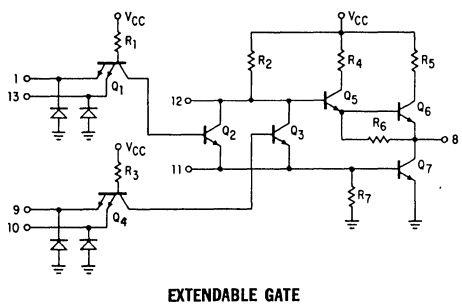
9006

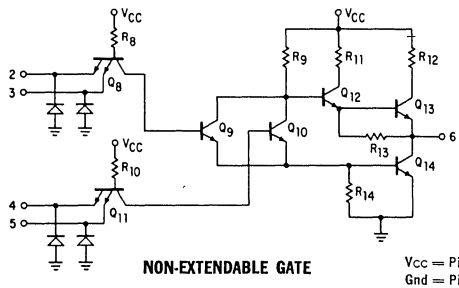


V_{CC} = Pin 14
Gnd = Pin 7

CIRCUIT DIAGRAMS

9005



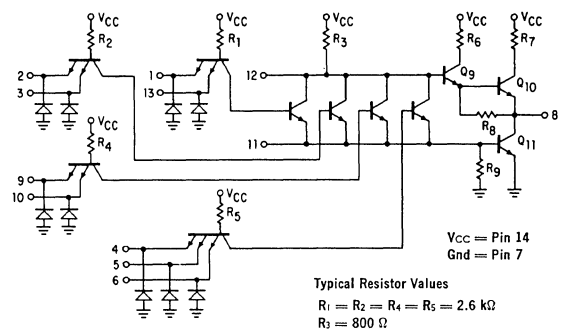


V_{CC} = Pin 14
Gnd = Pin 7

Typical Resistor Values

$R_1 = R_3 = 2.6\ k\Omega$
$R_2 = 800\ \Omega$
$R_4 = R_{11} = 150\ \Omega$
$R_5 = R_{12} = 80\ \Omega$
$R_6 = R_8 = R_{10} = R_{13} = 4.0\ k\Omega$
$R_7 = 665\ \Omega$
$R_9 = 1.5\ k\Omega$
$R_{14} = 1.25\ k\Omega$

9008

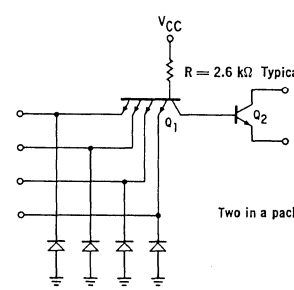


V_{CC} = Pin 14
Gnd = Pin 7

Typical Resistor Values

$R_1 = R_2 = R_4 = R_5 = 2.6\ k\Omega$
$R_3 = 800\ \Omega$
$R_6 = 150\ \Omega$
$R_7 = 80\ \Omega$
$R_8 = 4.0\ k\Omega$
$R_9 = 665\ \Omega$

9006



V_{CC} = Pin 14
Gnd = Pin 7

ELECTRICAL CHARACTERISTICS 9005, 9006 AND 9008 ($T_A = -55°C$ to $125°C$, $V_{CC} = 5.0\ V \pm 10\%$)

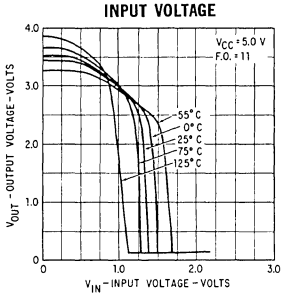
SYMBOL	CHARACTERISTIC	LIMITS −55°C MIN.	LIMITS −55°C MAX.	LIMITS 25°C MIN.	LIMITS 25°C TYP.	LIMITS 25°C MAX.	LIMITS 125°C MIN.	LIMITS 125°C MAX.	UNITS	CONDITIONS & COMMENTS	
V_{OH}	Output High Voltage	2.4		2.4	2.7		2.4		Volts	$V_{CC} = 4.5\ V$ $I_{OH} = -1.32$ mA; V_{IL} = value indicated below on this table	
V_{OL}	Output Low Voltage		0.4		0.2	0.4		0.4	Volts	$V_{CC} = 5.5\ V$ $I_{OL} = 17.6$ mA; $V_{IH} = 5.5\ V$	
										$V_{CC} = 4.5\ V$ $I_{OL} = 13.6$ mA; V_{IH} = (see below)	
V_{IH}	Input High Voltage	2.0		1.7			1.4		Volts	Guaranteed input high threshold for all inputs	
V_{IL}	Input Low Voltage		0.8			0.9		0.8	Volts	Guaranteed input low threshold for all inputs	
I_F	Input Load Current		−1.6		−1.1	−1.6		−1.6	mA	$V_{CC} = 5.5\ V$	$V_F = 0.4\ V$, 5.5 V on other inputs
	9005 Non-Extendable Gate		−1.24		−0.87	−1.24		−1.24		$V_{CC} = 4.5\ V$	
	Input Load Current		−2.4		−1.5	−2.4		−2.4	μA	$V_{CC} = 5.5\ V$	
	Extendable Gate and Extender		−1.86		−1.31	−1.86		−1.86		$V_{CC} = 4.5\ V$	
I_R	Input Leakage Current 9005 Non-Extendable Gate				5.0	60		60	mA	$V_{CC} = 5.5\ V$ $V_R = 4.5\ V$	Gnd on all other inputs
	Input Leakage Current Extendable Gate and Extender				7.5	90		90			
I_{PD}	V_{CC} Current, Gate "ON" 9005 Non-Extendable Gate		6.5		4.5	6.5		6.5	mA	$V_{CC} = 5.0\ V$	All inputs open
	9005 Extendable Gate		11.3		7.6	11.3		11.3			
	9008		12.5		9.3	12.5		12.5			
	V_{CC} Current, Gate "OFF" 9005 Non-Extendable Gate		3.1		2.1	3.1		3.1	mA	$V_{CC} = 5.0\ V$	All inputs except extender inputs gnd.
	9005 Extendable Gate		4.7		3.3	4.7		4.7			
	9008		9.4		6.6	9.4		9.4			
$\triangle I_{PD}$	Extra Current Drain from one 9006 Extender Gate "ON"		1.61		1.08	1.61		1.61	mA	$V_{CC} = 5.0\ V$ All inputs high 9006 attached to a 9005	
	Extra Current Drain from one 9006 Extender Gate "OFF"		2.35		1.65	2.35		2.35	mA	$V_{CC} = 5.0\ V$ All inputs grounded 9006 attached to a 9005	

Note: Output characteristics apply to a 9005 (both gates) or a 9008.
Input characteristics apply to a 9005 (both gates) or a 9008 using either the internal gates or an external 9006 extender.

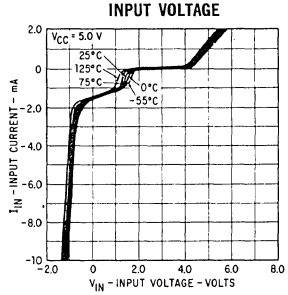
9005, 9006, 9008
TYPICAL INPUT-OUTPUT CHARACTERISTICS

(EXTENDABLE GATES*)

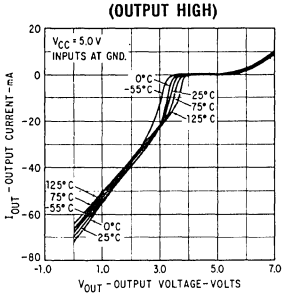
OUTPUT VOLTAGE VERSUS INPUT VOLTAGE



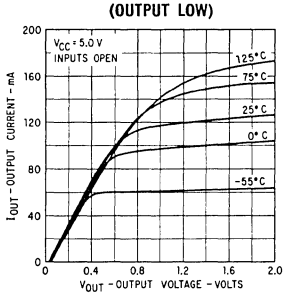
INPUT CURRENT VERSUS INPUT VOLTAGE



OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (OUTPUT HIGH)



OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (OUTPUT LOW)



*Curves on Page 6 apply to 9005 nonextendable gate.

ELECTRICAL CHARACTERISTICS 9005, 9006 AND 9008 ($T_A = 0°C$ to $75°C$, $V_{CC} = 5.0\ V \pm 5\%$)

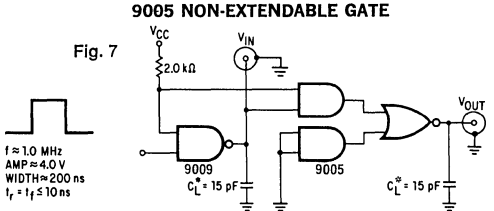
SYMBOL	CHARACTERISTIC	LIMITS 0°C MIN.	LIMITS 0°C MAX.	LIMITS 25°C MIN.	LIMITS 25°C TYP.	LIMITS 25°C MAX.	LIMITS 75°C MIN.	LIMITS 75°C MAX.	UNITS	CONDITIONS
V_{OH}	Output High Voltage	2.4		2.4	2.9		2.4		Volts	$V_{CC} = 4.75\ V$, $I_{OH} = -1.2\ mA$; V_{IL} = value indicated below on this table
V_{OL}	Output Low Voltage		0.45		0.2	0.45		0.45	Volts	$V_{CC} = 5.25\ V$, $I_{OL} = 16.0\ mA$; $V_{CC} = 4.75\ V$, $I_{OL} = 14.1\ mA$
V_{IH}	Input High Voltage	1.9		1.8			1.6		Volts	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.85			0.85		0.85	Volts	Guaranteed input low threshold for all inputs
I_F	Input Load Current		−1.6		−1.04	−1.6		−1.6	mA	$V_{CC} = 5.25\ V$
	9005 Non-Extendable Gate		−1.41		−0.79	−1.41		−1.41		$V_{CC} = 4.75\ V$
	Input Load Current		−2.4		−1.56	−2.4		−2.4	mA	$V_{CC} = 5.25\ V$
	9005 Extendable Gates and Extender		−2.12		−1.19	−2.12		−2.12		$V_{CC} = 4.75\ V$
										$V_F = 0.45\ V$, 5.25 V on other inputs
I_R	Input Leakage Current 9005 Non-Extendable Gate				5.0	60		60	μA	$V_R = 4.5\ V$, $V_{CC} = 4.75\ V$, Gnd on all other inputs
	Input Leakage Current Extendable Gates and Extender				7.5	90		90		
I_{PD}	V_{CC} Current, Gate "ON"								mA	$V_{CC} = 5.0\ V$, All inputs open
	9005 Non-Extendable Gate		7.7		4.5	7.7		7.7		
	9005 Extendable Gate		13.6		7.6	13.6		13.6		
	9008		17.7		9.3	17.7		17.7		
	V_{CC} Current, Gate "OFF"								mA	$V_{CC} = 5.0\ V$, All inputs except extender inputs gnd.
	9005 Non-Extendable Gate		3.4		2.2	3.4		3.4		
	9005 Extendable Gate		5.1		3.3	5.1		5.1		
	9008		10.2		6.6	10.2		10.2		
$\triangle I_{PD}$	Extra Current Drain when one 9006 Extender is attached to a 9005 Gate "ON"		2.05		1.08	2.05		2.05	mA	$V_{CC} = 5.0\ V$, All inputs high
	Extra Current Drain when one 9006 Extender is attached to a 9005 Gate "OFF"		2.54		1.65	2.54		2.54	mA	$V_{CC} = 5.0\ V$, All inputs grounded

Note: Output characteristics above apply to a 9005 (both gates) or a 9008.
Input characteristics above apply to a 9005 (both gates) or a 9008 using either the internal gates or an external 9006 extender.

AC CHARACTERISTICS tpd TEST CIRCUIT

9005 NON-EXTENDABLE GATE

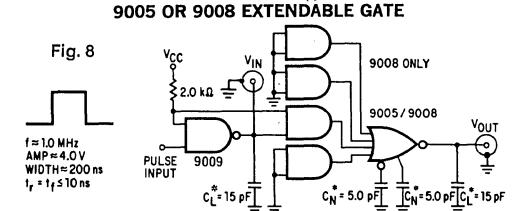
Fig. 7



*Includes all probe and/or jig capacitance.

9005 OR 9008 EXTENDABLE GATE

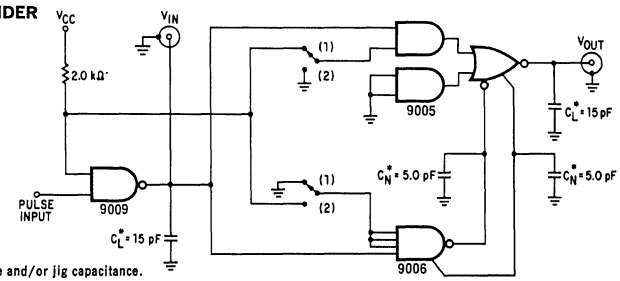
Fig. 8



*Includes all probe and/or jig capacitance.

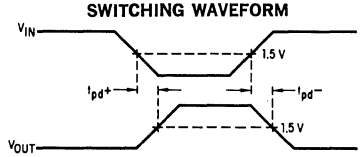
9006 EXTENDER

Fig. 9



*Includes all probe and/or jig capacitance.

SWITCHING WAVEFORM



NOTES:
With switch in position (1) measure tpd of 9005. With switch in position (2) measure tpd (9005) + Δtpd (9006). Capacitances include probe and jig capacitances.

AC CHARACTERISTICS ($T_A = 25°C$) **9005-1, 9006-1, AND 9008-1**

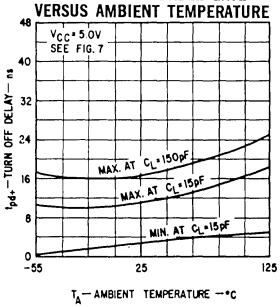
SYMBOL	LIMITS MIN.	LIMITS MAX.	UNITS	CONDITIONS & COMMENTS
t_{pd+}	3.0	15	ns	$V_{CC} = 5.0$ V, $C_L = 15$ pF
t_{pd-}	3.0	15		9005 Nonextendable gate only, See Fig. 7
t_{pd+}	3.0	18	ns	$V_{CC} = 5.0$ V, $C_L = 15$ pF, $C_N = 5.0$ pF
t_{pd-}	3.0	13		9005 Extendable gate and 9008, See Fig. 8
Δt_{pd+}	−3.0	5.0	ns	9006 only
Δt_{pd-}	−3.0	5.0		The 9006 is tested by measuring its propagation time through the 9005. The t_{pd} readings shall not exceed the 9005 readings by the specified amount. See Fig. 9.
Symbols are defined in the test circuit.				

AC CHARACTERISTICS ($T_A = 25°C$) **9005-5, 9006-5, AND 9008-5**

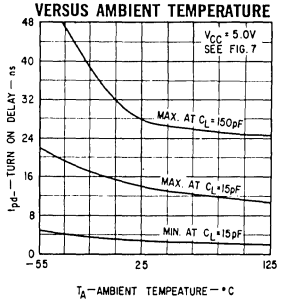
SYMBOL	LIMITS MIN.	LIMITS MAX.	UNITS	CONDITIONS & COMMENTS
t_{pd+}	3.0	12	ns	$V_{CC} = 5.0$ V, $C_L = 15$ pF
t_{pd-}	3.0	14		9005 Nonextendable gate only, See Fig. 7
t_{pd+}	3.0	15	ns	$V_{CC} = 5.0$ V, $C_L = 15$ pF, $C_N = 5.0$ pF
t_{pd-}	3.0	12		9005 Extendable gate and 9008, See Fig. 8
Δt_{pd+}	−2.0	4.0	ns	9006 only
Δt_{pd-}	−2.0	4.0		The 9006 is tested by measuring its propagation time through the 9005. The t_{pd} readings shall not exceed the 9005 readings by the specified amount. See Fig. 9.
Symbols are defined in the test circuit.				

9005-1, 9006-1 AND 9008-1

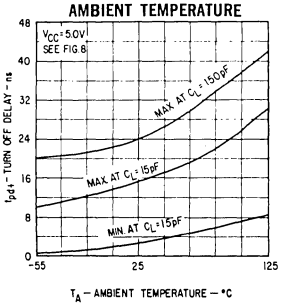
WORST CASE TURN OFF DELAY OF NONEXTENDABLE GATE VERSUS AMBIENT TEMPERATURE



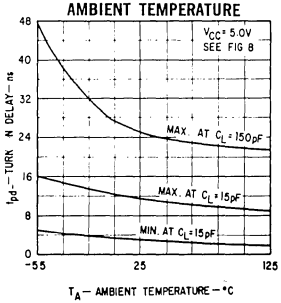
WORST CASE TURN ON DELAY OF NONEXTENDABLE GATE VERSUS AMBIENT TEMPERATURE



WORST CASE TURN OFF DELAY OF EXTENDABLE GATE VERSUS AMBIENT TEMPERATURE



WORST CASE TURN ON DELAY OF EXTENDABLE GATE VERSUS AMBIENT TEMPERATURE



J-K FLIP-FLOPS — 9000, 9001, DUAL J-K FLIP-FLOPS — 9020, 9022

The TTL 9000 series has four flip-flops to satisfy the storage requirements of a logic system. All are master-slave JK designs and have the same high speed and high noise immunity as the rest of the 9000 series. As with the gates, all inputs have diode clamps to further enhance the noise immunity.

The JK type flip-flop was chosen for all flip-flop elements in this family because of its inherent logic power. The input function required to produce a given sequency of states for a JK flip-flop will, in general, contain more "don't care" conditions than the corresponding function for an RS flip-flop. These additional "don't care" conditions will, in most cases, reduce the amount of gating elements required to implement the input function.

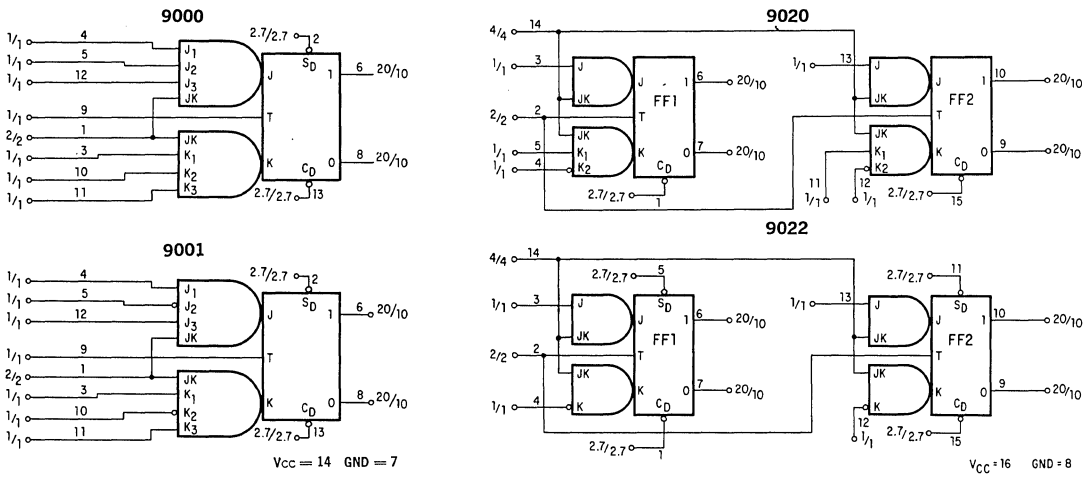
The master-slave design offers the advantage of a DC threshold on the clock input initiating the transition of the outputs, so that careful control of clock pulse rise and fall times is not required.

Data is accepted by the master while the clock is in the low state. Refer to the truth table for definition of "ONE" and "ZERO" data. Transfer from the master to the slave occurs on the low to high transition of the clock. When the clock is high, the J and K inputs are inhibited.

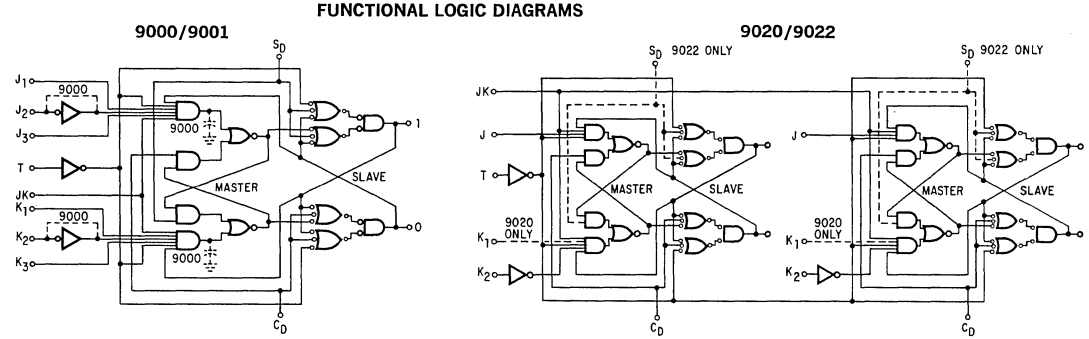
A joint (JK) input is provided for all flip-flops in this family. This common input removes the necessity of gating the clock signal with an external gate in many applications. This not only reduces package count, but also reduces the possibility of clock skew problems, since with internal gating provided, all flip-flops may be driven from a common clock line. Several TTL drivers may be used in parallel to drive this common clock line, if the load exceeds the F.O. capability of the 9009 buffer.

The asynchronous inputs provide ability to control the state of the flip-flop independent of static conditions of the clock and synchronous inputs. Both asynchronous set and clear are provided on all flip-flops except the 9020, which because of a logic trade-off has only clear inputs. The set or clear pin being low absolutely guarantees that one output will be high, but if opposing data is present at the synchronous inputs and the flip-flop is clocked, the low output may momentarily spike high synchronous with a positive transition of the clock. If the low output of the flip-flop is connected to other flip-flop inputs clocked from the same line, the spike will be masked by the clock. If the clock is suspended during the time when the asynchronous inputs are activated, no spike will occur. When the spikes can cause problems, a simple solution is to common the joint JK inputs with the synchronous set or reset signal.

LOGIC DIAGRAMS AND LOADING FACTORS



FUNCTIONAL LOGIC DIAGRAMS



TRUTH TABLES

SYNCHRONOUS OPERATION

BEFORE CLOCK OUTPUTS		BEFORE CLOCK INPUTS		OUTPUTS AFTER CLOCK	
ONE	ZERO	J	K	ONE	ZERO
L	H	L*	X	L	H
L	H	H*	X	H	L
H	L	X	L*	H	L
H	L	X	H*	L	H

ASYNCHRONOUS OPERATION

INPUTS		OUTPUTS	
S_D	C_D	ONE	ZERO
L	L	H	H
L	H	H	L
H	L	L	H
H	H	Synchronous Inputs Control	

SYNCHRONOUS OPERATION

The truth table defines the next state of the flip-flop after a low-to-high transition of the clock pulse. The next state is a function of the present state and the J and K inputs as shown in the table.

The J and K inputs in the table refer to the basic flip-flop J and K inputs as indicated on the logic diagrams. These internal inputs are for every flip-flop the result of a logic operation on the external J and K inputs. This operation is represented symbolically by AND gates in the logic diagram for each flip-flop. Logic diagrams are in accordance with MIL Standard 806B.

The L* symbol in the J and K input column is defined as meaning that that input does not go high at any time while the clock is low.

The H* symbol in the J or K input column is defined as meaning that the input has been high at some time while the clock was low.

The X symbol indicates that the condition of that input has no effect on the next state of the flip-flop.

The H and L symbols refer to steady state high and low voltage levels, respectively.

UNUSED INPUTS

The 9001, 9020 and 9022 all have active level low synchronous inputs. When not in use they must be grounded. All other unused inputs including asynchronous should be tied high for maximum operating speed. Use one of the methods recommended on Page 3.

ELECTRICAL CHARACTERISTICS 9000, 9001, 9020 AND 9022 ($T_A = -55°C$ to $125°C$, $V_{CC} = 5.0\ V \pm 10\%$)

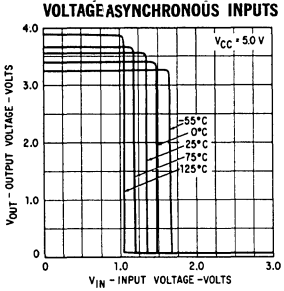
SYMBOL	CHARACTERISTIC	LIMITS −55°C MIN.	LIMITS −55°C MAX.	LIMITS 25°C MIN.	LIMITS 25°C TYP.	LIMITS 25°C MAX.	LIMITS 125°C MIN.	LIMITS 125°C MAX.	UNITS	CONDITIONS & COMMENTS	
V_{OH}	Output High Voltage	2.4		2.4	2.7		2.4		Volts	$V_{CC} = 4.5\ V$, $I_{OH} = -1.2\ mA$	
V_{OL}	Output Low Voltage		0.4		0.21	0.4		0.4	Volts	$V_{CC} = 4.5\ V$, $I_{OL} = 12.4\ mA$ $V_{CC} = 5.5\ V$, $I_{OL} = 16.0\ mA$	
V_{IH}	Input High Voltage	2.0		1.7			1.4		Volts	Guaranteed input high threshold for all inputs	
V_{IL}	Input Low Voltage		0.8			0.9		0.8	Volts	Guaranteed input low threshold for all inputs	
I_R	Input Leakage All J, K inputs T inputs 9000, 9001 JK inputs 9000, 9001 T inputs 9020, 9022 JK inputs 9020, 9022 S_D, C_D (all flip-flops)				5.0 10 20 14	60 120 240 160		60 120 240 160	μA	$V_{CC} = 5.5\ V$ $V_R = 4.5\ V$ Gnd. on other inputs.	
I_F	Input Current All J, K inputs T inputs 9000, 9001 JK inputs 9000, 9001 T inputs 9020, 9022 JK inputs 9020, 9022 S_D, C_D (all flip-flops)		−1.60 −3.20 −6.40 −4.32		−1.1 −2.2 −4.4 −2.97	−1.60 −3.20 −6.40 −4.32		−1.60 −3.20 −6.40 −4.32	mA	$V_{CC} = 5.5\ V$	$V_F = 0.4\ V$ 5.5 V Gnd on other inputs
I_F	Input Current All J, K inputs T inputs 9000, 9001 JK inputs 9000, 9001 T inputs 9020, 9022 JK inputs 9020, 9022 S_D, C_D (all flip-flops)		−1.24 −2.48 −4.96 −3.35		−0.87 −1.74 −3.48 −2.35	−1.24 −2.48 −4.96 −3.75		−1.24 −2.48 −4.96 −3.35	mA	$V_{CC} = 4.5\ V$	
I_{FD}	V_{CC} Current 9000 9001 9020, 9022 each flip-flop		24 28 27		13 14 14	24 28 27		24 28 27	mA	S_D at gnd S_D at gnd C_{D1}, C_{D2} at gnd	$V_{CC} = 5.0\ V$

ELECTRICAL CHARACTERISTICS 9000, 9001, 9020 AND 9022 ($T_A = 0°C$ to $75°C$, $V_{CC} = 5.0\ V \pm 5\%$)

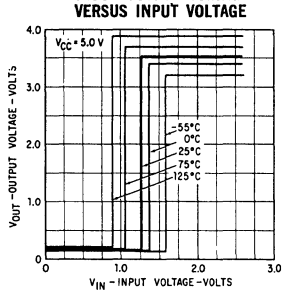
SYMBOL	CHARACTERISTIC	LIMITS 0°C MIN.	LIMITS 0°C MAX.	LIMITS 25°C MIN.	LIMITS 25°C TYP.	LIMITS 25°C MAX.	LIMITS 75°C MIN.	LIMITS 75°C MAX.	UNITS	CONDITIONS & COMMENTS	
V_{OH}	Output High Voltage	2.4		2.4	3.0		2.4		Volts	$V_{CC} = 4.75\ V$, $I_{OH} = -1.2\ mA$	
V_{OL}	Output Low Voltage		0.45		0.21	0.45		0.45	Volts	$V_{CC} = 4.75\ V$, $I_{OL} = 14.1\ mA$ $V_{CC} = 5.25\ V$, $I_{OL} = 16\ mA$	
V_{IH}	Input High Voltage	1.9		1.8			1.6		Volts	Guaranteed input high threshold for all inputs	
V_{IL}	Input Low Voltage		0.85			0.85		0.85	Volts	Guaranteed input low threshold for all inputs	
I_R	Input Leakage All J, K inputs T inputs 9000, 9001 JK inputs 9000, 9001 T inputs 9020, 9022 JK inputs 9020, 9022 S_D, C_D (all flip-flops)				5.0 10 20 14	60 120 240 160		60 120 240 160	μA	VCC = 5.25 V, $V_R = 4.5\ V$ Gnd. on other inputs.	
I_F	Input Current All J, K inputs T inputs 9000, 9001 JK inputs 9000, 9001 T inputs 9020, 9022 JK inputs 9020, 9022 S_D, C_D (all flip-flops)		−1.60 −3.20 −6.40 −4.32		−1.0 −2.0 −4.0 −2.7	−1.60 −3.20 −6.40 −4.32		−1.60 −3.20 −6.40 −4.32	mA	$V_{CC} = 5.25\ V$	$V_F = 0.45\ V$ 5.25 V on other inputs
I_F	Input Current All J, K inputs T inputs 9000, 9001 JK inputs 9000, 9001 T inputs 9020, 9022 JK inputs 9020, 9022 S_D, C_D (all flip-flops)		−1.41 −2.82 −5.64 −3.78		−0.94 −1.88 −3.76 −2.54	−1.41 −2.82 −5.64 −3.78		−1.41 −2.82 −5.64 −3.78	mA	$V_{CC} = 4.75\ V$	
I_{PD}	V_{CC} Current 9000 9001 9020, 9022 each flip-flop		28 33 30			28 33 30		28 33 30	mA	 S_D at gnd S_D at gnd C_{D1}, C_{D2} at gnd	$V_{CC} = 5.0\ V$

TYPICAL INPUT AND OUTPUT CHARACTERISTICS 9000, 9001, 9020 AND 9022

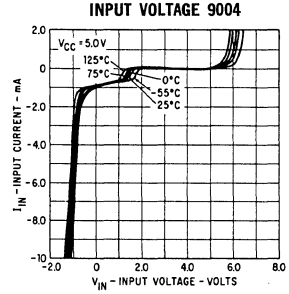
OUTPUT VOLTAGE VERSUS INPUT VOLTAGE ASYNCHRONOUS INPUTS



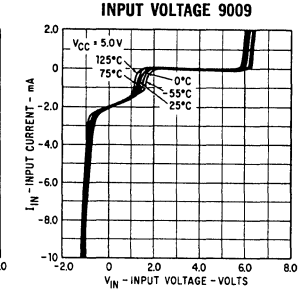
CLOCK OUTPUT VOLTAGE VERSUS INPUT VOLTAGE



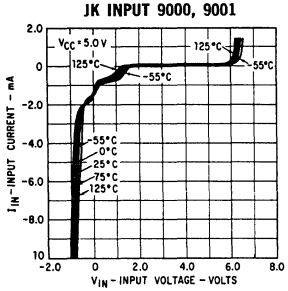
INPUT CURRENT VERSUS INPUT VOLTAGE 9004



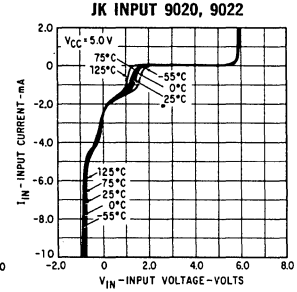
INPUT CURRENT VERSUS INPUT VOLTAGE 9009



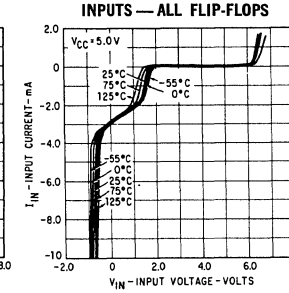
INPUT CURRENT VERSUS INPUT VOLTAGE JK INPUT 9000, 9001



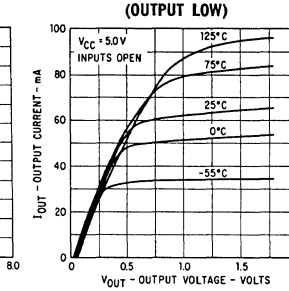
INPUT CURRENT VERSUS INPUT VOLTAGE JK INPUT 9020, 9022



INPUT CURRENT VERSUS INPUT VOLTAGE ASYNCHRONOUS INPUTS — ALL FLIP-FLOPS



OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (OUTPUT LOW)

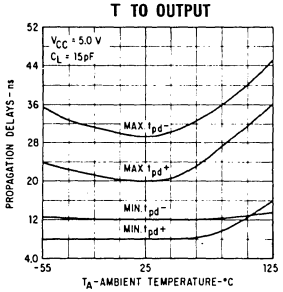


SWITCHING CHARACTERISTICS ($T_A = 25°C$, $V_{CC} = 5.0$ V, $C_L = C_I = 15$ pF of all flip-flops unless otherwise noted)

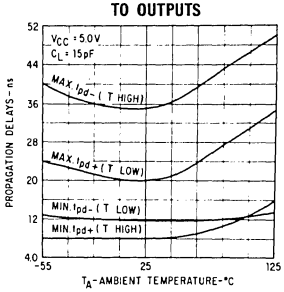
	CHARACTERISTICS			MIN.	TYP.	MAX.	UNITS	FIGURES
t_{pd+}	Clock-to-Output				12	20	ns	10, 11, 12
	S_D or C_D-to-Otuput				12	20	ns	10, 11. 12
t_{pd-}	Clock-to-Output				20	30	ns	10, 11, 12
	S_D or C_D-to-Output				25	35	ns	10, 11. 12
t_{set-up}	J, K or JK		9000 Only	30* 35	22		ns	10, 12
	Data Entry			10* 12	8.0		ns	10, 11, 12
	$\overline{J}$ or $\overline{K}$ Data Entry			17	12		ns	10, 11, 12
$t_{release}$	J, K or JK		9000 Only		18	12	ns	10, 12
	Data Entry				7.0	1.0	ns	10, 11, 12
	$\overline{J}$ or $\overline{K}$ Data Entry				11	4.0	ns	10, 11, 12
Pulse Widths	Clock	9000 Only	Positive		20		ns	10, 12
			Negative		25		ns	10, 12
			Positive		8.0		ns	10, 11, 12
			Negative		10		ns	10, 11, 12
	S_D or C_D		Negative		25		ns	10, 11, 12
Toggle Frequency			9000 Only		20		MHz	10, 12
					50		MHz	10, 11, 12

*For –1 types

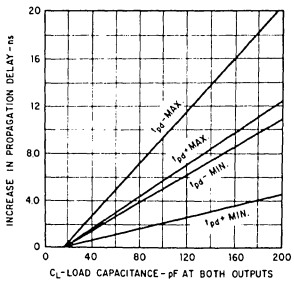
MAX. AND MIN. PROPAGATION DELAYS VERSUS AMBIENT TEMPERATURE T TO OUTPUT



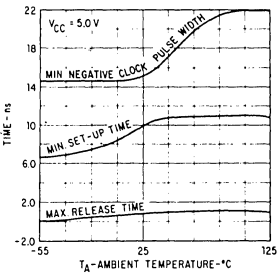
MAX. AND MIN. PROPAGATION DELAYS VERSUS AMBIENT TEMPERATURE ASYNCHRONOUS INPUTS TO OUTPUTS



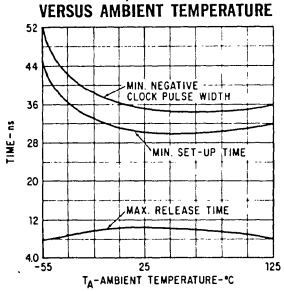
INCREASE IN ASYNCHRONOUS OR CLOCK INPUT DUE TO OUTPUT CAPACITANCE



9001-9020-9022 SET-UP/RELEASE TIME AND NEGATIVE CLOCK PULSE WIDTH VERSUS AMBIENT TEMPERATURE

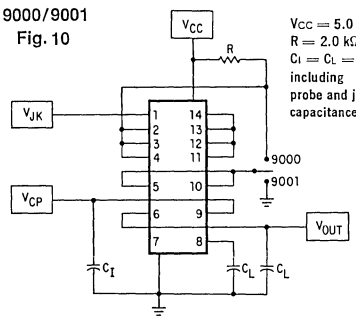


9000 NEGATIVE CLOCK PULSE WIDTH SET-UP/RELEASE TIME VERSUS AMBIENT TEMPERATURE



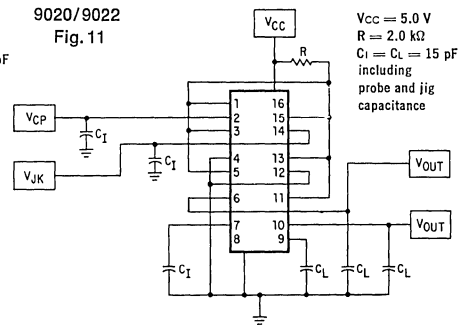
SWITCHING TEST CIRCUITS

9000/9001
Fig. 10



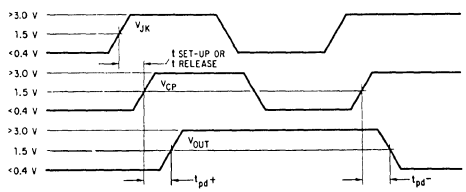
V_{CC} = 5.0 V
R = 2.0 kΩ
$C_I = C_L$ = 15 pF including probe and jig capacitance

9020/9022
Fig. 11



V_{CC} = 5.0 V
R = 2.0 kΩ
$C_I = C_L$ = 15 pF including probe and jig capacitance

WAVEFORMS
Fig.12



SWITCHING TEST NOTES

t_{pd+} and t_{pd-}

1. V_{JK} should be kept at the high logic level when performing t_{pd} tests.
2. Drive the clock pulse input with a suitable pulse source. t_{pd+} and t_{pd-} delays are as defined in the waveforms.

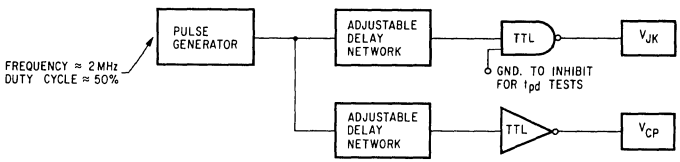
$t_{set\text{-}up}$

1. $t_{set\text{-}up}$ is defined as the minimum time required for a HIGH to be present at a synchronous logic input at any time during the low state of the clock in order for the flip-flop to respond to the data.
2. The test for $t_{set\text{-}up}$ is performed by adjusting the timing relationship between the V_{CP} and V_{JK} inputs to the $t_{set\text{-}up}$ minimum value. A device that passes the test will have the output waveform shown. The output of a device that does not pass the $t_{set\text{-}up}$ test will remain at a static logic level (no switching will occur).

$t_{release}$

1. $t_{release}$ is defined as the maximum time allowed for a HIGH to be present at a synchronous logic input at any time during the low state of the clock and not be recognized.
2. The test for $t_{release}$ is performed by adjusting the timing relationship between V_{CP} and V_{JK} to the $t_{release}$ maximum value. The outputs of devices that pass will remain at static logic levels. In order to check both J and K sides of the flip-flop it is necessary to perform the test with the flip-flop in each of its two possible states, i.e., set and clear. This can be accomplished by making use of the appropriate direct inputs to establish the state before a test. The outputs of devices that do not pass the $t_{release}$ test will exhibit pulses instead of static levels.

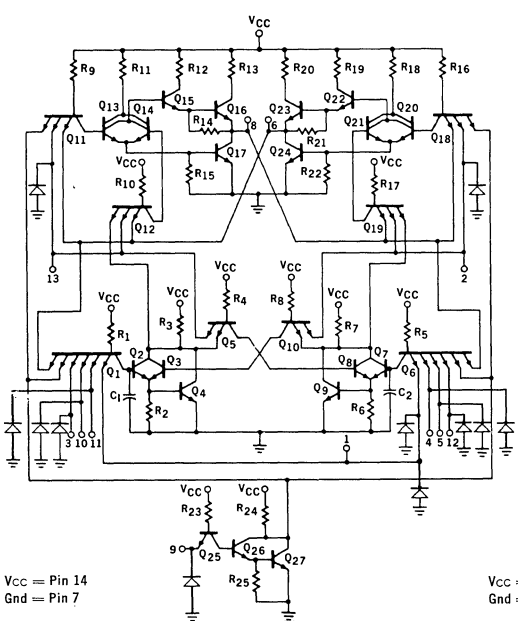
RECOMMENDED INPUT PULSE SOURCES



DTL9932 gates with adjustable capacitors connected from extender inputs to ground make suitable delay elements.

9000 SCHEMATIC DIAGRAM

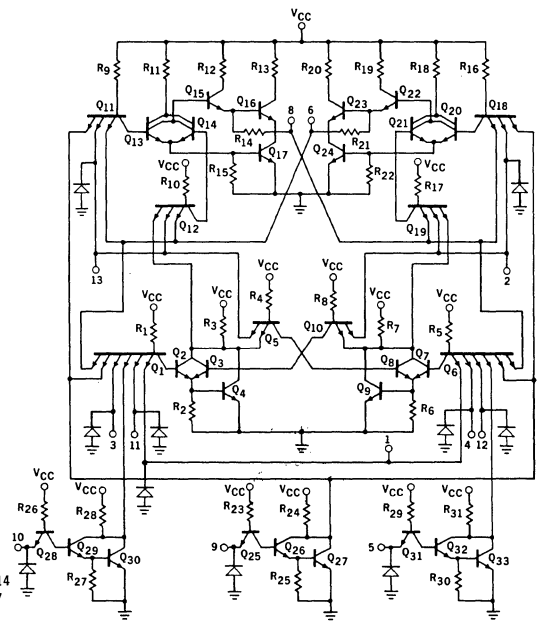
For resistor values, see page 16



V_{CC} = Pin 14
Gnd = Pin 7

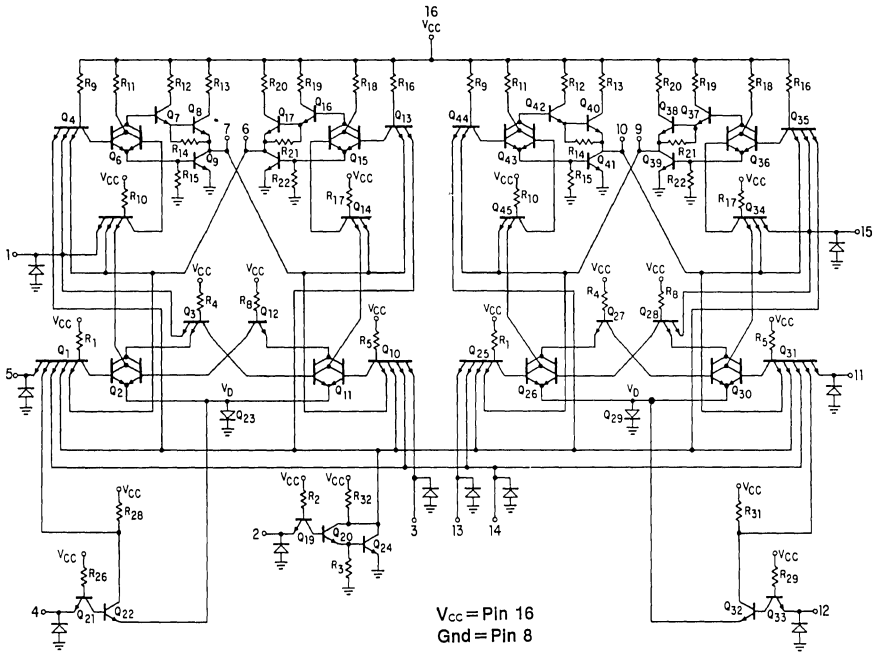
9001 SCHEMATIC DIAGRAM

For resistor values, see page 16



V_{CC} = Pin 14
Gnd = Pin 7

9020 SCHEMATIC DIAGRAM

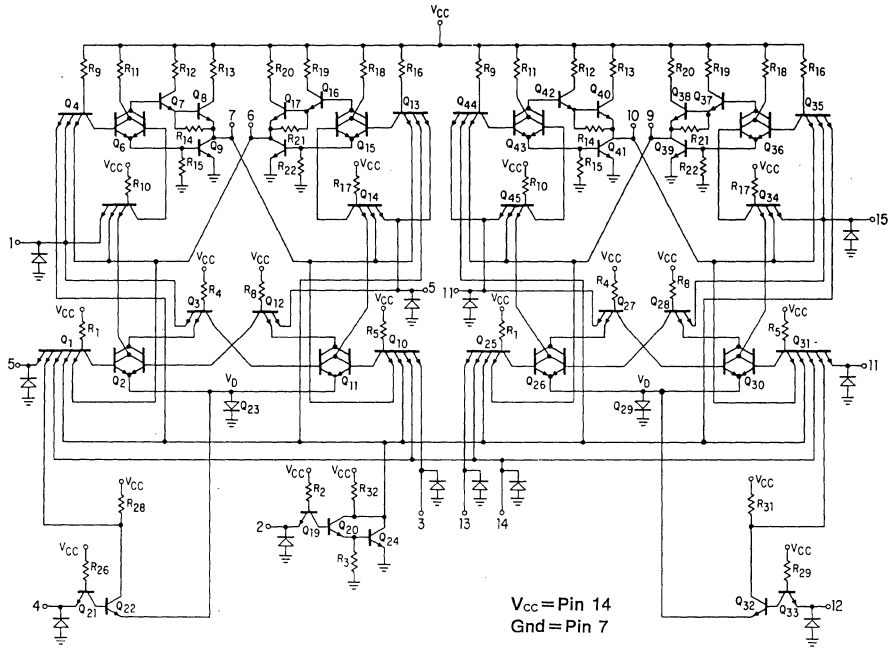


NOMINAL COMPONENT VALUES (ALL FLIP-FLOPS)

R_1, R_4, R_5, R_8, R_{10}, R_{14}, R_{17}, R_{21}, R_{22}, R_{23}, R_{24}, R_{26}, R_{29} = 4.0 kΩ
R_2, R_3, R_6, R_7 = 2.0 kΩ
R_9, R_{16}, R_{28}, R_{31} = 6.0 kΩ
R_{11}, R_{18} = 1.5 kΩ
R_{12}, R_{19} = 150 Ω
R_{13}, R_{20} = 80 Ω
R_{15}, R_{22}, R_{25}, R_{27}, R_{30} = 1.25 kΩ
R_{32} = 1.0 kΩ
C_1, C_2 = 10 pF

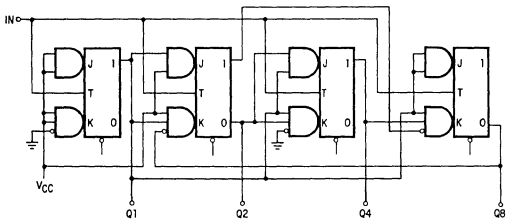
9022 SCHEMATIC DIAGRAM

For resistor values, see table on page



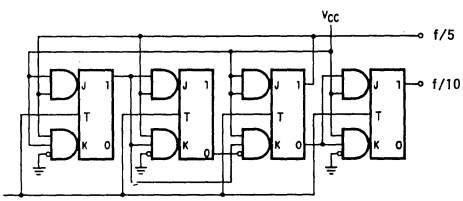
APPLICATIONS

SYNCHRONOUS BCD COUNTER



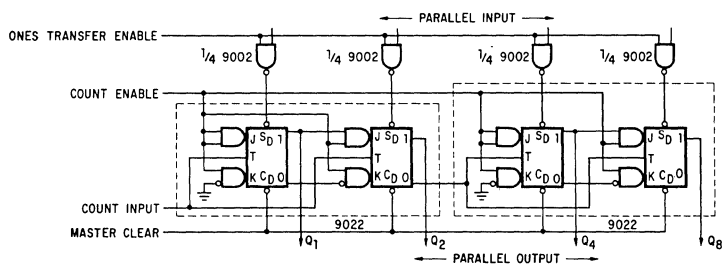
Two TTL 9020 Dual Flip-Flops require no additional gating to produce a fully synchronous 8421 code BCD Counter.

DIVIDE BY TEN COUNTER



Two TTL 9020 Dual Flip-Flops require no additional gating elements to produce divide by ten circuit with a square wave divide by ten output and a divide by five output.

BINARY COUNTER WITH ASYNCHRONOUS PARALLEL LOAD AND CLEAR



Binary counter using synchronous 2 bit stages with trickle down between stages illustrates method of utilizing dual JK flip-flops having common clocks in counter applications.

DUAL J$\overline{K}$ (OR D) FLIP-FLOP

- **Dual Rank Type Circuit**
- **Separate Clocks**
- **Separate Asynchronous Set and Clear Inputs**
- **Low Power Dissipation**
- **Compatible with ITT DTL and Other TTL Families**
- **Input Diode Clamping**
- **25 MHz Operation**

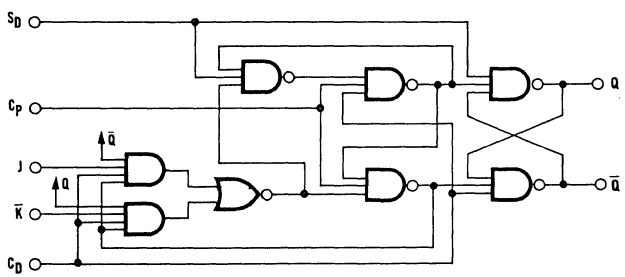
The MIC9024 consists of two high-speed, completely independent transition clocked J$\overline{K}$ flip-flops. The clocking operation is independent of rise and fall times of the clock waveform. The J$\overline{K}$ design allows operation as a D flip-flop by simply connecting the J and $\overline{K}$ pins together.

ABSOLUTE MAXIMUM RATINGS

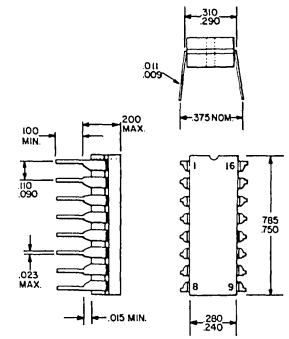
CHARACTERISTICS		UNITS
Storage Temperature	−65 to +150	°C
Temperature (Ambient) Under Bias	−55 to +125	°C
V_{CC} Pin Potential to Ground Pin (See Note 1)	−0.5 to +8	Volts
Voltage applied to output when output is high	0 V to $+V_{CC}$	value
Input Voltage (DC) (See Note 2)	−0.5 to +5.5	Volts
Input Current (DC) (See Note 2)	−30 to +5	mA
Current into output when output is low	+30	mA

Notes 1 and 2 following page

LOGIC DIAGRAM

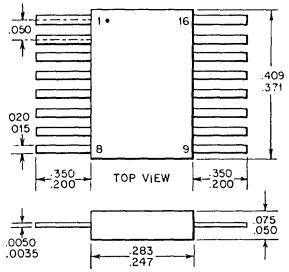


DIMENSIONS — DUAL IN-LINE

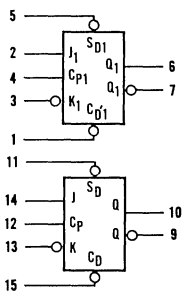


Leads are intended for insertion in hole rows on .300" centers. They are purposely shipped with "positive" (.375) misalignment to facilitate insertion.

DIMENSIONS — FLAT PACK



LOGIC SYMBOL



*ELECTRICAL CHARACTERISTICS ($T_A = 0°C$ to $75°C$, $V_{CC} = 5\ V \pm 5\%$) (Note 3)

SYMBOL	CHARACTERISTIC	LIMITS 0°C MIN.	LIMITS 0°C MAX.	LIMITS 25°C MIN.	LIMITS 25°C TYP.	LIMITS 25°C MAX.	LIMITS 75°C MIN.	LIMITS 75°C MAX.	UNITS	CONDITIONS AND COMMENTS
V_{OH}	Output High Voltage	2.4		2.4	3.0		2.4		Volts	$V_{CC} = 4.75\ V$, $I_{OH} = -1.2\ mA$
V_{OL}	Output Low Voltage		0.45		0.21	0.45		0.45	Volts	$V_{CC} = 4.75\ V$, $I_{OL} = 14.1\ mA$ $V_{CC} = 5.25\ V$, $I_{OL} = 16\ mA$
V_{IH}	Input High Voltage	1.9		1.8			1.6		Volts	Guaranteed input high threshold for all inputs. (To Sink I_{OL})
V_{IL}	Input Low Voltage		0.85			0.85		0.85	Volts	Guaranteed input low threshold for all inputs. (For V_{OH} Output)
I_R $2I_R$ $4\ I_R$	J, K Leakage Current Clock Input, S_D C_D				5.0 10 20	60 120 240		60 120 240	μA	$V_{CC} = 5.25\ V$, $V_R = 4.5\ V$ Gnd. on other inputs
I_F $2\ I_F$ $3\ I_F$	J, K Input Current Clock Input, S_D C_D (Note 4)		−1.6 −3.2 −4.8		−1.0 −2.0 −3.0	−1.6 −3.2 −4.8		−1.6 −3.2 −4.8	mA	$V_{CC} = 5.25\ V$ $V_F = 0.45\ V$ 4.5 V on other inputs
I_F $2\ I_F$ $3\ I_F$	J, K Input Current Clock Input, S_D C_D (Note 4)		−1.41 −2.82 −4.23		−0.94 −1.88 −2.82	−1.41 −2.82 −4.23		−1.41 −2.82 −4.23	mA	$V_{CC} = 4.75\ V$
I_{PD}	Current Drain				9.0	14			mA	Per Flip Flop in Worst Logic State
I_{SC}	Output Current				−65				mA	Logic 1 Output Short Circuit

*Pulse tested.

*ELECTRICAL CHARACTERISTICS ($T_A = -55°C$ to $125°C$, $V_{CC} = 5\ V \pm 10\%$) (Note 3)

SYMBOL	CHARACTERISTIC	LIMITS −55°C MIN.	LIMITS −55°C MAX.	LIMITS 25°C MIN.	LIMITS 25°C TYP.	LIMITS 25°C MAX.	LIMITS 125°C MIN.	LIMITS 125°C MAX.	UNITS	CONDITIONS AND COMMENTS
V_{OH}	Output High Voltage	2.4		2.4	2.7		2.4		Volts	$V_{CC} = 4.5\ V$, $I_{OH} = -1.2\ mA$
V_{OL}	Output Low Voltage		0.4 0.4		0.2 0.25	0.4 0.4		0.4 0.4	Volts Volts	$V_{CC} = 4.5\ V$, $I_{OL} = 12.4\ mA$ $V_{CC} = 5.5\ V$, $I_{OL} = 16\ mA$
V_{IH}	Input High Voltage	2.0		1.7			1.4		Volts	Guaranteed input high threshold for all inputs. (To Sink I_{OL})
V_{IL}	Input Low Voltage		0.8			0.9		0.8	Volts	Guaranteed input low threshold for all inputs. (For V_{OH} Output)
I_R $2I_R$ $4\ I_R$	J, K Leakage Current Clock Input, S_D C_D				5.0 10 20	60 120 240		60 120 240	μA	$V_{CC} = 5.5\ V$, $V_R = 4.5\ V$ Gnd. on other inputs
I_F $2\ I_F$ $3\ I_F$	J, K Input Current Clock Input, S_D C_D (Note 4)		−1.6 −3.2 −4.8		−1.1 −2.2 −3.3	−1.6 −3.2 −4.8		−1.6 −3.2 −4.8	mA	$V_{CC} = 5.5\ V$ $V_F = 0.4\ V$ 4.5 V on other inputs
I_F $2\ I_F$ $3\ I_F$	J, K Input Current Clock Input, S_D C_D (Note 4)		−1.24 −2.48 −3.72		−0.91 −1.82 −2.73	−1.24 −2.48 −3.72		−1.24 −2.48 −3.72	mA	$V_{CC} = 4.5\ V$
I_{PD}	Current Drain				9.0	14			mA	Per Flip Flop in Worst Logic State
I_{SC}	Output Current				−65				mA	Logic 1 Output Short Circuit

*Pulse tested.

NOTES:

(1) The maximum V_{CC} value of 8.0 volts is not the primary factor in determining the maximum V_{CC} which may be applied to a number of interconnected devices. The voltage at a high output is approximately 1 V_{BE} below the V_{CC} voltage, so the primary limit on the V_{CC} is that the voltage at any input may not go above 5.5 V unless the current is limited, so this effectively limits the system V_{CC} to approximately 7.0 volts.

(2) Because of the input clamp diodes, excess current can be drawn out of the inputs if the D.C. input voltage is more negative than −0.5 V. The diode is designed to clamp off large negative A.C. swings associated with fast fall times and long lines. This maximum rating is intended only to limit the steady state input voltage and current.

(3) Positive current is into device and negative current is out of device.

(4) Denotes maximum current under normal operation. These currents may increase up to 4 I_F if J, K = Logic 1 and S_D = Logic 0.

TRUTH TABLES

SYNCHRONOUS ENTRY J-K MODE OPERATION

INPUTS AT t_n		OUTPUTS AT t_{n+1}	
J	$\overline{K}$	Q	$\overline{Q}$
L	H	No Change	
L	L	L	H
H	H	H	L
H	L	Toggles	

SYNCHRONOUS ENTRY D MODE OPERATION

INPUTS AT t_n	OUTPUTS AT t_{n+1}	
D	Q	$\overline{Q}$
L	L	H
H	H	L

L = Low Logic Level, H = High Logic Level

ASYNCHRONOUS ENTRY INDEPENDENT OF CLOCK & SYNCHRONOUS INPUTS

INPUTS		OUTPUTS	
S_D 5(11)	C_D 1(15)	Q 6(10)	$\overline{Q}$ 7(9)
L	L	H	H
L	H	H	L
H	L	L	H
H	H	No Change	

LOADING RULES

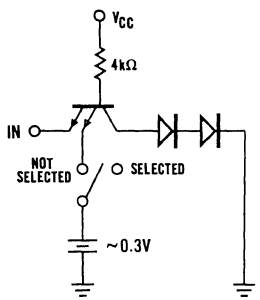
INPUT	LOADING
J and $\overline{K}$	1 U.L.
C_P and S_D	2 U.L.
C_D* (Note 4)	3 U.L.

OUTPUTS	FAN OUT	
	High State	Low State
Q	20	10
$\overline{Q}$	20	10

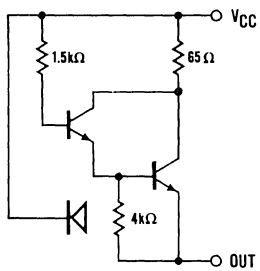
1 U.L. = 1 TTL Unit Load as defined by the entries I_R and I_F tables.

TYPICAL INPUT AND OUTPUT CHARACTERISTICS

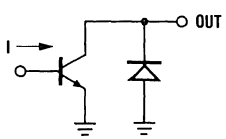
EQUIVALENT INPUT CIRCUIT



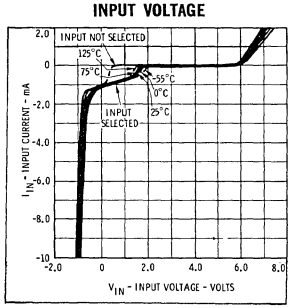
OUTPUT HIGH EQUIVALENT CIRCUIT



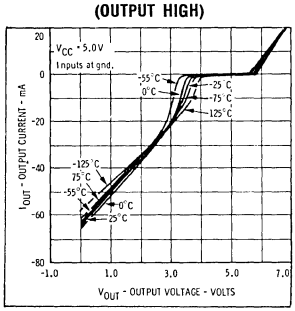
OUTPUT LOW EQUIVALENT CIRCUIT



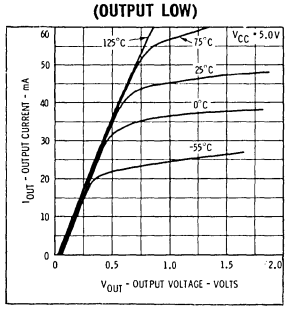
INPUT CURRENT VERSUS INPUT VOLTAGE



OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (OUTPUT HIGH)



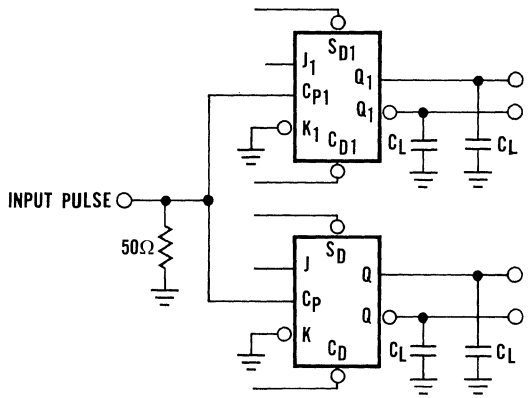
OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (OUTPUT LOW)



SWITCHING CHARACTERISTICS ($T_A = 25°C$, $V_{CC} = 5.0$ V, $C_L = 15$ pF)

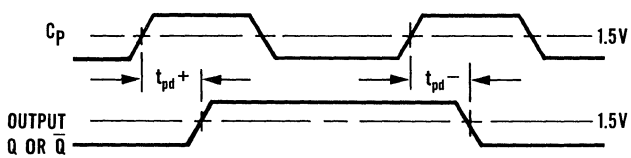
SYMBOL	CHARACTERISTIC	LIMITS 25°C MIN.	TYP.	MAX.	UNITS	COMMENTS
t_{pd+}	J, K, D		25		ns	Each Flip-Flop
t_{pd-}	J, K, D		20		ns	
$t_{release}$			2.0		ns	
$t_{set\text{-}up}$			15		ns	
t_{pd+}	S_D to Q		10		ns	
t_{pd-}	S_D to Q		25		ns	
	Toggle Frequency		25		MHz	

SWITCHING TEST CIRCUIT



C_L includes probe and jig capacitance

WAVEFORMS



SPECIAL ORDERING CODE

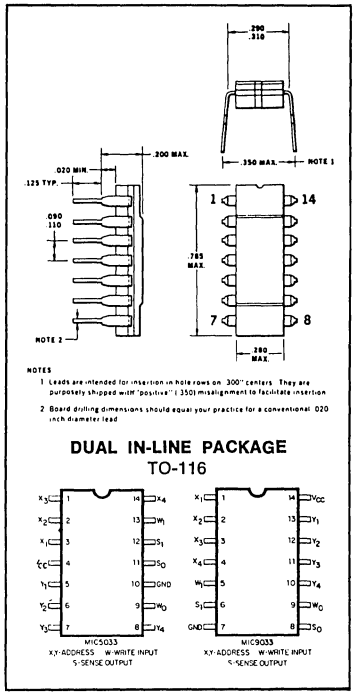
Temperature Range:
1 = −55° to +125°C
5 = 0° to +75°C

Package:
B = .250″ X .250″ Flat Pack
D = Dual In-Line, 16 leads

Example:
MIC9024 - 1B means operating temperature range of −55° to +125°C, supplied in a Flat Pack

16-BIT MEMORY CELL

- **High Speed**
- **Compatible with DTL and TTL Logic**
- **High Noise Immunity, Typically >1 Volt**
- **High Fanout**
- **Low Power Dissipation - 250 mw Typical**



DUAL IN-LINE PACKAGE
TO-116

The MIC 9033/5033 is a Planar epitaxial integrated 16-bit, bit-oriented, non-destructive readout memory cell, compatible with ITT MIC 930 DTL and ITT MIC 9000 TTL digital integrated circuits. This memory cell, organized as 16 word by one bit, is designed for high-speed scratch-pad memory applications.

The memory cells consist of 16 R-S flip-flops arranged in an addressable four-by-four matrix. The desired bit location is selected by raising the coincident X-Y address lines to a logic "1" (typically 3.5 volts) and holding the non-selected address lines at logic "0" (approximately ground). As many as four locations may be addressed simultaneously without destroying stored information. The data and complemented data stored at the addressed bit location may be read at the output terminals. If the addressed bit location contains a "1", the one output (S_1) will be in a low state; zero output (S_0) will be in a high state. Both W_1 and W_0 must be at logic "0" during reading.

Writing is accomplished by activating one of the write amplifiers. To write a "1", the desired bit location is addressed and the input of the "write one" (W_1) amplifier is raised to a logic "1". To write a "0", the input of the "write zero" (W_0) amplifier is raised to a logic "1".

The outputs are open-collector, which may be wire "OR" ed for word expansion. An external resistor should be returned to V_{CC} to pull-up the wire "OR"ed outputs.

ELECTRICAL CHARACTERISTICS

Ratings

SYMBOL	CHARACTERISTIC	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS
V_{CC}	Supply Voltage			7.0	Volts
V_{CC}	Operating Supply Voltage	4.5	5.0	5.5	Volts
	Input Voltage			5.5	Volts
	Output Voltage			5.5	Volts
T_A	Ambient Temperature	0		+75	°C
T_S	Storage Temperature	−65		+150	°C
θ_{J-A}	Thermal Resistance, Junction-to-Ambient:				
	(1) Free Air		120		°C/Watt
	(2) 200 Ft./Min. Air Flow		65		°C/Watt
	(3) 400 Ft./Min. Air Flow		55		°C/Watt
θ_{J-C}	Thermal Resistance, Junction-to-Case		30		°C/Watt
P_D	Power Dissipation		0.25		Watts

SPECIAL ORDERING CODE

Temperature Range:
5 = 0°C to 75°C

Case Style:
Ceramic Dual-In-Line, 14 leads, add "D" following last digit.

Fanout:
40 mA Fanout part numbers:
MIC5033-5D1 or MIC9033-5D1
20 mA Fanout part numbers:
MIC5033-5D2 or MIC9033-5D2

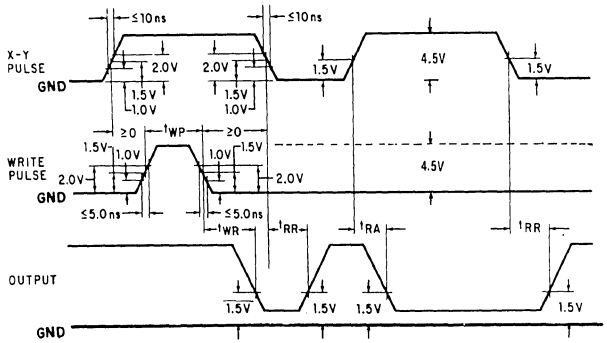
D. C. Characteristics (V_{CC} = 5.0 V, T_A = 0°C to +75°C)

TEST	CHARACTERISTIC	LIMITS MIN.	LIMITS MAX.	UNITS	CONDITIONS
I_{FA}	Address Input Low Current		11	mA	V_{FA} = 0 V
I_{RA}	Address Input High Current		0.4	mA	V_{RA} = 4.5 V
I_{FW}	Write Input Low Current		1.5	mA	V_{FW} = 0 V
I_{RW}	Write Input High Current		0.1	mA	V_{RW} = 4.5 V
V_{IL}	Input Low Voltage		1.0	Volts	
V_{IH}	Input High Voltage	2.1		Volts	
V_{OL}	Output Low Voltage 9033/5033-XX1		0.45	Volts	R_L = 120 Ω to V_{CC}
	9033/5033-XX2		0.45	Volts	R_L = 240 Ω to V_{CC}
I_{OH}	Output Leakage Current		0.1	mA	V_{OH} = V_{CC}
I_{CC}	Power Drain		65	mA	V_{CC} = 5.25 V Inputs Grounded

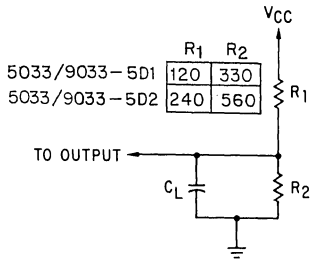
Switching Time Tests (V_{CC} = 5.0 V, T_A = 0°C to +75°C)

TEST	CHARACTERISTIC	LIMITS C_L(pF)	LIMITS MIN.	LIMITS MAX.	UNITS	CONDITIONS
t_{WP}	Write Pulse Width		25		ns	One X-Y location high, all others low, W_O low when checking W_I, W_I low when checking W_O.
t_{WR}	Write Recovery Time	30		35	ns	One X-Y location high, all others low, "1" previously stored when testing S_O, "0" previously stored when checking S_I.
t_{RR}	Read Recovery Time	30		20	ns	One X-Y location switched, all others low, "1" previously stored when testing S_I, "0" previously stored when testing S_O.
t_{RA}	Read Access Time	200		30	ns	
t_{RA}	Read Access Time	30		22	ns	Four X-Y locations switched, all others low, "1"s previously stored when testing S_I, "0"s previously stored when testing S_O.

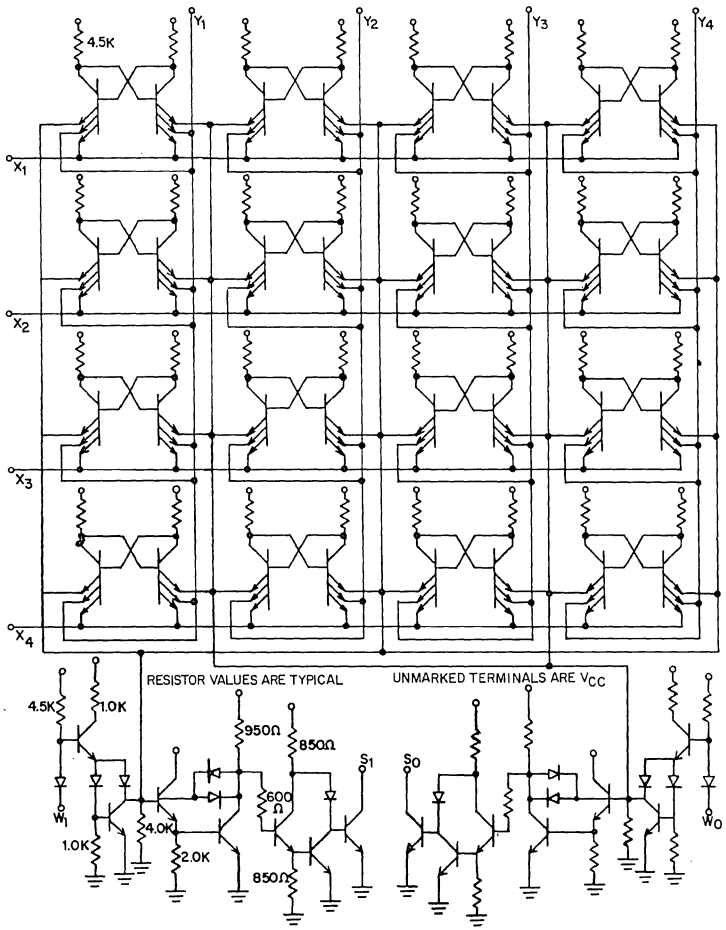
SWITCHING TEST WAVEFORMS



SWITCHING TEST OUTPUT LOAD



CIRCUIT DIAGRAM



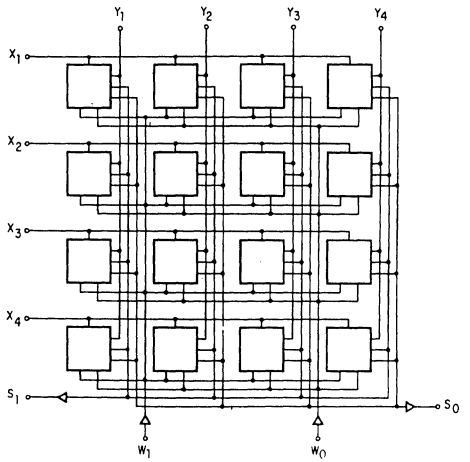
APPLICATIONS

A memory utilizing MIC5033/9033 16-bit memory cells may have any desired word length and the number of words in the memory is a multiple of 16. To illustrate how the MIC5033/9033 may be used to construct a larger memory, the following example is given:

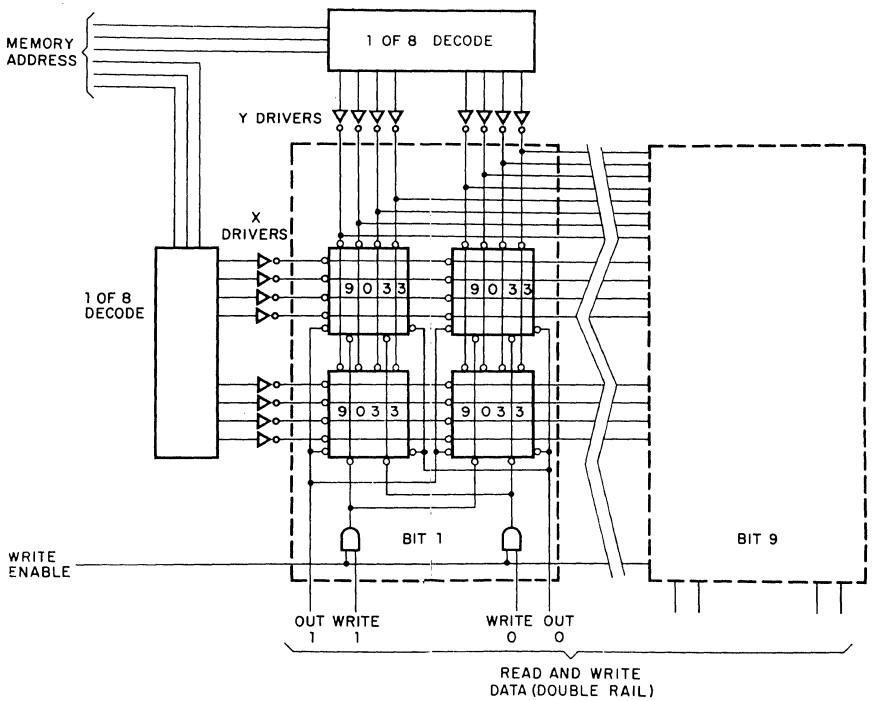
The six memory address lines from an external source may be decoded at the first level with two 1-out-of-8 decoders. Each output of the 1-out-of-8 decoders controls a driving transistor. These driving transistors provide the current necessary to drive eight X and eight Y address lines. Each transistor drives 18 MIC5033/9033 memory cells. The figure below shows the organization of such a memory. The four MIC5033/9033's shown in detail represent 64 words of one bit each. There are nine such groups of four MIC5033/9033's each, each group representing one of the nine bit positions. The 16 address driving transistors drive all nine groups.

The 1-out-of-8 decoder produces one of the eight combinations of three inputs only if the Enable input is at a high logic level. If the Enable input is at a high logic level, one, and only one, of the eight outputs assumes a low logic level. If the Enable input is at a low logic level, all the outputs assume a high logic level. This feature allows the several decoders to be used for memory addressing where the number of words is increased to say 128 or 256.

The example given above is only one of many organizations and is presented as an illustration. Obviously many address decoding schemes may be utilized depending on memory size, driver fan-out, decoder fan-out, wiring, heat dissipation, etc.



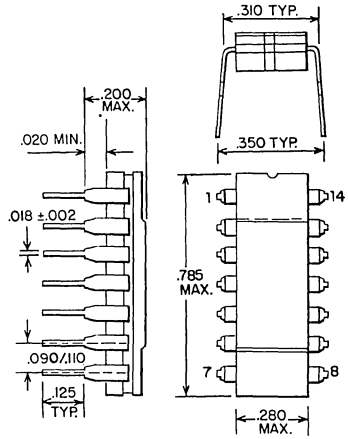
LOGIC DIAGRAM



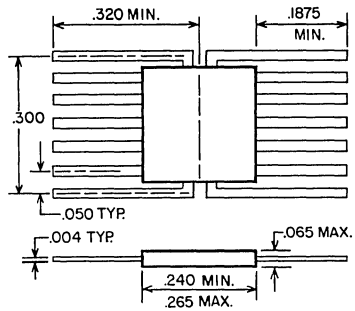
RETRIGGERABLE MONOSTABLE MULTIVIBRATOR TTL

- **Complementary Outputs and Complementary DC level sensitive inputs — insensitive to input pulse transition time.**
- **"Leading edge" or "trailing edge" triggering.**
- **High speed operation — maximum input repetition rate greater than 10 MHz.**
- **High noise immunity — 400 mV worst case.**
- **High fanout — up to 8 TTL loads.**
- **Accurate timing — determined by external R and C — 50 nsec. to ∞ output pulse width range.**
- **Choice of operating mode — inputs can normally allow retriggering, but can also be locked out.**
- **Input diode clamps prevent ringing.**
- **Logic levels are compatible with ITT DTL 930, ITT TTL 9000, MSI and other DTL and TTL families.**
- **Pulse width compensated for V_{CC} and temperature variations.**

DUAL IN-LINE PACKAGE
TO-116



DIMENSIONS — FLAT PACK



The retriggerable monostable multivibrator or one-shot provides an output pulse with high accuracy and a very wide duration range (50 nsec to ∞). It has four DC level-sensitive inputs, two are active-level High and two are active-level Low. Designed for high speed operation, the MIC9601 will respond to trigger inputs even when already in its active timing state, and will time itself out from the last input pulse received.

The unique design of the MIC9601 makes it very useful in applications such as in square-wave and variable delay pulse generators, long delay timers, pulse absence detectors, digital low-pass filters, and even FM demodulators.

ABSOLUTE MAXIMUM RATINGS

CHARACTERISTICS		UNITS
Storage Temperature	−65 to +150	°C
Temperature (Ambient) Under Bias	−55 to +125	°C
V_{CC} Pin Potential to Ground (See Note 1)	−0.5 to +8.0	Volts
Input Voltage (D.C.) (See Note 2)	−0.5 to +5.5	Volts
Input Current (See Note 2)	−30 to +5.0	mA
Voltage Applied to Output When Output is High	0 V to +V_{CC}	value
Current Into Output When Output is Low	50	mA

NOTES:

(1) The maximum V_{CC} value of 8.0 volts is not the primary factor in determining the maximum V_{CC} which may be applied to a number of interconnected devices. The voltage at a high output is approximately 1 V_{BE} below the V_{CC} voltage, so the primary limit on the V_{CC} is that the voltage at any input may not go above 5.5 V unless the current is limited, so this effectively limits the system V_{CC} to approximately 7.0 volts.

(2) Because of the input clamp diodes, excess current can be drawn out of the inputs if the D.C. input voltage is more negative than −0.5 V. The diode is designed to clamp off large negative A.C. swings associated with fast fall times and long lines. This maximum rating is intended only to limit the steady state input voltage and current.

FUNCTIONAL DESCRIPTION

The 9601 monostable multivibrator has four inputs, two of which are active level high and two active level low. This allows a choice of leading edge or trailing edge triggering. The inputs are D.C. coupled making triggering independent of input transition times.

Each time the input conditions for triggering are met, the external capacitor is discharged in a short time and a new cycle is begun. Successive inputs with a period shorter than the delay time retrigger the 9601 and result in a continuous true output. Retriggering may be inhibited by tying the negation (Q) output back to an active level high input.

Active pullups are provided for good drive capability into capacitive loads.

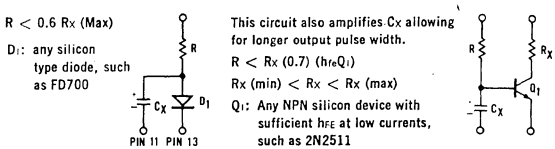
OPERATION RULES

1. An external resistor R_X and an external capacitor C_X are required as shown in the logic diagram. The values of R_X may vary from 5.0 kΩ to 50 kΩ for 0 to +75°C operation, and 5.0 kΩ to 25 kΩ for −55 to +125°C operation. C_X may vary from 0 to any value necessary and obtainable.
2. If a fixed value of R_X is used, the following values are recommended: R_X = 30 kΩ for 0 to +75°C operation; R_X = 10 kΩ for −55 to +125°C operation.
3. The output pulse width T is defined as follows:

   $T = 0.32\ R_XC_X\ [1 + \frac{0.7}{R_X}]$ (For C_X greater than 10^3 pF)

   Where R_X is in kΩ, C_X is in pF, T is in ns

   For $C_X < 10^3$ pF, see Fig. 14
4. If electrolytic type capacitors are to be used, the following two arrangements are recommended:

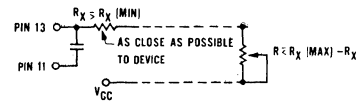


Both circuits prevent reverse voltage across C_X. The pulse width T for the circuits is defined as follows:

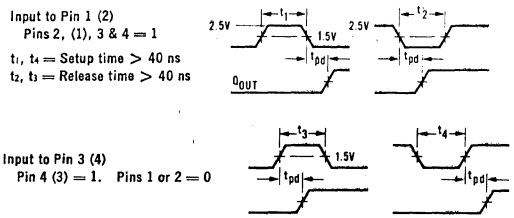
$T \approx 0.36\ RC_X\ [1 + \frac{0.7}{R}]$

Where R is in kΩ, C_X is in pF, T is in ns

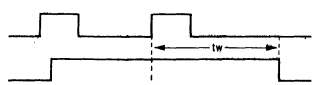
5. To obtain variable pulse width, by remote trimming, the following circuit is recommended:



6. Under any operating condition, C_X and R_X (min) must be kept as close to the circuit as possible to minimize stray capacitance and reduce noise pickup.
7. Input Trigger Pulse Rules.



8. The retrigger pulse width is calculated as shown below:

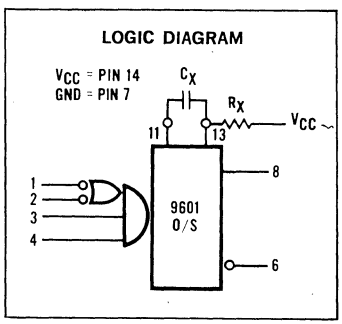


$tw = tpw + tpd+ = 0.32\ RxCx\ (1 + \frac{0.7}{Rx}) + tpd+$

The retrigger pulse width is equal to the pulse width tpw plus a delay time. For pulse widths greater than 500 ns, tw can be approximated as tpw.

NOTE: Retriggering will not occur if the retrigger pulse comes within $.32\ R_XC_X\ (\frac{.7}{R_X})$ ns after the initial trigger pulse.

LOGIC DIAGRAM



SPECIAL ORDERING CODE

Temperature Range:
1 = −55° +125°C
5 = 0° to +75C

Package:
B = .250" X .250" Flat Pack
D = Dual In-Line ,14 leads

Example:
MIC9601- 1B means operating temperature range of −55° to +125°C, supplied in a Flat Pack

ELECTRICAL CHARACTERISTICS ($T_A = -55°C$ to $125°C$, $V_{CC} = 5\ V \pm 10\%$)

SYMBOL	CHARACTERISTIC	LIMITS						UNITS	CONDITIONS (Note 1)
		−55°C		+25°C			+125°C		
		MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.	
V_{OH}	Output High Voltage	2.4		2.4	3.3		2.4		Volts	$V_{CC} = 4.5\ V$, $I_{OH} = -0.72$ mA (Note 2)
V_{OL}	Output Low Voltage		0.4		0.2	0.4		0.4	Volts	$V_{CC} = 4.5\ V$, $I_{OL} = 10$ mA (Note 2)
V_{IH}	Input High Voltage	2.0		1.7			1.4		Volts	$V_{CC} = 4.5\ V$ (Note 3)
V_{IL}	Input Low Voltage		0.85			0.90		0.85	Volts	$V_{CC} = 5.5\ V$ (Note 3)
I_F	Input Load Current		−1.6		−1.1	−1.6		−1.6	mA	$V_{CC} = 5.5\ V$, $V_F = 0.4\ V$
I_R	Input Leakage Current				15	60		60	μA	$V_{CC} = 5.5\ V$, $V_R = 4.5\ V$
I_{SC}	Short Circuit Current			−10		−40			mA	$V_{CC} = 5.0\ V$, $V_{OUT} = 0\ V$ (Note 2)
I_{pd}	Quiescent Power Supply Drain		25			25		25	mA	$V_{CC} = 5.5\ V$
t_{pd+}	Negative Trigger Input to True Output				25	40			ns	$V_{CC} = 5.0\ V$, $R_X = 5.0\ k\Omega$, $C_X = 0$, $C_L = 15$ pF
t_{pd-}	Negative Trigger Input to Complement Output				25	40			ns	$V_{CC} = 5.0\ V$, $R_X = 5.0\ k\Omega$, $C_X = 0$, $C_L = 15$ pF
$t_{pw(min)}$	Minimum True Output Pulse Width				45	65			ns	$V_{CC} = 5.0\ V$, $R_X = 5.0\ k\Omega$, $C_X = 0$, $C_L = 15$ pF
Δt_{pw}	Pulse Width Variation			3.08	3.42	3.76			μsec	$V_{CC} = 5.0\ V$, $R_X = 10\ k\Omega$, $C_X = 1000$ pF
C_{STRAY}	Maximum Allowable Wiring Cap. (Pin 13)		50			50		50	pF	Pin 13 to Ground
R_X	Timing Resistor	5.0	25	5.0		25	5.0	25	kΩ	

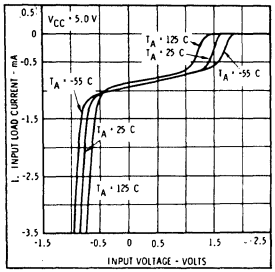
TABLE II — ELECTRICAL CHARACTERISTICS ($T_A = 0°C$ to $75°C$, $V_{CC} = 5\ V \pm 5\%$)

SYMBOL	CHARACTERISTIC	LIMITS						UNITS	CONDITIONS (Note 1)
		0°C		+25°C			+75°C		
		MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.	
V_{OH}	Output High Voltage	2.4		2.4	3.4		2.4		Volts	$V_{CC} = 4.75\ V$, $I_{OH} = -0.96$ mA (Note 2)
V_{OL}	Output Low Voltage		0.45		0.2	0.45		0.45	Volts	$V_{CC} = 4.75\ V$, $I_{OL} = 12.8$ mA (Note 2)
V_{IH}	Input High Voltage	1.9		1.8			1.6		Volts	$V_{CC} = 4.75\ V$ (Note 3)
V_{IL}	Input Low Voltage		.85			0.85		0.85	Volts	$V_{CC} = 5.25\ V$ (Note 3)
I_F	Input Load Current		−1.6		−1.0	−1.6		−1.6	mA	$V_{CC} = 5.25\ V$, $V_F = 0.45\ V$
I_R	Input Leakage Current				15	60		60	μA	$V_{CC} = 5.25\ V$, $V_R = 4.5\ V$
I_{SC}	Short Circuit Current			−10		−40			mA	$V_{CC} = 5.0\ V$, $V_{OUT} = 0\ V$ (Note 2)
I_{pd}	Quiescent Power Supply Drain		25			25		25	mA	$V_{CC} = 5.25\ V$ Ground Pins 1 and 2
t_{pd+}	Negative Trigger Input to True Output				25	40			ns	$V_{CC} = 5.0\ V$, $R_X = 5.0\ k\Omega$, $C_X = 0$, $C_L = 15$ pF
t_{pd-}	Negative Trigger Input to Complement Output				25	40			ns	$V_{CC} = 5.0\ V$, $R_X = 5.0\ k\Omega$, $C_X = 0$, $C_L = 15$ pF
$t_{pw(min)}$	Minimum True Output Pulse Width				45	65			ns	$V_{CC} = 5.0\ V$, $R_X = 5.0\ k\Omega$, $C_X = 0$, $C_L = 15$ pF
Δt_{pw}	Pulse Width Variation			3.08	3.42	3.76			μsec	$V_{CC} = 5.0\ V$, $R_X = 10\ k\Omega$, $C_X = 1000$ pF
C_{STRAY}	Maximum Allowable Wiring Cap. (Pin 13)		50			50		50	pF	Pin 13 to Ground
R_X	Timing Resistor	5.0	50	5.0		50	5.0	50	kΩ	

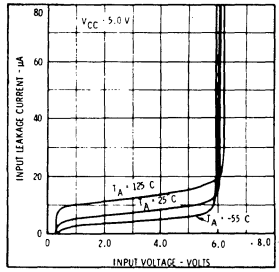
NOTES: (1) Unless otherwise noted, 10 kΩ resistor placed between Pin 13 and V_{CC}, for all tests. (R_X)
(2) Ground Pin 11 for V_{OL} Pin 6 or V_{OH} Pin 8 or I_{SC} Pin 8. Open Pin 11 for V_{OL} Pin 8 or V_{OH} Pin 6 or I_{SC} Pin 6.
(3) Pulse Test to determine V_{IH} and V_{IL} (Min PW 40 ns).

TYPICAL ELECTRICAL CHARACTERISTICS

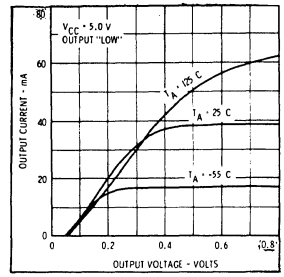
INPUT LOAD CURRENT VERSUS INPUT VOLTAGE



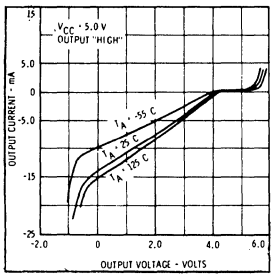
INPUT LEAKAGE CURRENT VERSUS INPUT VOLTAGE



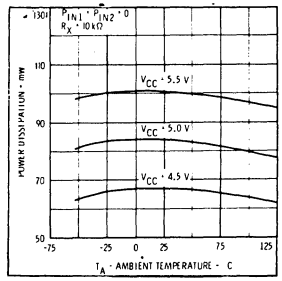
OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (LOW STATE)



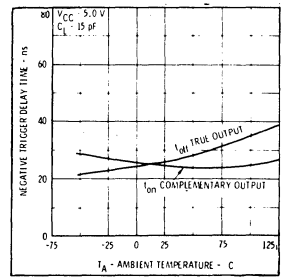
OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (HIGH STATE)



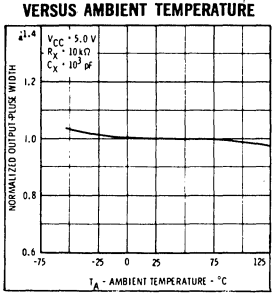
POWER DISSIPATION VERSUS AMBIENT TEMPERATURE



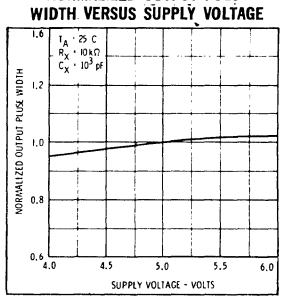
NEGATIVE TRIGGER DELAY TIME VERSUS AMBIENT TEMPERATURE



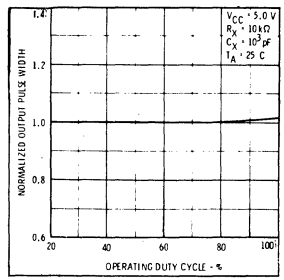
NORMALIZED OUTPUT PULSE WIDTH VERSUS AMBIENT TEMPERATURE



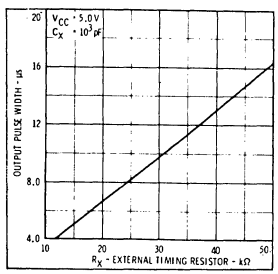
NORMALIZED OUTPUT PULSE WIDTH VERSUS SUPPLY VOLTAGE



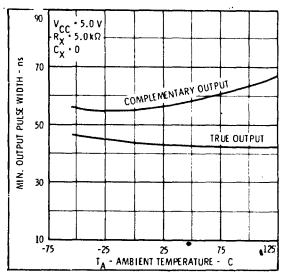
NORMALIZED OUTPUT PULSE WIDTH VERSUS OPERATING DUTY CYCLE



PULSE WIDTH VERSUS TIMING RESISTANCE

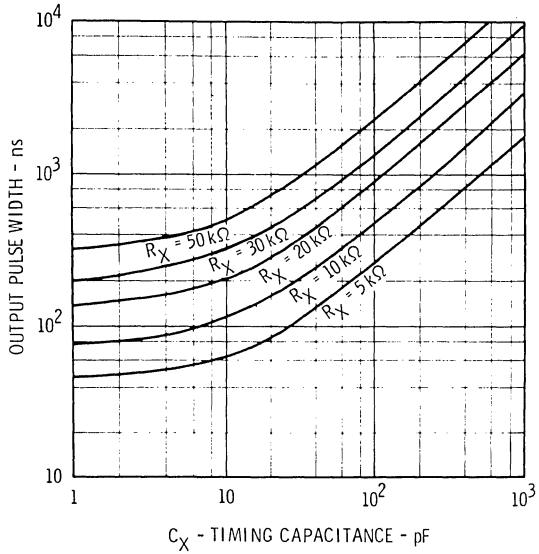


OUTPUT PULSE WIDTH VERSUS AMBIENT TEMPERATURE

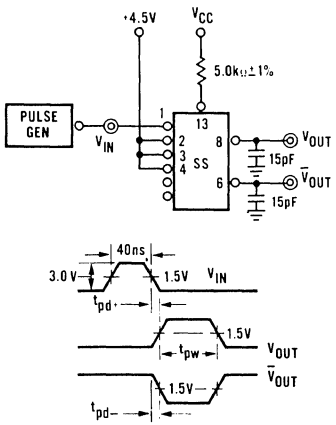


OUTPUT PULSE WIDTH VERSUS TIMING RESISTANCE AND CAPACITANCE

For $C_X < 10^3$ pF (For $C_X \geq 10^3$pF, $t_{pw} = 0.32\ R_X C_X\ (1 + \frac{0.7}{R_X})$



SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



NOTE: Capacitance includes Jig and Probe

LOADING RULES

TTμL INPUT LOAD AND DRIVE FACTORS

−55°C to +125°C

INPUT LEVEL	LOAD FACTOR
High	1
Low	1
OUTPUT STATE	DRIVE FACTOR
High	12
Low	6

0°C to 75°C

INPUT LEVEL	LOAD FACTOR
High	1
Low	1
OUTPUT STATE	DRIVE FACTOR
High	16
Low	8

CCSL INPUT LOAD AND DRIVE FACTORS

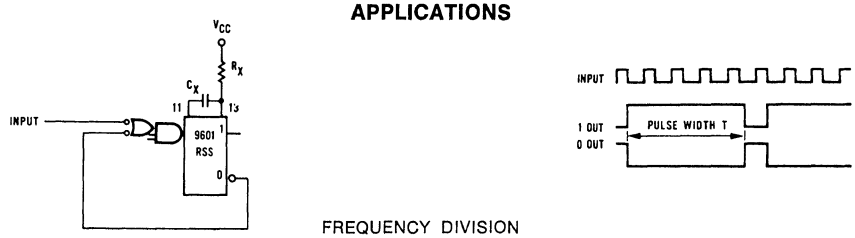
−55°C to +125°C

INPUT LEVEL	LOAD FACTOR
High	12
Low	10
OUTPUT STATE	DRIVE FACTOR
High	144
Low	62

0°C to 75°C

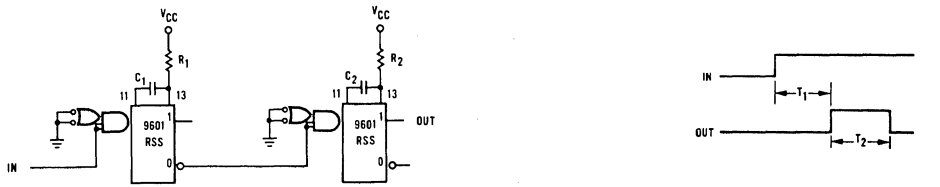
INPUT LEVEL	LOAD FACTOR
High	12
Low	10.5
OUTPUT STATE	DRIVE FACTOR
High	192
Low	85

APPLICATIONS



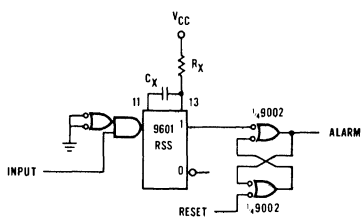
FREQUENCY DIVISION

This configuration makes the 9601 non-retriggerable and capable of frequency division.



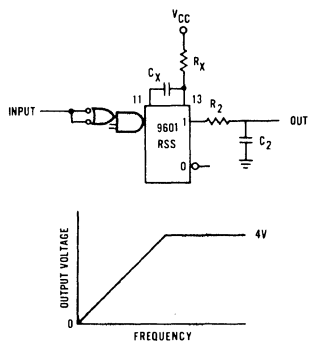
DELAYED PULSE GENERATION

The first 9601 determines the time T_1 before the initiation of the output pulse. The second 9601 determines T_2, the output pulse width.



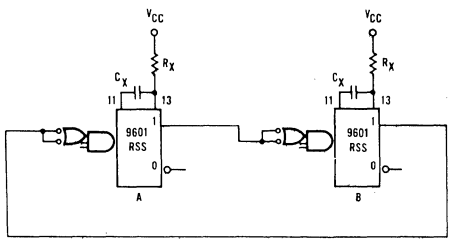
MALFUNCTION INDICATOR

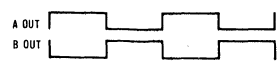
The output of the retriggerable single shot will only remain high if the input frequency is above some fixed value. The input, may be a flip flop which normally has a fixed frequency of operation. A system malfunction is indicated when the flip flop frequency drops and retriggering operation of single shot ceases.



DISCRIMINATOR

The 9601 can be used to produce a voltage output proportional to input frequency. For a fixed TC of R_X and C_X, the duty cycle of the output will vary with frequency. This is integrated by R_2 C_2 producing a voltage proportional to frequency.





ASTABLE MULTIVIBRATOR

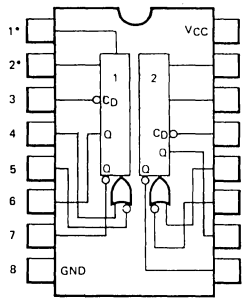
Frequency of operation is dependent upon value of R_X and C_X.

DUAL RETRIGGERABLE RESETTABLE MONOSTABLE MULTIVIBRATOR

The TTL/Monostable 9602 is a dual retriggerable, resettable monostable multivibrator which provides an output pulse whose duration and accuracy is a function of external timing components. The ITT9602 has excellent immunity to noise on the V_{CC} and ground lines. The ITT9602 uses TTL inputs and outputs for high speed and high fanout capability and is compatible with all members of the TTL family.

- **72 ns to ∞ Output Width Range**
- **Retriggerable 0 to 100% Duty Cycle**
- **TTL Input Gating - Leading or Trailing Edge Triggering**
- **Complementary TTL Outputs**
- **Optional Retrigger Lock-Out Capability**
- **Pulse Width Compensated for V_{CC} and Temperature Variations**
- **Resettable**

CONNECTION DIAGRAM
(TOP VIEW)

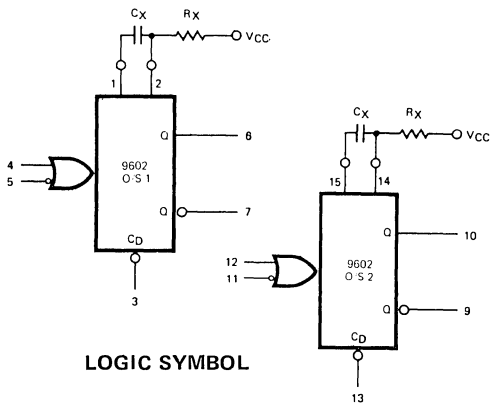


*Pins for external timing

ABSOLUTE MAXIMUM RATINGS

(above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground (See Note 1)	−0.5 V to +8.0 V
Input Voltage (D.C.) (See Note 2)	−0.5 V to +5.5 V
Input Current (See Note 2)	−30 mA to +5.0 mA
Voltage Applied to Output When Output is High	−0.5 V to +V_{CC} value
Current Into Output When Output is Low	50 mA



LOGIC SYMBOL

NOTES:

1. The maximum V_{CC} value of 8.0 volts is not the primary factor in determining the maximum V_{CC} which may be applied to a number of interconnected devices. The voltage at a high output is approximately 1 V_{BE} below the V_{CC} voltage, so the primary limit on the V_{CC} is that the voltage at any input may not go above 5.5 V unless the current is limited. This effectively limits the system V_{CC} to approximately 7.0 volts.
2. Because of the input clamp diodes, excess current can be drawn out of the inputs if the D.C. input voltage is more negative than −0.5 V. The diode is designed to clamp off large negative A.C. swings associated with fast fall times and long lines. This maximum rating is intended only to limit the steady state input voltage and current.

FUNCTIONAL DESCRIPTION

The 9602 dual resettable, retriggerable monostable multivibrator has two inputs per function, one active high and one active low. This allows leading edge or trailing edge triggering. The TTL inputs make triggering independent of input transition times. When input conditions for triggering are met, a new cycle starts and the external capacitor is rapidly discharged and then allowed to charge. An input cycle time shorter than the output cycle time will retrigger the 9602 and result in a continuous true output. (See Rule 9.) The output pulse may be terminated at any time by correcting the reset pin to a low logic level pin. Active pullups are provided on the outputs for good drive capability into the capacitive loads.

OPERATION RULES

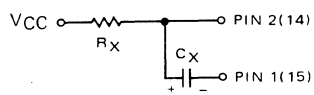
1. An external resistor (R_X) and external capacitor (C_X) are required as shown in the Logic Diagram.
2. The value of R_X may vary from 5.0 to 50 kΩ for 0 to 75°C operation. The value of R_X may vary from 5.0 to 25 kΩ for −55 to +125°C operation.
3. The value of C_X may vary from 0 to any necessary value available. If, however, the capacitor has leakages approaching 3.0 μA or if stray capacitance from either terminal to ground is more than 50 pF, the timing equations may not represent the pulse width obtained.
4. The output pulse with (t) is defined as follows:

$$t = 0.31\ R_X C_X \left[1 + \frac{1}{R_X}\right]$$

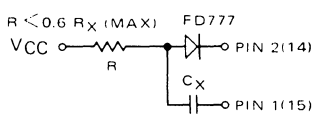
Where R_X is in kΩ
C_X is in pF
t is in ns
for $C_X < 10^3$ pF, see Fig. 17.

5. If electrolytic type capacitors are to be used, the following three configurations are recommended:

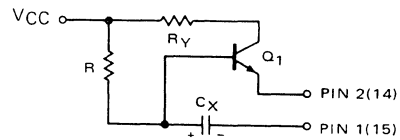
A. Use with low leakage electrolytic capacitors.
The normal RC configuration can be used predictably only if the forward capacitor leakage at 5.0 volts is less than 3 μA, and the inverse capacitor leakage at 1.0 volt is less than 5 μA over the operational temperature range and Rule 3 above is satisfied.



B. Use with high inverse leakage current electrolytic capacitors.
The diode in this configuration prevents high inverse leakage currents through the capacitor by preventing an inverse voltage across the capacitor. The use of this configuration is not recommended with retriggerable operation.



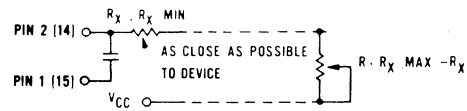
C. Use to obtain extended pulse widths:
$t \approx 0.3\ RC_X$
This configuration can be used to obtain extended pulse widths, because of the larger timing resistor allowed by beta multiplication. Electrolytics with high inverse leakage currents can be used.



$R < R_X\ (0.7)\ (h_{FE}\ Q_1)$ or < 2.5 MΩ whichever is the lesser
$R_X\ (min) < R_Y < R_X\ (max)$
Q_1: NPN silicon transistor with h_{FE} requirements of above equations, such as 2N5961 or 2N5962

$t \approx 0.3\ RC_X$
This configuration is not recommended with retriggerable operation.

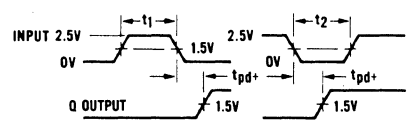
6. To obtain variable pulse width by remote trimming, the following circuit is recommended:



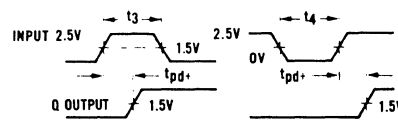
7. Under any operating condition, C_X and R_X (min) must be kept as close to the circuit as possible to minimize stray capacitance and reduce noise pickup.
8. Input Trigger Pulse Rules. See Triggering Truth Table, page 5.

Input to Pin 5 (11)
Pin 4 (12) = Low
Pin 3 (13) = High

t_1, t_3 = Min. Positive Input Pulse Width >40 ns
t_2, t_4 = Min. Negative Input Pulse Width >40 ns

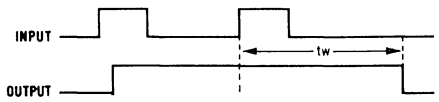


Input to Pin 4 (12)
Pin 5 (11) = High, Pin 3 (13) = High



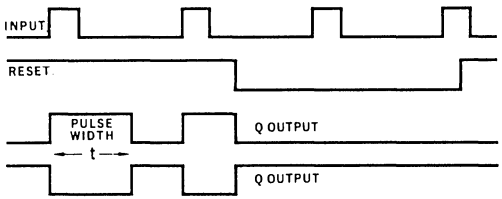
9. The retriggerable pulse width is calculated as shown below:

$$tw = tpw + t_{pd+} = 0.31\ R_X C_X\ (1 + \frac{1}{R_X}) + t_{pd+}.$$



The retrigger pulse width is equal to the pulse width tpw plus a delay time. For pulse widths greater than 500 ns, tw can be approximated as tpw. Retriggering will not occur if the retrigger pulse comes within ≈0.3 C_X ns after the initial trigger pulse. (i.e. during the discharge cycle).

10. Reset Operation — An overriding active low level reset is provided on each oneshot. By applying a low to the reset, any timing cycle can be terminated or any new cycle inhibited until the low reset input is removed. Trigger inputs will not produce spikes in the output when the reset is held low.



11. V_{CC} and Ground wiring should conform to good high frequency standards so that switching transients on V_{CC} and Ground leads do not cause interaction between one-shots.

ELECTRICAL CHARACTERISTICS (T_A = −55°C to 125°C, V_{CC} = 5 V ± 10%)

Symbol	−55°C Min.	−55°C Max.	+25°C Min.	+25°C Typ.	+25°C Max.	+125°C Min.	+125°C Max	Units	Conditions (Note 1)
V_{OH}	2.4		2.4	3.3		2.4		Volts	V_{CC} = 4.5 V, I_{OH} = −0.96 mA (Note 2)
V_{OL}		0.4		0.2	0.4		0.4	Volts	V_{CC} = 4.5 V, I_{OL} = 9.62 mA (Note 2) V_{CC} = 5.5 V, I_{OL} = 12.8 mA
V_{IH}	2.0		1.7			1.5		Volts	Guaranteed input high
V_{IL}		0.85			0.90		0.85	Volts	Guaranteed input low
I_{IL}		−1.6		−1.1	−1.6		−1.6	mA	V_{CC} = 5.5 V, V_{IN} = 0.4 V
		−1.24		−0.97	−1.24		−1.24	mA	V_{CC} = 4.5 V, V_{IN} = 0.4 V
I_{IH}				10	60		60	μA	V_{CC} = 5.5 V, V_{IN} = 4.5 V
I_{SC}					−25			mA	V_{CC} = 5.5 V, V_{OUT} = 1.0 V (Note 2)
I_{PD}		45		39	45		45	mA	V_{CC} = 5.0 V
t_{pd+}				25	35			ns	V_{CC} = 5.0 V, R_X = 5.0 kΩ C_X = 0, C_L = 15 pF
t_{pd-}				29	43			ns	V_{CC} = 5.0 V R_X = 5.0 kΩ C_X = 0, C_L = 15 pF
$t_{pw(min)}$				72	90			ns	V_{CC} = 5.0 V R_X = 5.0 kΩ
				78	100			ns	C_X = 0, C_L = 15 pF
t_{pw}			3.08	3.42	3.76			μs	V_{CC} = 5.0 V, R_X = 10 kΩ, C_X = 1000 pF
C_{STRAY}		50			50		50	pF	Pins 2 and 14 to Ground
R_X	5.0	25	5.0		25	5.0	25	kΩ	

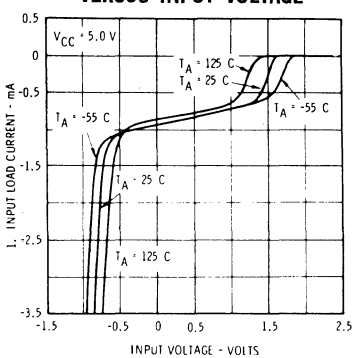
ELECTRICAL CHARACTERISTICS (T_A = 0°C to 75°C, V_{CC} = 5 V ± 5%)

Symbol	−0°C Min.	−0°C Max.	Limits +25°C Min.	+25°C Typ.	+25°C Max.	+75°C Min.	+75°C Max	Units	Conditions (Note 1)
V_{OH}	2.4		2.4	3.4		2.4		Volts	V_{CC} = 4.75 V, I_{OH} =−0.96 mA (Note 2)
V_{OL}		0.45		0.2	0.45		0.45	Volts	V_{CC} = 4.75 V, I_{OL} = 11.3 mA (Note 2)
									V_{CC} = 5.25 V, I_{OL} = 12.8 mA
V_{IH}	1.9		1.8			1.65		Volts	Guaranteed input high
V_{IL}		0.85			0.85		0.85	Volts	Guaranteed input low
I_{IL}		−1.6		−1.0	−1.6		−1.6	mA	V_{CC} = 5.25 V, V_{IN} = 0.45 V
		−1.41			−1.41		−1.41	mA	V_{CC} = 4.75 V, V_{IN} = 0.45 V
I_{IH}				10	60		60	μA	V_{CC} = 5.25 V, V_{IN} = 4.5 V
I_{SC}					−35			mA	V_{CC} = 5.25 V, V_{OUT} = 1.0 V (Note 2)
I_{PD}		52		39	50		52	mA	V_{CC} = 5.0 V, Ground, Pins 1 and 2
t_{pd+}				25	40			ns	V_{CC} = 5.0 V, R_X = 5.0 kΩ
									C_X = 0, C_L = 15 pF
t_{pd-}				29	48			ns	V_{CC} = 5.0 V R_X = 5.0 kΩ
									C_X = 0, C_L = 15 pF
$t_{pw(min)}$				72	100			ns	V_{CC} = 5.0 V R_X = 5.0 kΩ
				78	110			ns	C_X = 0, C_L = 15 pF
t_{pw}			3.08	3.42	3.76			μs	V_{CC} = 5.0 V, R_X = 10 kΩ, C_X = 1000 pF
C_{STRAY}		50			50		50	pF	Pins 2 and 14 to Ground
R_X	5.0	50	5.0		50	5.0	50	kΩ	

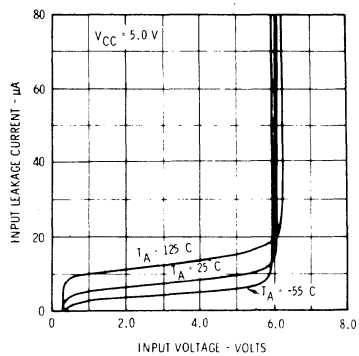
1. Unless otherwise noted, 10 kΩ resistor placed between Pin 2 (14) and V_{CC}, for all tests. (R_X)
2. Ground Pin 1 (15) for V_{OL} on Pin 7 (9), or for V_{OH} on Pin 6 (10), or for I_{SC} on Pin 6 (10); also, apply momentary ground to Pin 4 (12). Open Pin 1 (15) for V_{OL} on Pin 6 (10), or for V_{OH} on Pin 7 (9), or for I_{SC} on Pin 7 (9).

TYPICAL ELECTRICAL CHARACTERISTICS

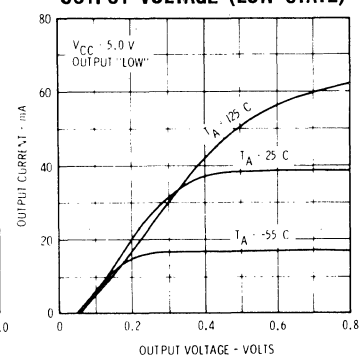
INPUT LOAD CURRENT VERSUS INPUT VOLTAGE



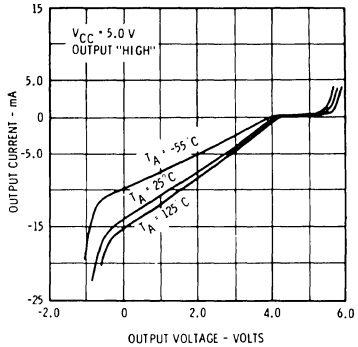
INPUT LEAKAGE CURRENT VERSUS INPUT VOLTAGE



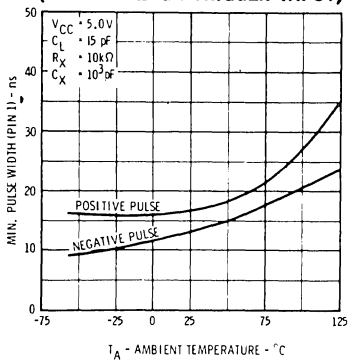
OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (LOW STATE)



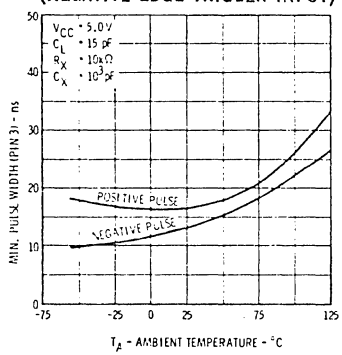
OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (HIGH STATE)



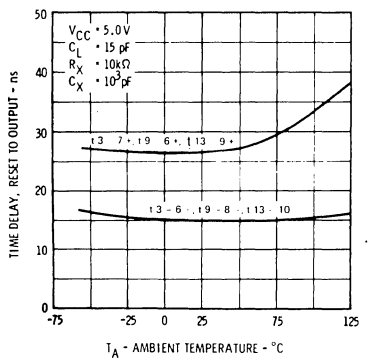
MINIMUM PULSE WIDTH TO TRIGGER VERSUS AMBIENT TEMPERATURE (POSITIVE EDGE TRIGGER INPUT)



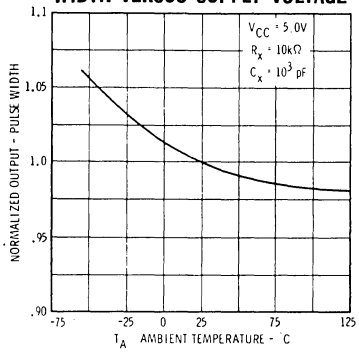
MINIMUM PULSE WIDTH TO TRIGGER VERSUS AMBIENT TEMPERATURE (NEGATIVE EDGE TRIGGER INPUT)



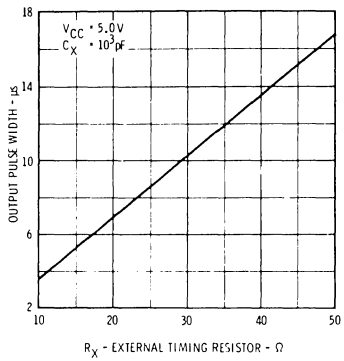
MINIMUM TIME DELAY, RESET TO OUTPUT VERSUS AMBIENT TEMPERATURE



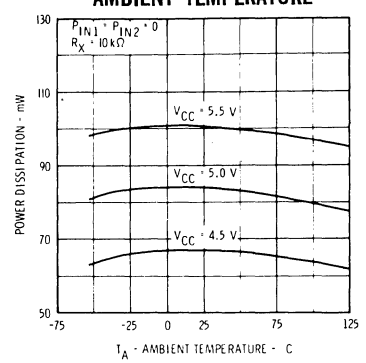
NORMALIZED OUTPUT PULSE WIDTH VERSUS SUPPLY VOLTAGE



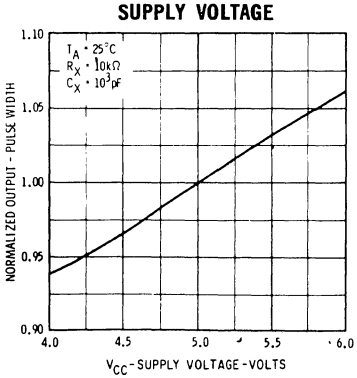
PULSE WIDTH VERSUS TIMING RESISTOR



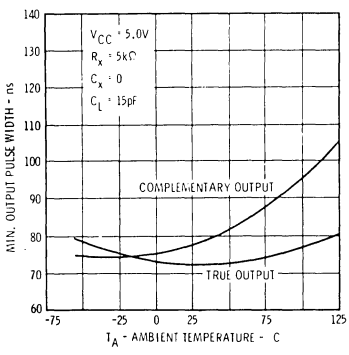
POWER DISSIPATION VERSUS AMBIENT TEMPERATURE



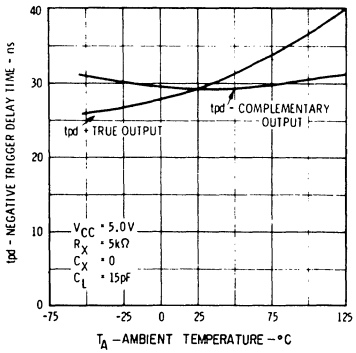
NORMALIZED OUTPUT PULSE WIDTH VERSUS SUPPLY VOLTAGE



MINIMUM OUTPUT PULSE WIDTH VERSUS AMBIENT TEMPERATURE

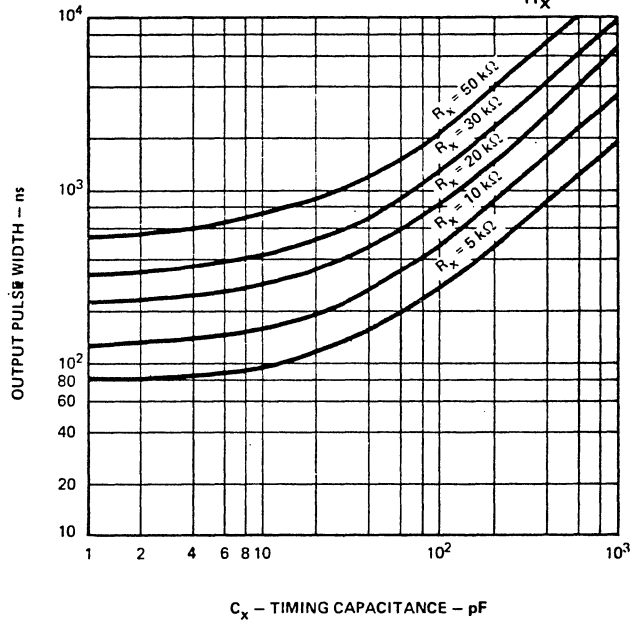


NEGATIVE TRIGGER DELAY TIME VERSUS AMBIENT TEMPERATURE



OUTPUT PULSE WIDTH VERSUS TIMING RESISTANCE AND CAPACITANCE FOR $C_X < 10^3$ pF

For $C_X \geq 10^3$ pF, $t_{pw} = 0.31\ R_X C_X\ (1 + \frac{1}{R_X})$



LOADING RULES

TTμL INPUT LOAD AND DRIVE FACTORS

INPUTS	LOAD	
	HIGH	LOW
3, 4, 5, 11, 12, 13	1 U.L.	1 U.L.

OUTPUTS	DRIVE FACTOR	
	HIGH	LOW
6, 7, 9, 10	16 U.L.	8 U.L.

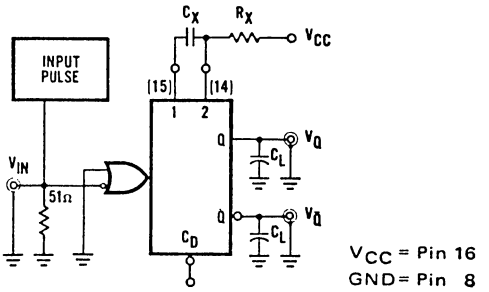
1 U.L. = 1 TTL Gate Input Load

TRIGGERING TRUTH TABLE

PIN NO'S. 5(11)	4(12)	3(13)	Operation
H→L	L	H	Trigger
H	L→H	H	Trigger
X	X	L	Reset

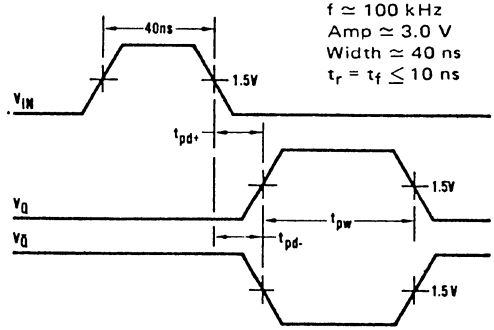
H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
H→L = HIGH to LOW Voltage Level transition
L→H = LOW to HIGH Voltage Level transition

SWITCHING CIRCUITS AND WAVEFORMS

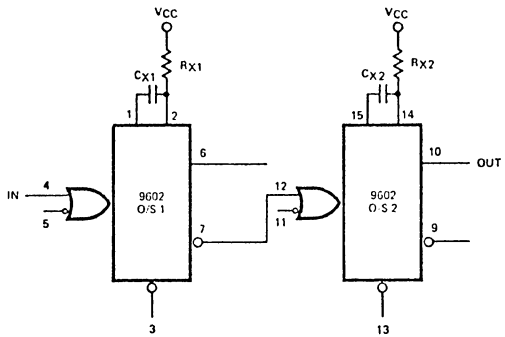


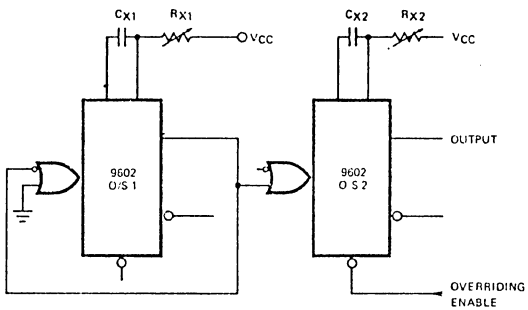
V_{CC} = Pin 16
GND = Pin 8

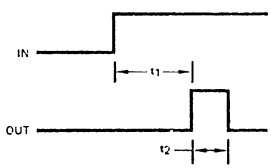
INPUT PULSE
f ≃ 100 kHz
Amp ≃ 3.0 V
Width ≃ 40 ns
$t_r = t_f \leq 10$ ns

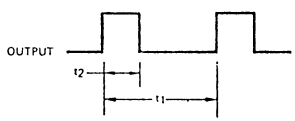


APPLICATIONS









The first one-shot determines the time t_1 before the initiation of the output pulse. The second one-shot determines t_2 the output pulse width.

PULSE GENERATOR

The output frequency produced with the above configuration is determined by C_{X1} and R_{X1}, while the pulse width is determined by C_{X2} and R_{X2}. O/S 1 forms an astable multivibrator with an output pulse width of approximately 25 ns, while O/S 2 extends the pulse width to the required value.

MSI 4-BIT SHIFT REGISTER

The MIC9300 Four Bit Shift Register is a high speed multi-functional sequential logic block which is useful in a wide variety of register and counter applications. As a register it may be used in serial-serial, shift left, shift right, serial-parallel, parallel-serial, and parallel-parallel data transfers. The circuit uses TTL for high speed and high fanout capability, and is compatible with DTL, and TTL digital integrated circuits.

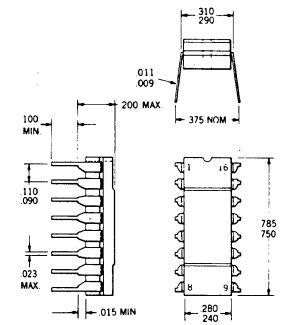
- **15 MHz shift frequency**
- **Synchronous parallel entry**
- **J, $\overline{K}$ inputs to first stage**
- **Asynchronous common reset**
- **Typical power dissipation of 300 mW**
- **The input/output characteristics provide easy interfacing with DTL930, TTL9000, TTL7400 and MSI families**
- **All ceramic HERMETIC 16 pin Dual In-Line package**
- **Input diode clamping**

ABSOLUTE MAXIMUM RATINGS

(above which the useful life may be impaired)

CHARACTERISTICS		UNITS
Storage Temperature	−65°C to +150	°C
Temperature (Ambient) Under Bias	−55°C to +125	°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7	Volts
Voltage Applied to Outputs for high output state	−0.5V to +V_{CC}	value
Input Voltage (D.C.)	−0.5V to +5.5	Volts

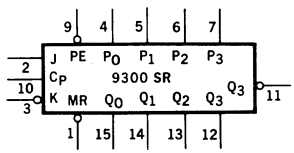
PHYSICAL DIMENSIONS



NOTES:
1 Leads are intended for insertion in hole rows on .300" centers. They are purposely shipped with "positive" (.375) misalignment to facilitate insertion.
2 Board drilling dimensions should equal your practice for a conventional .020 inch diameter lead.

Figure 1

LOGIC SYMBOL



V_{CC} = PIN 16
GND = PIN 8

Figure 2

SPECIAL ORDERING CODE

Temperature Range:
−55°C to +125°C, add -1 to MIC number.
0°C to +75°C, add -5 to MIC number.

Case Style:
¼" x ⅜" Flat Pack, add "B" following last digit.
Ceramic Dual In-Line, 16 leads, add "D" following last digit.

Example:
MIC9300-1D is −55°C to +125°C. Temperature range in Ceramic Dual-In-Line, 16 lead package.
Flat-pack and Dual-In-Line packages have same pin configuration.

FUNCTIONAL DESCRIPTION

The logic symbol of Figure 2 provides an indication of the functional characteristics of the MIC9300 four bit shift register. Several special logical features of the MIC9300 design which provide a high degree of general usefulness are described below:

1. A J$\overline{K}$ input is provided to the first flip flop in the register. This type of input is the same as the more common JK input except that the low voltage level activates the $\overline{K}$ input. This provides the greater power of the JK type input for more general applications and at the same time the simple D type input that is most appropriate for a shift register can be easily obtained by simply tying the two inputs together.
2. There is no restriction on the activity of the J or $\overline{K}$ inputs for logical operation — except for the set up and release time requirements.
3. Parallel inputs for all four stages are provided. These will determine the next condition of the shift register synchronous with the clock input, whenever the Parallel Enable input is low. With the Parallel Enable input low the element appears as four common clocked D flip flops. When the Parallel Enable is high, or not connected, the shift register performs a one bit shift for each clock input. In both cases the next state of the flip flop occurs after the low to high transition of the clock input.
4. An internal clock buffer provides both reduced clock input loading, and the ability to gate the clock with only a single NAND gate.
5. The active high output is provided for all four stages and an active low output is provided for the last stage.
6. A master asynchronous clear input allows the setting to zero of all stages, independent of the condition of any other inputs.

TABLE I — TRUTH TABLE FOR SERIAL ENTRY
(PE = HIGH, MR = HIGH, (n + 1) indicates state after next clock)

J	$\overline{K}$	Q_0 at t_{n+1}
L	L	L
L	H	Q_0 at t_n (no change)
H	L	$\overline{Q}_0$ at t_n (toggles)
H	H	H

TABLE II — LOADING RULES (1 U.L. = 1 TTL Gate Input Load)

INPUTS	LOADING
J, $\overline{K}$, $\overline{MR}$, P_0, P_1, P_2 & P_3	1 U.L.
$\overline{PE}$	2.3 U.L.
C_P	4 U.L.
OUTPUTS	**FANOUT**
Q_0, Q_1, Q_2, Q_3 & $\overline{Q}_3$	6 U.L.

ELECTRICAL CHARACTERISTICS (MIC9300-1X) ($T_A = -55°C$ to $+125°C$, $V_{CC} = 5.0\ V \pm 10\%$)

SYMBOL	CHARACTERISTICS	LIMITS						UNITS	CONDITIONS & COMMENTS
		−55°C		+25°C			+125°C		
		MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.	
V_{OH}	Output High Voltage	2.2		2.4	2.7		2.4		Volts	$V_{CC} = 4.5\ V$, $I_{OH} = -0.36$ mA
V_{OL}	Output Low Voltage		0.4		0.2	0.4		0.4	Volts	$V_{CC} = 5.5\ V$, $I_{OL} = 9.6$ mA $V_{CC} = 4.5\ V$, $I_{OL} = 7.44$ mA
V_{IH}	Input High Voltage	2.0		1.7			1.4		Volts	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.8			0.9		0.8	Volts	Guaranteed input low threshold for all inputs
I_F	Input Load Current* J, K, MR, P_0, P_1, P_2 & P_3		−1.6 −1.24		−1.10 −0.97	−1.6 −1.24		−1.6 −1.24	mA mA	$V_{CC} = 5.5\ V$ $V_{CC} = 4.5\ V$, $V_F = 0.4\ V$
I_R	Input Leakage Current* J, $\overline{K}$, $\overline{MR}$, P_0, P_1, P_2 & P_3				15	60		60	μA	$V_{CC} = 5.5\ V$, $V_R = 4.5\ V$

ELECTRICAL CHARACTERISTICS (MIC9300-5X) ($T_A = 0°C$ to $+75°C$, $V_{CC} = 5.0\ V \pm 5\%$)

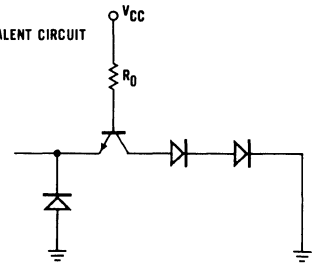
SYMBOL	CHARACTERISTICS	LIMITS						UNITS	CONDITIONS
		0°C		+25°C			+75°C		
		MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.	
V_{OH}	Output High Voltage	2.4		2.4	3.0		2.4		Volts	$V_{CC} = 4.75\ V$, $I_{OH} = -0.36$ mA
V_{OL}	Output Low Voltage		0.45		0.2	0.45		0.45	Volts	$V_{CC} = 5.25\ V$, $I_{OL} = 9.6$ mA
V_{IH}	Input High Voltage	1.9		1.8			1.6		Volts	$V_{CC} = 4.75\ V$, $I_{OL} = 8.5$ mA Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.85			0.85		0.85	Volts	Guaranteed input low threshold for all inputs
I_F	Input Load Current* J, K, MR, P_0, P_1, P_2 & P_3		−1.6 −1.41		−1.0 −0.9	−1.6 −1.41		−1.6 −1.41	mA mA	$V_{CC} = 5.25\ V$ $V_{CC} = 4.75\ V$, $V_F = 0.45\ V$
I_R	Input Leakage Current* J, $\overline{K}$, $\overline{MR}$, P_0, P_1, P_2 & P_3				15	60		60	μA	$V_{CC} = 5.25\ V$, $V_R = 4.5\ V$

*For CP and $\overline{PE}$ input currents, use load factors in Table II

TYPICAL INPUT AND OUTPUT CHARACTERISTICS

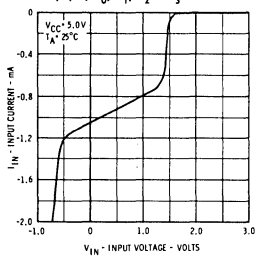
INPUTS

EQUIVALENT CIRCUIT

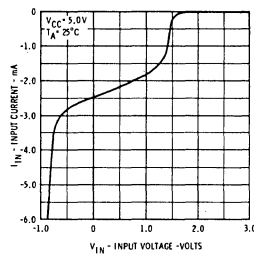


INPUT CURRENT VERSUS INPUT VOLTAGE

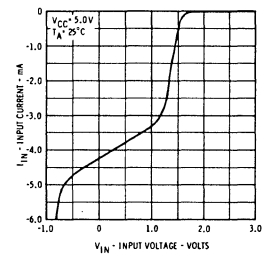
$\overline{MR}$, J, $\overline{K}$, P_0, P_1, P_2 & P_3



$\overline{PE}$

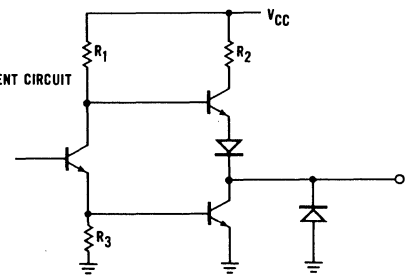


CP



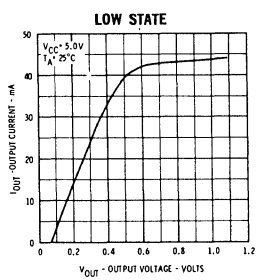
OUTPUTS

EQUIVALENT CIRCUIT

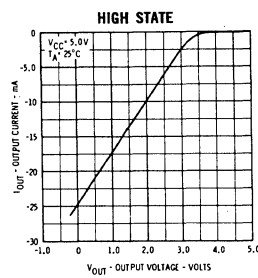


OUTPUT CURRENT VERSUS OUTPUT VOLTAGE
(Q_0, Q_1, Q_2, Q_3 AND $\overline{Q}_3$)

LOW STATE



HIGH STATE



SWITCHING CHARACTERISTICS ($T_A = 25°C$)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS & COMMENTS
t_{pd+}	Turn Off Delay		20	35	ns	$V_{CC} = 5.0$ V, $C_L = 15$ pF
t_{pd-}	Turn On Delay		25	45	ns	(See Fig. 5 & 6a)
f_{sr}	Shift Right Frequency	15	25		MHz	$V_{CC} = 5.0$ V, $C_L = 15$ pF (See Fig. 5 & 6c)
CP_{pw}	Clock Pulse Width	35	15		ns	
t_s	Set-up Time	35	17		ns	$V_{CC} = 5.0$ V
t_r	Release Time		16	0	ns	$C_L = 15$ pF
$t_s(\overline{PE})$	Set-up Time for $\overline{PE}$	45	26		ns	(See Figs. 6a & 6b)
$t_r(\overline{PE})$	Release Time for $\overline{PE}$		25	10	ns	
$t_{pd-}(\overline{MR})$	Reset Time for $\overline{MR}$		35		ns	
$t_{rec}(\overline{MR})$	Recovery Time for $\overline{MR}$		20		ns	
$\overline{MR}_{pw}$	Min Reset Pulse Width		15		ns	

SET-UP TIME: t_s is defined as the minimum time required for the logic level to be present at the logic input prior to the clock transition from low to high in order for the flip-flop(s) to respond.

RELEASE TIME: t_r is defined as the maximum time allowed for the logic level to be present at the logic input prior to the clock transition from low to high in order for the flip-flop(s) not to respond.

RECOVERY TIME FOR MR: $t_{rec}(MR)$ is defined as the minimum time required between the end of the reset pulse and the clock transition from low to high in order for the flip-flop(s) to respond to the clock.

Figure 3

PROPAGATION DELAY — CLOCK TO Q_3 OR $\overline{Q}_3$ OUTPUT VS TEMPERATURE

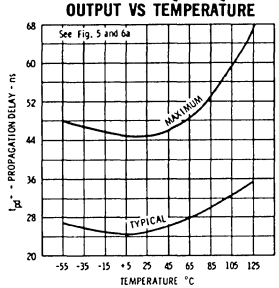
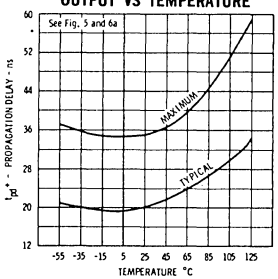
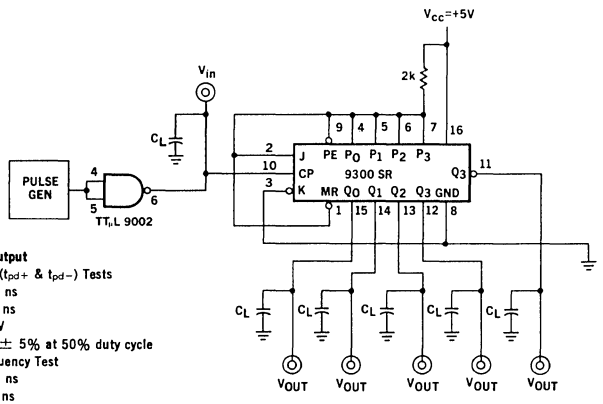


Figure 4

PROPAGATION DELAY — CLOCK TO Q_3 OR $\overline{Q}_3$ OUTPUT VS TEMPERATURE





Pulse Generator Output

1. Switching Time (t_{pd+} & t_{pd-}) Tests
   - Rise Time < 15 ns
   - Fall Time < 15 ns
   - Amplitude ≈ 4 V
   - Freq. = 2 MHz ± 5% at 50% duty cycle
2. Shift Right Frequency Test
   - Rise Time < 15 ns
   - Fall Time < 15 ns
   - Amplitude ≈ 4 V
   - Freq. = 15 MHz with pulse width adjustment so that V_{IN} has duty cycle of approx. 50%.

C_L includes probe and jig capacitance

Figure 5 — SWITCHING TIME & SHIFT RIGHT FREQUENCY TEST CIRCUIT

Fig. 6a

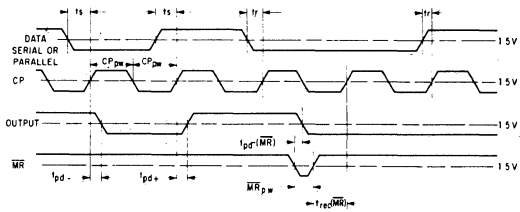


Fig. 6b

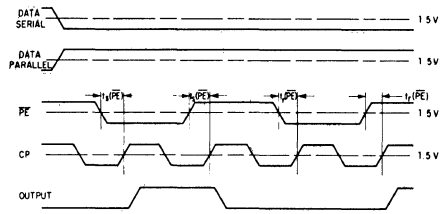


Fig. 6c

VOUT Frequency = ½ X VIN Frequency

Figure 6 — SWITCHING TIME & SHIFT RIGHT FREQUENCY WAVEFORMS

APPLICATIONS — The MIC9300 has been designed to be useful in a wide variety of applications. The multifunctional capability of the MIC9300 is illustrated by the applications shown below. below.

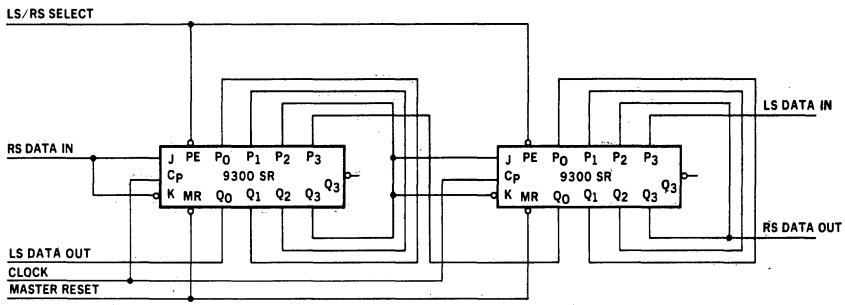


Figure 7 — EIGHT BIT LEFT/RIGHT SHIFT REGISTER

This register shifts Left or Right on each shift clock, depending upon the condition of the LS/RS SELECT input. If this input is high, Right Shift occurs and if low, Left Shift occurs.

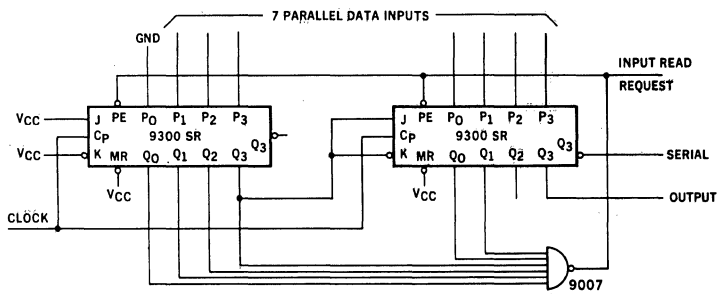


Figure 8 — SEVEN BIT PARALLEL TO SERIAL CONVERTER

This parallel to serial converter uses a marker bit, to count the data bits shifted out, so that a parallel load enable is generated to load the next parallel word for conversion at the correct time.

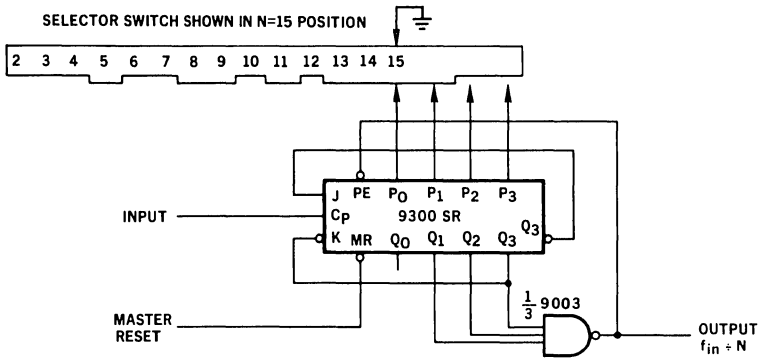
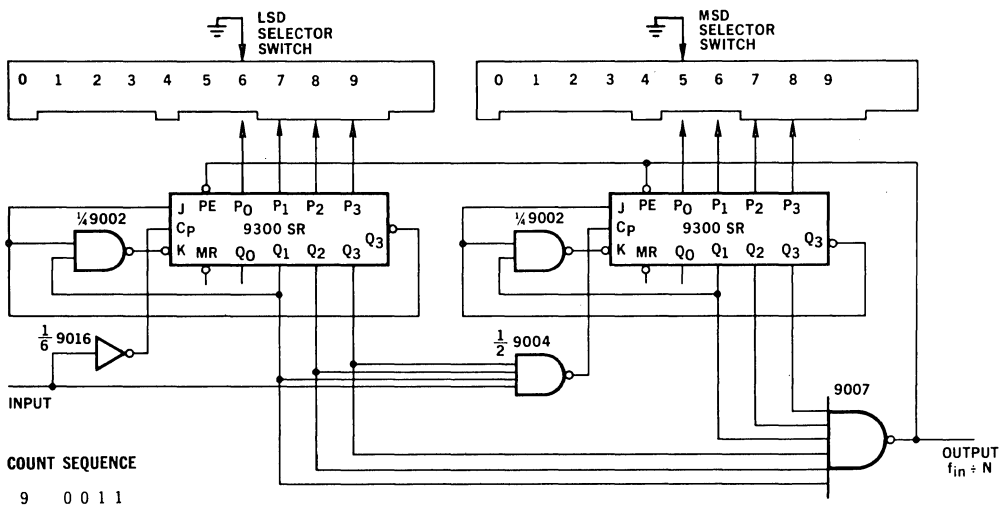


Figure 9 — DIVIDE BY N COUNTER FOR N=2 to 15

This counter produces an output pulse for every N input pulses, where the number N is determined by the setting of the slide selector switch as shown or by logic inputs to the parallel data lines from an external source.



COUNT SEQUENCE

9	0 0 1 1
8	0 0 0 1
7	0 0 0 0
6	1 0 0 0
5	1 1 0 0
4	0 1 1 0
3	1 0 1 1
2	1 1 0 1
1	1 1 1 0
0	0 1 1 1

Figure 10 — TWO DECADE PROGRAMMABLE DIVIDER

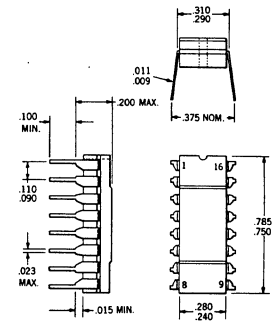
This circuit divides by any number "N" from 1 to 100. The selected N is one greater than is shown on the slide switches. As an example the switches are showing 56, therefore the circuit will divide by 57 with this setting.

MSI ONE-OF-TEN DECODER

The MIC9301 is a multipurpose decoder designed to accept four inputs and provide 10 mutually exclusive outputs. The circuit uses TTL for high speed and high fan out capability, and is compatible with DTL, and TTL digital integrated circuits.

- **Multi-function capability**
- **Mutually exclusive outputs**
- **Guaranteed fanout of 10 TTL loads over the full temperature range and supply voltage ranges**
- **High capacitive drive capability**
- **Demultiplexing capability**
- **Typical power dissipation of 145 mW**
- **The input/output characteristics provide easy interfacing with DTL930, TTL9000, TTL7400 and MSI families**
- **All ceramic HERMETIC 16-pin Dual In-Line package**
- **Input clamp diodes limit high speed line termination effects**

PHYSICAL DIMENSIONS



NOTES:
1. Leads are intended for insertion in hole rows on .300" centers. They are purposely shipped with "positive" (.375) misalignment to facilitate insertion.
2. Board drilling dimensions should equal your practice for a conventional .020 inch diameter lead.

Fig. 1

ABSOLUTE MAXIMUM RATINGS

(above which the useful life may be impaired)

CHARACTERISTICS		UNITS
Storage Temperature	−65°C to +150	°C
Temperature (Ambient) Under Bias	−55°C to +125	°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7	Volts
Voltage Applied to Outputs for high output state	−0.5V to +V_{CC}	value
Input Voltage (D.C.)	−0.5V to +5.5	Volts

LOGIC SYMBOL

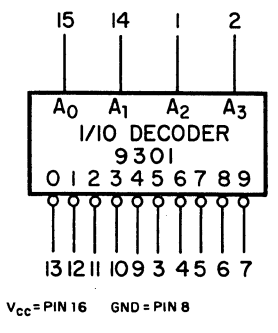


Fig. 2

ELECTRICAL CHARACTERISTICS (MIC9301-1X) ($T_A = -55°C$ to $+125°C$, $V_{CC} = 5.0\ V \pm 10\%$)

SYMBOL	CHARACTERISTICS	LIMITS −55°C MIN.	LIMITS −55°C MAX.	LIMITS +25°C MIN.	LIMITS +25°C TYP.	LIMITS +25°C MAX.	LIMITS +125°C MIN.	LIMITS +125°C MAX.	UNITS	CONDITIONS
V_{OH}	Output High Voltage	2.4		2.4	2.7		2.4		Volts	$V_{CC} = 4.5\ V$, $I_{OH} = -0.6\ mA$
V_{OL}	Output Low Voltage		0.4		0.2	0.4		0.4	Volts	$V_{CC} = 4.5\ V$, $I_{OL} = 12.4\ mA$ $V_{CC} = 5.5\ V$, $I_{OL} = 16.0\ mA$
V_{IH}	Input High Voltage	2.0		1.7			1.4		Volts	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.8			.09		0.8	Volts	Guaranteed input low threshold for all inputs
I_F	Input Load Current		−1.6		−1.10	−1.6		−1.6	mA	$V_{CC} = 5.5\ V$, $V_F = 0.4\ V$
			−1.24		−0.97	−1.24		−1.24	mA	$V_{CC} = 4.5\ V$, $V_F = 0.4\ V$
I_R	Input Leakage Current				15	60		60	μA	$V_{CC} = 5.5\ V$, $V_R = 4.5\ V$
t_{pd+}	Turn Off Delay Input to Output				23	35			ns	$V_{CC} = 5.0\ V$
t_{pd-}	Turn On Delay Input to Output				20	30			ns	$C_L = 15\ pF$ See Fig. 8

FUNCTIONAL DESCRIPTION

The MIC9301 Decoder accepts four active high BCD inputs and provides ten mutually exclusive active low outputs, as shown by Figure 2. The active low outputs facilitate memory addressing when inverting drivers are used between decoder and memory elements such as the MIC9033.

The logic design of the MIC9301 ensures that all outputs are high when binary codes greater than nine are applied to the inputs.

The most significant A_3 input produces a useful inhibit function when the MIC9301 is used as a 1 out of 8 decoder. This is illustrated in the 1 out of 32 decoder shown in Figure 9.

The Truth Table and Loading Rules for the MIC9301 are shown in Table I and Table II.

SPECIAL ORDERING CODE

Temperature Range:
−55°C to +125°C, add -1 to MIC number.
0°C to +75°C, add -5 to MIC number.

Case Style:
¼" x ⅜" Flat Pack, add "B" following last digit.
Ceramic Dual In-Line, 16 leads, add "D" following last digit.

Example:
MIC9301-1D is −55°C to +125°C. Temperature range in Ceramic Dual-In-Line, 16 lead package.
Flat-pack and Dual-In-Line packages have same pin configuration.

TABLE I — TRUTH TABLE

A_0	A_1	A_2	A_3	0	1	2	3	4	5	6	7	8	9
L	L	L	L	L	H	H	H	H	H	H	H	H	H
H	L	L	L	H	L	H	H	H	H	H	H	H	H
L	H	L	L	H	H	L	H	H	H	H	H	H	H
H	H	L	L	H	H	H	L	H	H	H	H	H	H
L	L	H	L	H	H	H	H	L	H	H	H	H	H
H	L	H	L	H	H	H	H	H	L	H	H	H	H
L	H	H	L	H	H	H	H	H	H	L	H	H	H
H	H	H	L	H	H	H	H	H	H	H	L	H	H
L	L	L	H	H	H	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L
L	H	L	H	H	H	H	H	H	H	H	H	H	H
H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H
H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	H	H	H	H	H	H	H	H	H	H	H	H	H
H	H	H	H	H	H	H	H	H	H	H	H	H	H

H = High Voltage Level
L = Low Voltage Level

TABLE II — LOADING RULES (1U.L. = TTL Gate Input Load)

INPUTS	LOADING
A_0, A_1, A_2 & A_3	1 U.L.

OUTPUTS	FANOUT
0, 1, 2, 3, 4, 5, 6, 7, 8, & 9	10 U.L.

ELECTRICAL CHARACTERISTICS (MIC9301-5X) (T_A = 0°C to +75°C, V_{CC} = 5.0 V ±5%)

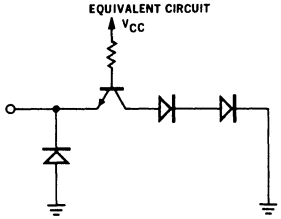
SYMBOL	CHARACTERISTICS	LIMITS 0°C MIN.	0°C MAX.	+25°C MIN.	+25°C TYP.	+25°C MAX.	+75°C MIN.	+75°C MAX.	UNITS	CONDITIONS
V_{OH}	Output High Voltage	2.4		2.4	3.0		2.4		Volts	V_{CC} = 4.75 V, I_{OH} = −0.6 mA
V_{OL}	Output Low Voltage		0.45		0.2	0.45		0.45	Volts	V_{CC} = 4.75 V, I_{OL} = 14.1 mA V_{CC} = 5.25 V, I_{OL} = 16.0 mA
V_{IH}	Input High Voltage	1.9		1.8			1.6		Volts	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.85			0.85		0.85	Volts	Guaranteed input low threshold for all inputs
I_F	Input Load Current		−1.6		−1.0	−1.6		−1.6	mA	V_{CC} = 5.25 V, V_F = 0.45 V
			−1.41		−0.9	−1.41		−1.41	mA	V_{CC} = 4.75 V, V_F = 0.45 V
I_R	Input Leakage Current				15	60		60	μA	V_{CC} = 5.25 V, V_R = 4.5 V
t_{pd+}	Turn Off Delay Input to Output				23	35			ns	V_{CC} = 5.0 V
t_{pd-}	Turn On Delay				20	30			ns	C_L = 15 pF See Fig. 8

TYPICAL INPUT AND OUTPUT CHARACTERISTICS

Fig. 3

INPUTS

EQUIVALENT CIRCUIT



INPUT CURRENT VERSUS INPUT VOLTAGE

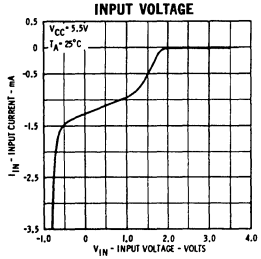
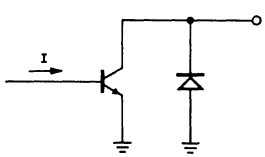


Fig. 4

OUTPUTS

EQUIVALENT CIRCUIT

OUTPUT LOW



OUTPUT CURRENT VERSUS OUTPUT VOLTAGE OUTPUT LOW

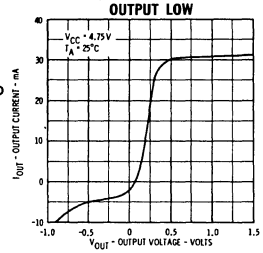
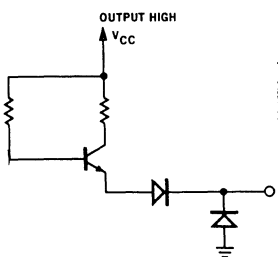
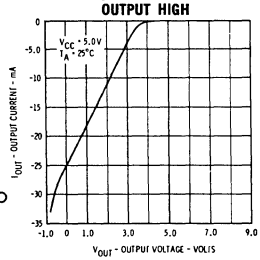


Fig. 5

OUTPUT HIGH



OUTPUT CURRENT VERSUS OUTPUT VOLTAGE OUTPUT HIGH



SWITCHING PERFORMANCE

Fig. 6

TYPICAL TURN ON DELAY VERSUS TEMPERATURE

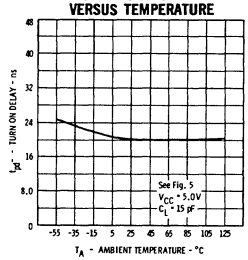
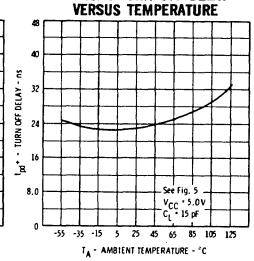
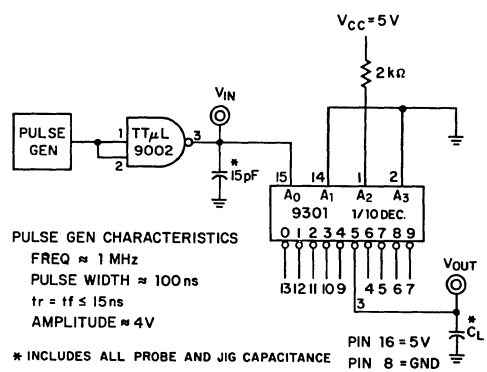


Fig. 7

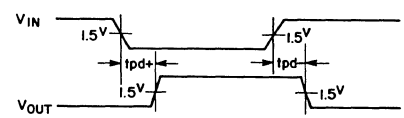
TYPICAL TURN OFF DELAY VERSUS TEMPERATURE





PULSE GEN CHARACTERISTICS
FREQ ≈ 1 MHz
PULSE WIDTH ≈ 100 ns
tr = tf ≤ 15 ns
AMPLITUDE ≈ 4V

* INCLUDES ALL PROBE AND JIG CAPACITANCE



SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

Fig. 8

APPLICATIONS — The MIC9301 decoder may be used for BCD to Decimal or 3 bit binary to octal conversion as well as many other applications. The general purpose nature of the MIC9301 is indicated by its use in the following applications.

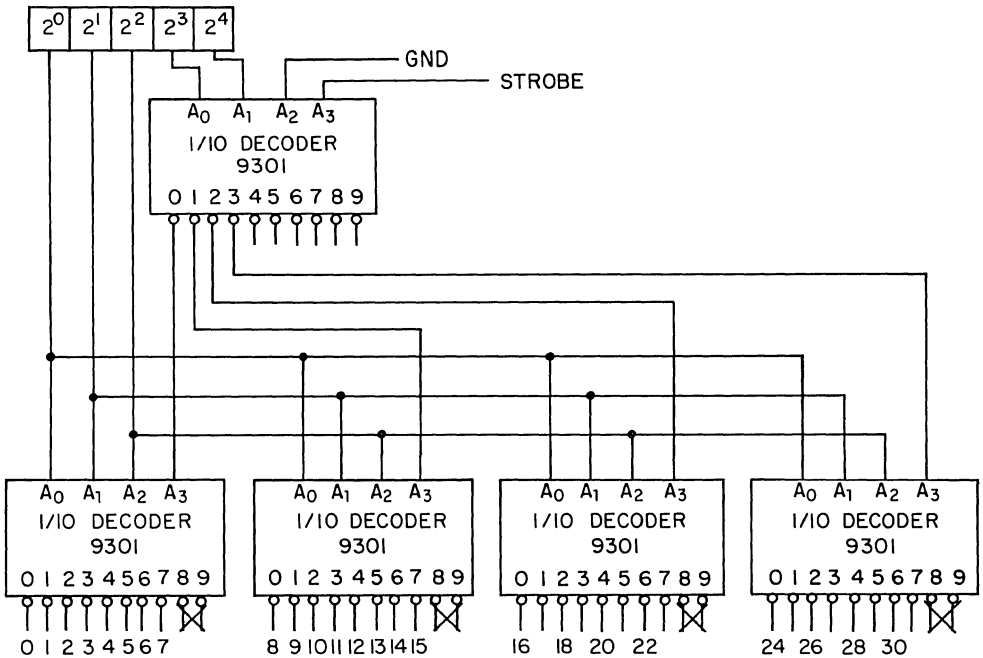
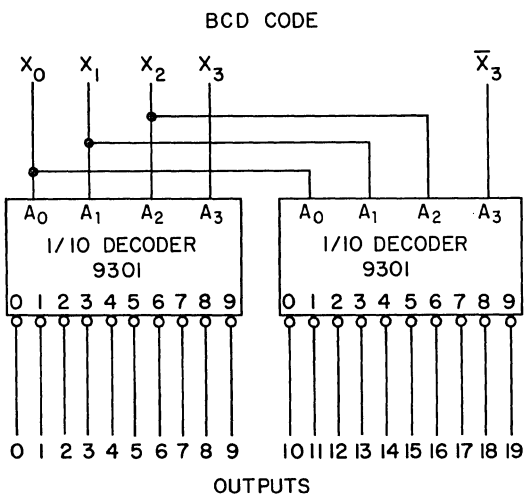


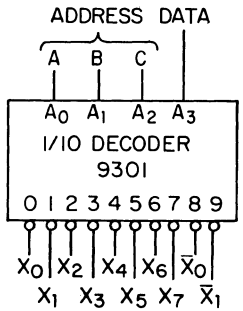
Fig. 9 — ONE-OUT-OF-THIRTY-TWO DECODING



DECIMAL DIGIT	OUTPUT SELECTION BCD CODE 8421	5421	EXCESS 3	4221
0	0, 18	0, 18	3	0, 18
1	1, 19	1, 19	4	1, 19
2	2	2	5	2
3	3	3	6	3
4	4	4	7	6
5	5	8, 10	8, 10	9, 11
6	6	9, 11	9, 11	14
7	7	12	12	15
8	8, 10	13	13	16
9	9, 11	14	14	17

Decode any BCD code using two 9301 elements. Any 4 bit BCD code may be decoded by selecting outputs as shown in the table.

Fig. 10 — DECODE ANY BCD CODE

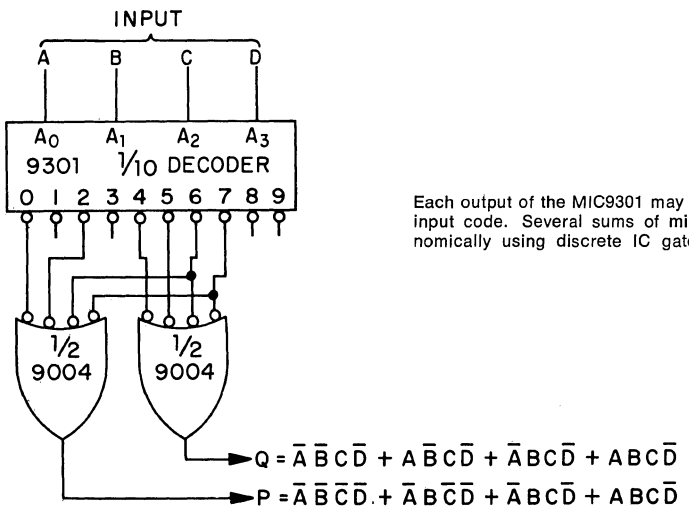


ADDRESS			OUTPUT
A	B	C	LINE
0	0	0	0
1	0	0	1
0	1	0	2
1	1	0	3
0	0	1	4
1	0	1	5
0	1	1	6
1	1	1	7

Data may be routed from a source to any of 8 outputs by addressing that output. All non-addressed outputs remain high.

Complements of outputs 0 and 1 are available at outputs 8 and 9 respectively.

Fig. 11 — DIGITAL DEMULTIPLEXER



Each output of the MIC9301 may be considered a minterm of the input code. Several sums of minterms may be generated economically using discrete IC gates and one MIC9301 decoder.

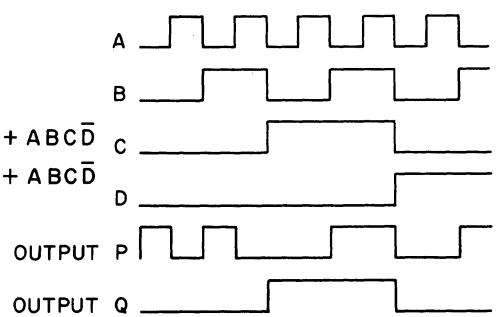


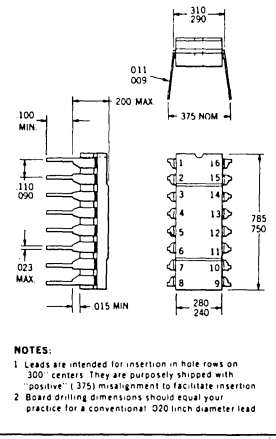
Fig. 12 — MINTERM GENERATOR

MSI DUAL FULL ADDER

- **Multi-function capability**
- **8ns carry propagation delay**
- **Complementary inputs and outputs available**
- **Typical power dissipation of 150mW**
- **The input/output characteristics provide easy interfacing with DTL930, TTL9000, TTL7400 and MSI families**
- **All ceramic HERMETIC 16-pin Dual In-Line package**
- **Input clamp diodes limit high speed termination effects**

The MIC9304 consists of two independent, high speed, binary full adders. The adders are useful in a wide variety of applications including multiple bit parallel add/serial carry addition, parity generation and checking, code conversion, and majority gating. The circuit uses TTL for high speed, high fanout operation and is compatible with DTL, and TTL digital integrated circuits.

PHYSICAL DIMENSIONS



NOTES:
1. Leads are intended for insertion in hole rows on .300" centers. They are purposely shipped with "positive" (.375) misalignment to facilitate insertion.
2. Board drilling dimensions should equal your practice for a conventional .020 inch diameter lead.

Fig. 1

LOGIC SYMBOL

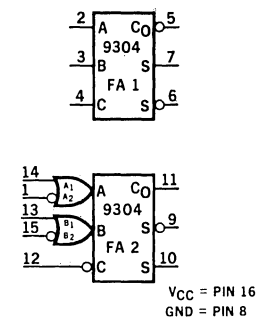


Fig. 2

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

CHARACTERISTICS		UNITS
Storage Temperature	−65°C to +150	°C
Temperature (Ambient) Under Bias	−55°C to +125	°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7	Volts
Voltage Applied to Outputs for high output state	−0.5V to +V_{CC}	value
Input Voltage (D.C.)	−0.5V to +5.5	Volts

TABLE I — TRUTH TABLES

ADDER 1					
INPUTS			OUTPUTS		
C	B	A	$\overline{C}_O$	$\overline{S}$	S
L	L	L	H	H	L
L	L	H	H	L	H
L	H	L	H	L	H
L	H	H	L	H	L
H	L	L	H	L	H
H	L	H	L	H	L
H	H	L	L	H	L
H	H	H	L	L	H

ADDER 2							
INPUTS					OUTPUTS		
$\overline{C}$	B_1	A_1	$\overline{B}_2$	$\overline{A}_2$	C_O	S	$\overline{S}$
L	L	L	L	L	H	H	L
L	L	L	L	H	H	L	H
L	L	L	H	L	H	L	H
L	L	L	H	H	L	H	L
L	L	H	L	L	H	H	L
L	L	H	L	H	H	H	L
L	L	H	H	L	H	L	H
L	L	H	H	H	H	L	H
L	H	L	L	L	H	H	L
L	H	L	L	H	H	L	H
L	H	L	H	L	H	H	L
L	H	L	H	H	H	L	H
L	H	H	L	L	H	H	L
L	H	H	L	H	H	H	L
L	H	H	H	L	H	H	L
L	H	H	H	H	H	H	L
H	L	L	L	L	H	L	H
H	L	L	L	H	L	H	L
H	L	L	H	L	L	H	L
H	L	L	H	H	L	L	H
H	L	H	L	L	H	L	H
H	L	H	L	H	H	L	H
H	L	H	H	L	L	H	L
H	L	H	H	H	L	H	L
H	H	L	L	L	H	L	H
H	H	L	L	H	L	H	L
H	H	L	H	L	H	L	H
H	H	L	H	H	L	H	L
H	H	H	L	L	H	L	H
H	H	H	L	H	H	L	H
H	H	H	H	L	H	L	H
H	H	H	H	H	H	L	H

H = High Voltage Level
L = Low Voltage Level

TABLE II —
LOADING RULES (1 U.L. = TTL Gate Input Unit Load)

INPUTS		LOADING
FA 1	A, B & C	4 U.L.
FA 2	$\overline{A}_2$, $\overline{B}_2$ & $\overline{C}$	4 U.L.
	A_1 & B_1	1 U.L.

OUTPUTS		FANOUT
FA 1	$\overline{C}_O$	7 U.L.
	$\overline{S}$	9 U.L.
	S	10 U.L.
FA 2	C_O	7 U.L.
	S	9 U.L.
	$\overline{S}$	10 U.L.

FUNCTIONAL DESCRIPTION

The MIC9304 logic block consists of two separate high speed carry dependent sum full adders. This design allows a minimum carry propagation time when the adders are used in ripple carry applications. The adders are identical except that adder 2 has provision for either active high or active low inputs at the A and B terminals. The adders produce a low carry and both low and high sum with active high inputs, a high carry and both high and low sum when active low inputs are used. This principle of duality is shown in Figure 12, where the adders are drawn as functional blocks.

The Truth Table and Loading Rules for the MIC9304 are shown in Table I and Table II.

SPECIAL ORDERING CODE

Temperature Range:
−55°C to +125°C, add -1 to MIC number.
0°C to +75°C, add -5 to MIC number.

Case Style:
¼" x ⅜" Flat Pack, add "B" following last digit.
Ceramic Dual In-Line, 16 leads, add "D" following last digit.

Example:
MIC9304-1D is −55°C to +125°C. Temperature range in Ceramic Dual-In-Line, 16 lead package. Flat-pack and Dual-In-Line packages have same pin configuration.

ELECTRICAL CHARACTERISTICS (MIC9304-1X) ($T_A = -55°C$ to $+125°C$, $V_{CC} = 5.0\ V \pm 10\%$)

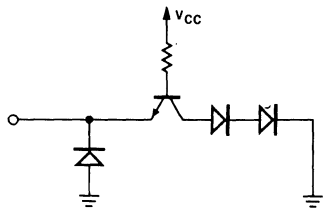
SYMBOL	CHARACTERISTICS	LIMITS −55°C MIN.	LIMITS −55°C MAX.	LIMITS +25°C MIN.	LIMITS +25°C TYP.	LIMITS +25°C MAX.	LIMITS +125°C MIN.	LIMITS +125°C MAX.	UNITS	CONDITIONS
V_{OH}	Output High Voltage	2.2		2.4	2.7		2.4		Volts	$V_{CC} = 4.5\ V$, $I_{OH} = -1.2\ mA$ (Pins 7 & 9) $V_{CC} = 4.5\ V$, $I_{OH} = -1.08\ mA$ (Pins 6 & 10) $V_{CC} = 4.5\ V$, $I_{OH} = -0.84\ mA$ (Pins 5 & 11)
V_{OL}	Output Low Voltage		0.4		0.21	0.4		0.4	Volts	$V_{CC} = 5.5\ V$, $I_{OL} = 16\ mA$ (Pins 7 & 9) $I_{OL} = 14.4\ mA$ (Pins 6 & 10) $I_{OL} = 11.2\ mA$ (Pins 5 & 11) $V_{CC} = 4.5\ V$, $I_{OL} = 12.4\ mA$ (Pins 7 & 9) $I_{OL} = 11.2\ mA$ (Pins 6 & 10) $I_{OL} = 8.7\ mA$ (Pins 5 & 11)
V_{IH}	Input High Voltage	2.0		1.7			1.4		Volts	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.8			0.9		0.8	Volts	Guaranteed input low threshold for all inputs
I_F	Input Load Current		−1.6		−1.1	−1.6		−1.6	mA	$V_{CC} = 5.5\ V$; $V_F = 0.4\ V$, $V_R = 5.5\ V$ on other inputs
4 I_F	Input Load Current		−6.4		−4.4	−6.4		−6.4		
I_F	Input Load Current		−1.24		−0.97	−1.24		−1.24	mA	$V_{CC} = 4.5\ V$; $V_F = 0.4\ V$, $V_R = 5.5\ V$ on other inputs
4 I_F	Input Load Current		−4.96		−3.88	−4.96		−4.96		
I_R	Input Leakage Current				15	60		60	µA	$V_{CC} = 5.5\ V$, $V_R = 4.5\ V$ Ground on other inputs
4 I_R	Input Leakage Current				60	240		240		
t_{pd+}	C to C_O				8	13			ns	$V_{CC} = 5.0\ V$ $C_L = 15\ pF$ See Fig. 11
t_{pd-}	C to C_O				8	13			ns	
t_{pd+}	A_I to S				28	40			ns	
t_{pd-}	A_I to S				25	35			ns	

ELECTRICAL CHARACTERISTICS (MIC9304-5X) ($T_A = 0°C$ to $+75°C$, $V_{CC} = 5.0\ V \pm 5\%$)

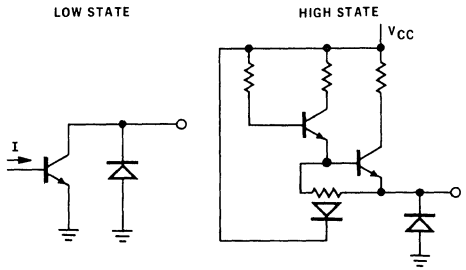
SYMBOL	CHARACTERISTICS	LIMITS 0°C MIN.	LIMITS 0°C MAX.	LIMITS +25°C MIN.	LIMITS +25°C TYP.	LIMITS +25°C MAX.	LIMITS +75°C MIN.	LIMITS +75°C MAX.	UNITS	CONDITIONS
V_{OH}	Output High Voltage	2.4		2.4	3.0		2.4		Volts	$V_{CC} = 4.75\ V$, $I_{OH} = -1.2\ mA$ (Pins 7 & 9) $V_{CC} = 4.75\ V$, $I_{OH} = -1.08\ mA$ (Pins 6 & 10) $V_{CC} = 4.75\ V$, $I_{OH} = -0.84\ mA$ (Pins 5 & 11)
V_{OL}	Output Low Voltage		0.45		0.21	0.45		0.45	Volts	$V_{CC} = 5.25\ V$, $I_{OL} = 16\ mA$ (Pins 7 & 9) $I_{OL} = 14.4\ mA$ (Pins 6 & 10) $I_{OL} = 11.2\ mA$ (Pins 5 & 11) $V_{CC} = 4.75\ V$, $I_{OL} = 14.1\ mA$ (Pins 7 & 9) $I_{OL} = 12.7\ mA$ (Pins 6 & 10) $I_{OL} = 9.85\ mA$ (Pins 5 & 11)
V_{IH}	Input High Voltage	1.9		1.8			1.6		Volts	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.85			0.85		0.85	Volts	Guaranteed input low threshold for all inputs
I_F	Input Load Current		−1.6		−1.0	−1.6		−1.6	mA	$V_{CC} = 5.25\ V$, $V_F = 0.45\ V$ $V_R = 5.25\ V$ on other inputs
4 I_F	Input Load Current		−6.4		−4.0	−6.4		−6.4		
I_F	Input Load Current		−1.41		−0.9	−1.41		−1.41	mA	$V_{CC} = 4.75\ V$, $V_F = 0.45\ V$ $V_R = 5.25\ V$ on other inputs
4 I_F	Input Load Current		−5.64		−3.6	−5.64		−5.64		
I_R	Input Leakage Current				15	60		60	µA	$V_{CC} = 5.25\ V$, $V_R = 4.5\ V$ Ground on other inputs
4 I_R	Input Leakage Current				60	240		240		
t_{pd+}	C to C_O				8.0	15			ns	$V_{CC} = 5.0\ V$ $C_L = 15\ pF$ See Fig. 11
t_{pd-}	C to C_O				8.0	15			ns	
t_{pd+}	A_I to S				28	45			ns	
t_{pd-}	A_I to S				25	40			ns	

INPUTS

EQUIVALENT CIRCUIT



OUTPUTS



INPUT CURRENT VS INPUT VOLTAGE

PINS 1, 2, 3, 4, 12, 15

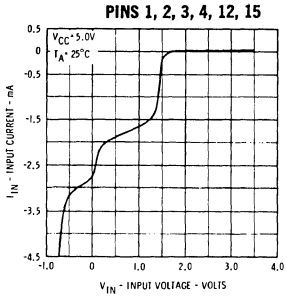


FIG. 4

PINS 13, 14

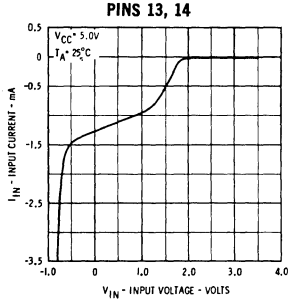


FIG. 3

OUTPUT CURRENT VS OUTPUT VOLTAGE

LOW STATE

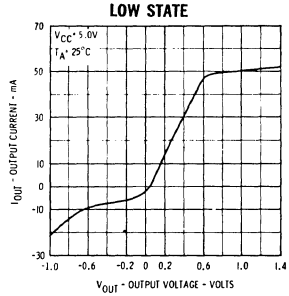


FIG. 5

HIGH STATE

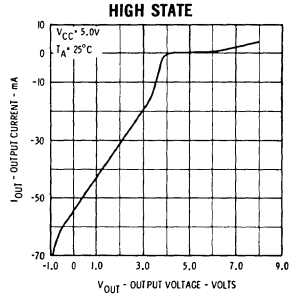


FIG. 6

TYPICAL CARRY TURN ON DELAY TIME VERSUS TEMPERATURE

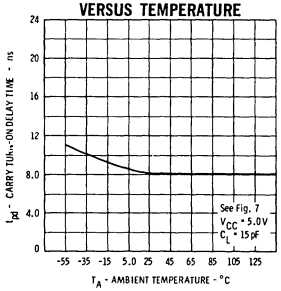


Fig. 7

TYPICAL CARRY TURN OFF DELAY TIME VERSUS TEMPERATURE

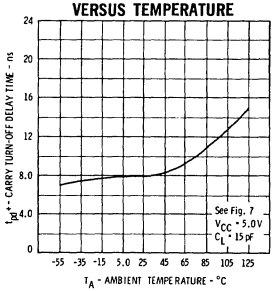


Fig. 8

TYPICAL ADD TURN ON DELAY TIME VERSUS TEMPERATURE

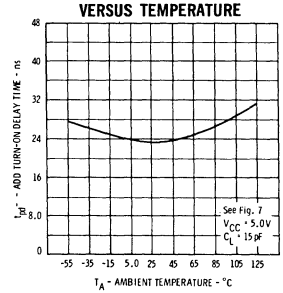


Fig. 9

TYPICAL ADD TURN OFF DELAY TIME VERSUS TEMPERATURE

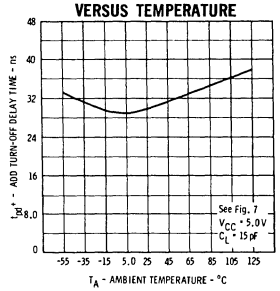
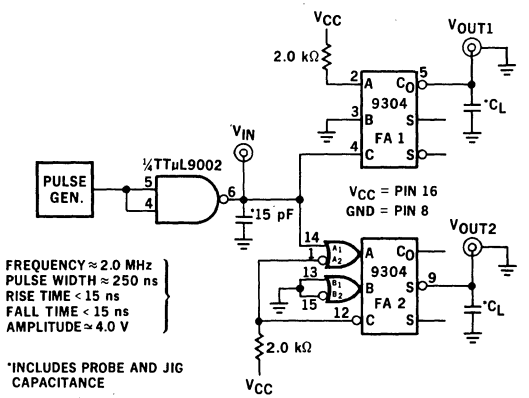


Fig. 10



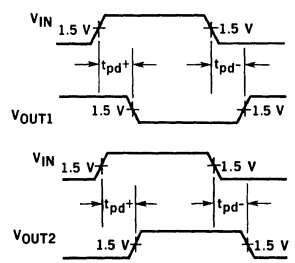


Fig. 11 — SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

APPLICATIONS — The MIC9304 dual adder has been designed to be useful in a wide variety of applications such as addition, parity generation and checking, code conversion, majority gating and other applications for which this combination of logic gates may be useful. The multifunctional capabilities of the MIC9304 dual adder can be seen from reference to the applications shown.

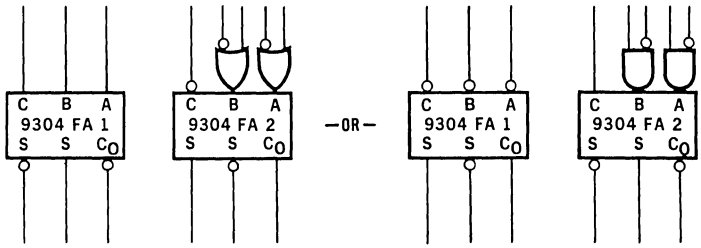


Fig. 12 — FUNCTIONAL BLOCK REPRESENTATION

The principle of duality allows 2 ways of representing each adder. The circuit is the same in both cases but the logic diagrams differ. The dual diagrams facilitate logic design and allow a greater understanding of the capabilities of the device.

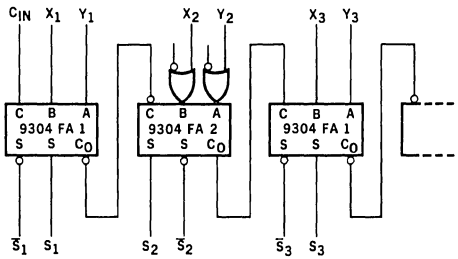


Fig. 13 — RIPPLE CARRY PARALLEL ADDITION

Shown above is a high speed ripple carry parallel addition scheme. Only one and-or-not gate delay is incurred at each stage allowing a typical addition speed of (N+1) x 8 ns, where N is the number of bits in the word. A similar scheme will work if the negation inputs are used, and the design acts as a subtractor when the complement of one variable is provided.

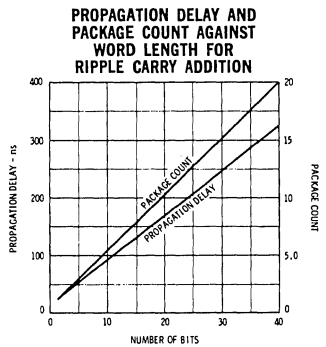


Fig. 14

The curve shows propagation delay of the ripple Carry Adder drawn in Figure 5. Plotted on the same diagram is a curve showing the low package count resulting from this Ripple Scheme.

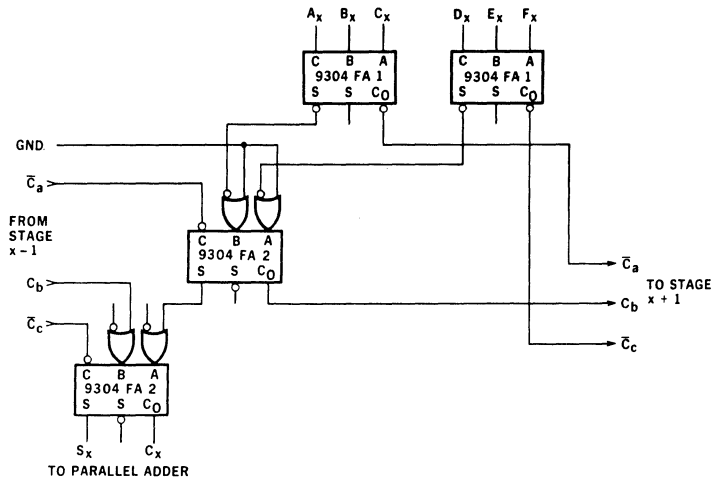


Fig. 15 — ADDITION OF SIX VARIABLES

The above design shows how the MIC9304 can be used in carry save arithmetic. Six input variable are reduced to two where they can be added in a parallel adder. Delay between inputs and outputs is typically 50 ns, allowing extremely high speed computation. Additional variables may be added or the concept can be extended to multiplication, division, and various other arithmetic operations.

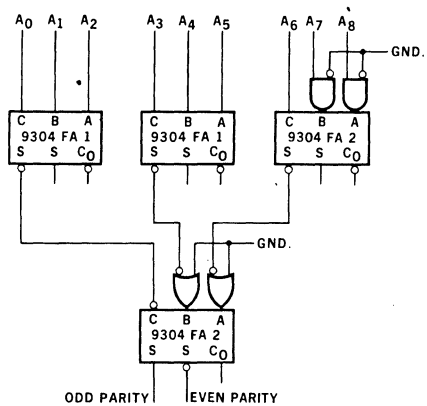


Fig. 16 — BYTE PARITY GENERATION OR CHECKING

The MIC9304 can be used for parity checking or generating. The above design uses 2 MIC9304's to generate parity for an 8 bit byte or check parity over 9 bits. The delay from input to odd parity is typically 35 ns. Additional adder blocks can be used to generate or check parity over larger word lengths. The concept can also be used for hamming and cyclic code generation and checking.

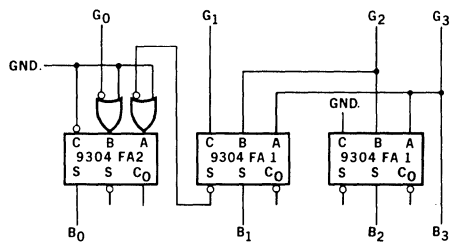


Fig. 17 — 4 BIT PARALLEL GRAY TO BINARY CONVERSION

A 4 bit parallel binary to gray conversion is shown. The adders can also be used for other cyclic code manipulations.

MSI DUAL FOUR-BIT LATCH

- **Active Level Low Enable Gate Inputs**
- **Overriding Master Reset**
- **25 ns Through Delay**
- **The Input/Output Characteristics Provide Direct Interfacing With Fairchild DTμL, LPDTμL, TTμL, and MSI Families (CCSL).**
- **Input Clamp Diodes Limit High Speed Termination Effects.**

The MSI MIC9308 is a Dual 4-Bit Latch designed for general purpose storage applications in high speed digital systems. The MIC9308 uses TTμL technology and is CCSL compatible. All inputs incorporate diode clamps to ground to reduce negative line transients. All outputs have active pull-up circuitry to provide high capacitive drive and low impedance outputs in both logic states to provide good A.C. noise immunity.

ABSOLUTE MAXIMUM RATINGS

(above which the useful life may be impaired)

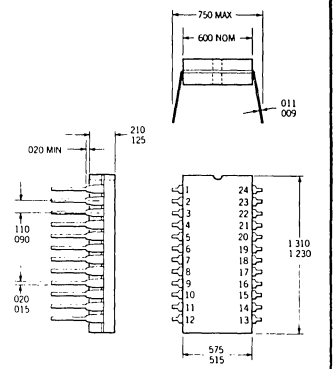
CONDITIONS		UNITS
Storage Temperature	−65 to +150	°C
Temperature (Ambient) Under Bias	−55 to +125	°C
V_{CC} Pin Potential to Ground Pin	−0.5 to +7	Volts
Input Voltage (D.C.) (See Note 1)	−0.5 to +5.5	Volts
Input Current (D.C.) (See Note 1)	−30 to +5	mA
Voltage Applied to Outputs (Output High)	−0.5 to +V_{CC}	value
Output Current (D.C.) (Output Low)	+30	mA

NOTE 1: Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

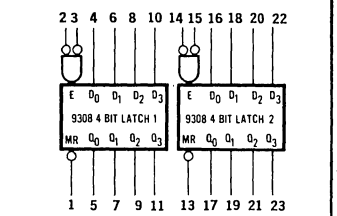
Description of Latch Operation—Data can be entered into the latch when both of the enable inputs are low. As long as this logic condition exists, the output of the latch will follow the input. If either of the enable inputs goes high, the data present in the latch at that time is held in the latch and is no longer affected by the data input.

The master reset overrides all other input conditions and forces the outputs of all the latches low when a low signal is applied to the master reset input.

PHYSICAL DIMENSIONS



LOGIC DIAGRAM



V_{CC} = Pin 24
Gnd = Pin 12

SPECIAL ORDERING CODE

Temperature Range:
−55°C to +125°C, add -1 to MIC number.
0°C to +75°C, add -5 to MIC number.

Case Style:
Ceramic Dual In-Line, 24 leads, add "D" following last digit.

Example:
MIC9301-1D is −55°C to +125°C.
Temperature range in Ceramic Dual-In-Line, 24 lead package.

ELECTRICAL CHARACTERISTICS (T_A = −55°C to +125°C, V_{CC} = 5.0 V ±10%, See Note 1)

SYMBOL	CHARACTERISTICS	LIMITS −55°C MIN.	LIMITS −55°C MAX.	LIMITS +25°C MIN.	LIMITS +25°C TYP.	LIMITS +25°C MAX.	LIMITS +125°C MIN.	LIMITS +125°C MAX.	UNITS	CONDITIONS
V_{OH}	Output High Voltage	2.4		2.4	2.8		2.4		Volts	V_{CC} = 4.5 V, I_{OH} = −0.6 mA Inputs at threshold voltages (V_{IL} or V_{IH}) (See Note 2)
V_{OL}	Output Low Voltage		0.4		0.21	0.4		0.4	Volts	V_{CC} = 5.5 V, I_{OL} = 14.4 mA V_{CC} = 4.5 V, I_{OL} = 11.2 mA Inputs at threshold voltages (V_{IL} or V_{IH}) (See Note 2)
V_{IH}	Input High Voltage	2.0		1.7			1.4		Volts	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.8			0.9		0.8	Volts	Guaranteed input low threshold for all inputs
I_F	Input Load Current E_0, E_I and MR Inputs		−1.6		−1.1	−1.6		−1.6	mA	V_{CC} = 5.5 V, V_F = 0.4 V
1.5 I_F	Input Load Current D Inputs		−2.7		−1.9	−2.7		−2.7		V_F = 0.0 V (See Note 3)
I_R	Input Leakage Current E_0, E_I and MR Inputs				10	60		60	μA	V_{CC} = 5.5 V, V_R = 4.5 V
1.5 I_R	Input Leakage Current D Inputs				15	90		90		
I_{PD}	Power Supply Current		90		65	90		90	mA	V_{CC} = 5.0 V all outputs low inputs disabled

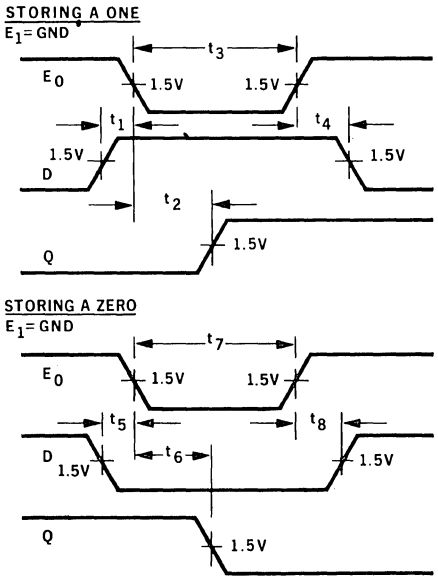
ELECTRICAL CHARACTERISTICS (T_A = 0°C to +75°C, V_{CC} = 5.0 V ±5%, See Note 1)

SYMBOL	CHARACTERISTICS	LIMITS 0°C MIN.	LIMITS 0°C MAX.	LIMITS +25°C MIN.	LIMITS +25°C TYP.	LIMITS +25°C MAX.	LIMITS +75°C MIN.	LIMITS +75°C MAX.	UNITS	CONDITIONS
V_{OH}	Output High Voltage	2.4		2.4	3.1		2.4		Volts	V_{CC} = 4.75 V, I_{OUT} = −0.6 mA Inputs at threshold voltages (V_{IL} or V_{IH}) (See Note 2)
V_{OL}	Output Low Voltage		0.45		0.21	0.45		0.45	Volts	V_{CC} = 5.25 V, I_{OUT} = 14.4 mA V_{CC} = 4.75 V, I_{OUT} = 12.7 mA Inputs at threshold voltages (V_{IL} or V_{IH}) (See Note 2)
V_{IH}	Input High Voltage	1.9		1.8			1.6		Volts	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.85			0.85		0.85	Volts	Guaranteed input low threshold for all inputs
I_F	Input Load Current E_0, E_I and MR Inputs		−1.6		−1.0	−1.6		−1.6	mA	V_{CC} = 5.25 V, V_F = 0.45 V
1.5 I_F	Input Load Current D Inputs		−2.7		−1.8	−2.6		−2.7		V_F = 0.0 V (See Note 3)
I_R	Input Leakage Current E_0, E_I and MR Inputs				10	60		60	μA	V_{CC} = 5.25 V, V_R = 4.5 V
1.5 I_R	Input Leakage Current D Inputs				15	90		90		
I_{PD}	Power Supply Current		117		65	117		117	mA	V_{CC} = 5.0 V all outputs low inputs disabled

NOTE 1: Units are pulse tested.
NOTE 2: Output Voltages are guaranteed for either the input enabled or input disabled case.
NOTE 3: This current is measured at $V_{IN} \doteq 0.0$ V to insure that no current is being absorbed by the device internally. The maximum value given guarantees that the maximum instantaneous current that can flow out of the input at V_{IN} = 0.4 V is 2.4 mA.

A.C. CHARACTERISTICS

9308 SWITCHING WAVEFORMS



TIME	DEFINITION	LIMIT (See Note 4)			
		MIN.	TYP.	MAX.	UNITS
t_1	Min. time that data must be present before enable to not increase t_2	X	minus 4	—	ns
t_2	Delay from enable to output turning off	—	22	X	ns
t_3	Min. enable pulse width to store a ONE	X	15	—	ns
t_4	Min. time that data must remain constant after removal of enable	X	5	—	ns
t_5	Min. time that data must be present before enable to not increase t_6	X	0	—	ns
t_6	Delay from enable to output turning on	—	15	X	ns
t_7	Min. enable pulse width to store a ZERO	X	15	—	ns
t_8	Min. time that data must remain constant after removal of enable	X	2	—	ns

NOTE 4: Limits indicated by X will be shown on final data sheets.

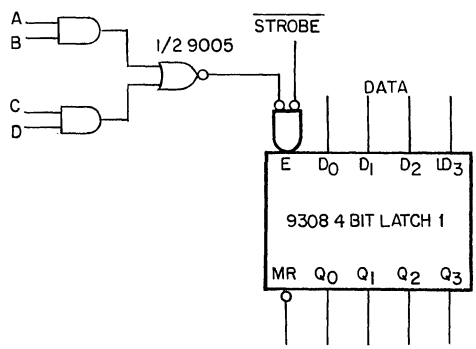
All delays are measured with V_{CC} = 5.0 V applied to Pin 24 and Pin 12 grounded. The active input is driven by a 9002 $TT_{\mu}L$ gate with the output loaded with 15 pF. All outputs are loaded with 15 pF.

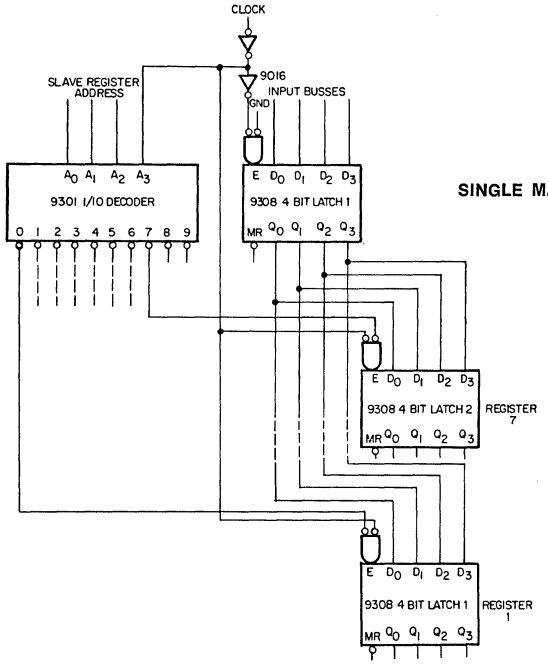
LOADING RULES

	PIN	LOADING
INPUTS	D_0, D_1, D_2, D_3	1.5
	MR, E_0, E_1	1.0
OUTPUTS	Q_0, Q_1, Q_2, Q_3	9.0

APPLICATIONS

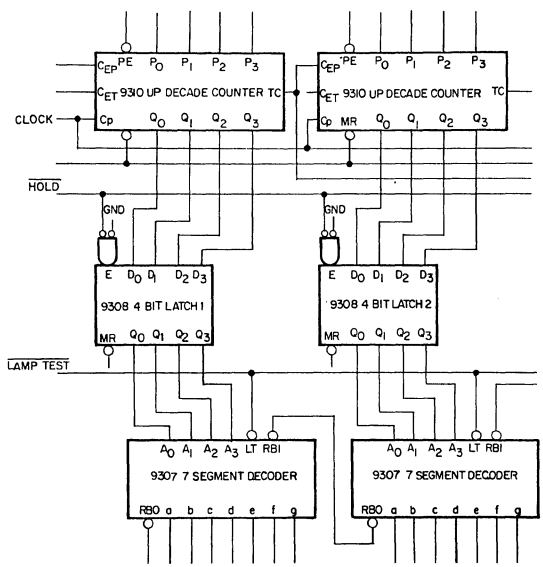
AND-OR ENABLE SHOWING ACTIVE LEVEL LOW ENABLE GATE UTILITY





SINGLE MASTER/MULTIPLE SLAVE FLIP-FLOP

MIC9308 AS A HOLDING REGISTER IN COUNTING & DISPLAY APPLICATION



MSI DUAL FOUR-INPUT MULTIPLEXER

- **Multifunction Capability**
- **25 ns Through Delay**
- **On-Chip Select Logic Decoding**
- **Fully Buffered Complementary Outputs**
- **The Input/Output Characteristics Provide Easy Interfacing with DTL930, TTL9000, TTL7400 and MSI Families**
- **Input Clamp Diodes Limit High Speed Termination Effects**

The MIC9309 is a monolithic, high speed, dual four-input digital multiplexer circuit, constructed with a planar epitaxial process. It consists of two multiplexing circuits with common input select logic, each circuit contains four inputs and fully buffered complementary outputs. In addition to operating as a multiplexer, the MIC9309 can generate any two functions of three variables. Active pullups in the outputs ensure high drive and high speed performance. Because of its high speed performance and on-chip select decoding, the MIC9309 may be cascaded to multiple levels so that any number of lines can be multiplexed onto a single output buss. The circuit uses TTL for high speed, high fanout operation and is compatible with all DTL, and TTL digital integrated circuits.

ABSOLUTE MAXIMUM RATINGS

(above which the useful life may be impaired)

CHARACTERISTICS		UNITS
Storage Temperature	−65°C to +150	°C
Temperature (Ambient) Under Bias	−55°C to +125	°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7	Volts
Voltage Applied to Output when output is high	0.V to +V_{CC}	value
Input Voltage (DC) (See Note 1)	−0.5 V to +5.5	Volts
Input Current (DC) (See Note 1)	−30 mA to +5	mA
Current into Output when output is low	+30	mA

Note 1: Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

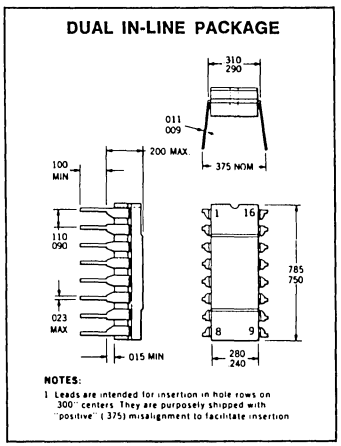


Fig. 1

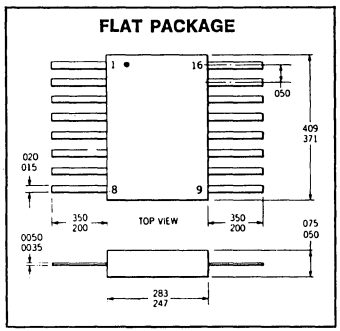


Fig. 2

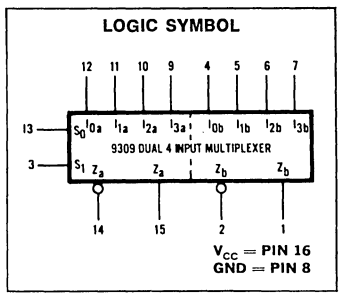
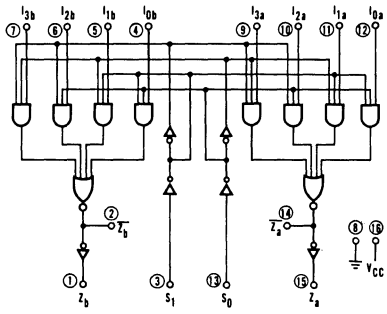


Fig. 3

LOGIC DIAGRAM



9309
Dual four input multiplexer
Logic diagram

Fig. 4

FUNCTIONAL DESCRIPTION

The MIC9309 dual four input multiplexer is a member of the ITT family of compatible Medium Scale Integrated (MSI) digital building blocks. It provides this family with the ability to select two bits of either data or control from up to four sources, in one package.

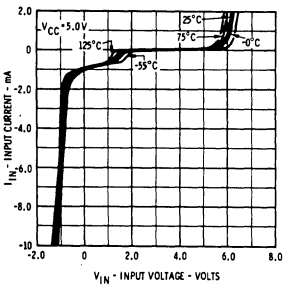
The MIC9309 dual four input multiplexer is the logical implementation of a two-pole four-position switch, with the position of the switch being set by the logic levels supplied to the two select inputs. Both assertion and negation outputs are provided for both multiplexers. The logic equations for the outputs are shown below:

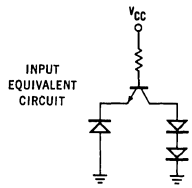
$$Z_a = I_{0a} \cdot \overline{S}_1 \cdot \overline{S}_0 + I_{1a} \cdot \overline{S}_1 \cdot S_0 + I_{2a} \cdot S_1 \cdot \overline{S}_0 + I_{3a} \cdot S_1 \cdot S_0$$
$$Z_b = I_{0b} \cdot \overline{S}_1 \cdot \overline{S}_0 + I_{1b} \cdot \overline{S}_1 \cdot S_0 + I_{2b} \cdot S_1 \cdot \overline{S}_0 + I_{3b} \cdot S_1 \cdot S_0$$

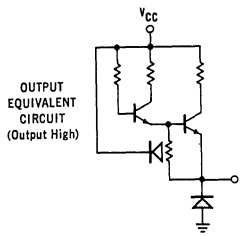
A common use of the MIC9309 would be the moving of data from a group of registers to a common output buss. The particular register from which the data came would be determined by the state of the select inputs. A less obvious use is as a function generator. The MIC9309 can generate any two functions of three variables. This is useful for implementing random gating functions.

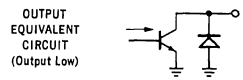
TYPICAL INPUT AND OUTPUT CHARACTERISTICS

Fig. 5 INPUT CURRENT VERSUS INPUT VOLTAGE









TRUTH TABLE

SELECT INPUTS		INPUTS				OUTPUTS	
S_0	S_1	I_{0a}	I_{1a}	I_{2a}	I_{3a}	Z_a	$\overline{Z}_a$
L	L	L	X	X	X	L	H
L	L	H	X	X	X	H	L
H	L	X	L	X	X	L	H
H	L	X	H	X	X	H	L
L	H	X	X	L	X	L	H
L	H	X	X	H	X	H	L
H	H	X	X	X	L	L	H
H	H	X	X	X	H	H	L
S_0	S_1	I_{0b}	I_{1b}	I_{2b}	I_{3b}	Z_b	$\overline{Z}_b$
L	L	L	X	X	X	L	H
L	L	H	X	X	X	H	L
H	L	X	L	X	X	L	H
H	L	X	H	X	X	H	L
L	H	X	X	L	X	L	H
L	H	X	X	H	X	H	L
H	H	X	X	X	L	L	H
H	H	X	X	X	H	H	L

L = low voltage level
H = high voltage level
X = either high or low logic level

Fig. 6 OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (OUTPUT HIGH)

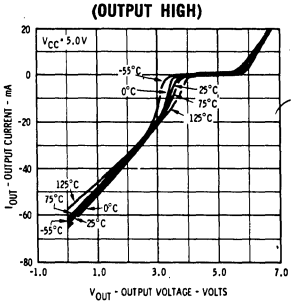
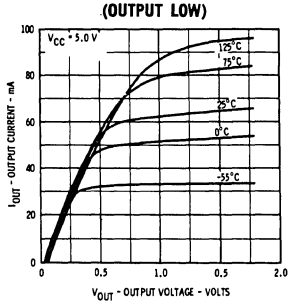


Fig. 7 OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (OUTPUT LOW)



LOADING RULES

(1 U.L. = 1 TTL gate input load)

INPUTS	LOADING
I_{0a}, I_{1a}, I_{2a}, I_{3a}, I_{0b}, I_{1b}, I_{2b}, I_{3b}, S_0, S_1	1 U.L.

OUTPUTS	FANOUT AT LOGIC LEVEL HIGH	LOW
Z_a, Z_b	20 U.L.	10 U.L.
$\overline{Z}_a$, $\overline{Z}_b$	18 U.L.	9 U.L.

ELECTRICAL CHARACTERISTICS* (MIC9309-1X) ($T_A = -55°C$ to $+125°C$, $V_{CC} = 5.0\ V \pm 10\%$)

SYMBOL	CHARACTERISTICS	LIMITS −55°C MIN.	LIMITS −55°C MAX.	LIMITS +25°C MIN.	LIMITS +25°C TYP.	LIMITS +25°C MAX.	LIMITS +125°C MIN.	LIMITS +125°C MAX.	UNITS	CONDITIONS
V_{OH}	Output High Voltage	2.4		2.4	2.7		2.4		Volts	$V_{CC} = 4.5\ V$ $I_{OH} = -1.2$ mA (Pins 1 & 15) $V_{CC} = 4.5\ V$ $I_{OH} = -1.08$ mA (Pins 2 & 14) Inputs at threshold voltages (V_{IL} or V_{IH}) as per truth table
V_{OL}	Output Low Voltage		0.4		0.21	0.4		0.4	Volts	$V_{CC} = 5.5\ V$ $I_{OL} = 16.0$ mA (Pins 1 & 15) $I_{OL} = 14.4$ mA (Pins 2 & 14) $V_{CC} = 4.5\ V$ $I_{OL} = 12.4$ mA (Pins 1 & 15) $I_{OL} = 11.2$ mA (Pins 2 & 14) Inputs at threshold voltages (V_{IL} or V_{IH}) as per truth table
V_{IH}	Input High Voltage	2.0		1.7			1.4		Volts	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.8			0.9		0.8	Volts	Guaranteed input low threshold for all inputs
I_F (all inputs)	Input Load Current		−1.6 −1.24		−1.1 −.85	−1.6 −1.24		−1.6 −1.24	mA mA	$V_{CC} = 5.5\ V$ $V_F = 0.4\ V$ $V_{CC} = 4.5\ V$ Input selected
I_R (all inputs)	Input Leakage Current				15	60		60	μA	$V_{CC} = 5.5\ V$ $V_R = 4.5\ V$ Input not selected
I_{PDH}	V_{CC} Current		40		30	40		40	mA	$V_{CC} = 5.0\ V$ All inputs high
t_{pd+} (S_0 to Z_a)	Switching Speed				24	32			ns	$V_{CC} = 5.0\ V$, $C_L = 15$ pF, See Figure 8
t_{pd-} (S_0 to Z_a)	Switching Speed				24	32			ns	

*Pulse tested

ELECTRICAL CHARACTERISTICS* (MIC9309-5X) ($T_A = 0°C$ to $+75°C$, $V_{CC} = 5.0\ V \pm 5\%$)

SYMBOL	CHARACTERISTICS	LIMITS 0°C MIN.	LIMITS 0°C MAX.	LIMITS +25°C MIN.	LIMITS +25°C TYP.	LIMITS +25°C MAX.	LIMITS +75°C MIN.	LIMITS +75°C MAX.	UNITS	CONDITIONS
V_{OH}	Output High Voltage	2.4		2.4	3.0		2.4		Volts	$V_{CC} = 4.75\ V$ $I_{OH} = -1.2$ mA (Pins 1 & 15) $V_{CC} = 4.75\ V$ $I_{OH} = -1.08$ mA (Pins 2 & 14) Inputs at threshold voltages (V_{IL} or V_{IH}) as per truth table
V_{OL}	Output Low Voltage		0.45		0.21	0.45		0.45	Volts	$V_{CC} = 5.25\ V$ $I_{OL} = 16.0$ mA (Pins 1 & 15) $I_{OL} = 14.4$ mA (Pins 2 & 14) $V_{CC} = 4.75\ V$ $I_{OL} = 14.1$ mA (Pins 1 & 15) $I_{OL} = 12.7$ mA (Pins 2 & 14) Inputs at threshold voltages (V_{IL} or V_{IH}) as per truth table
V_{IH}	Input High Voltage	1.9		1.8			1.6		Volts	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.85			0.85		0.85	Volts	Guaranteed input low threshold for all inputs
I_F (all inputs)	Input Load Current		−1.6 −1.41		−1.0 −.91	−1.6 −1.41		−1.6 −1.41	mA mA	$V_{CC} = 5.25\ V$ $V_F = 0.45\ V$ $V_{CC} = 4.75\ V$ Input selected
I_R (all inputs)	Input Leakage Current				15	60		60	μA	$V_{CC} = 5.25\ V$ $V_R = 4.5\ V$ Input not selected
I_{PDH}	V_{CC} Current		43		30	43		43	mA	$V_{CC} = 5.0\ V$ All inputs high
t_{pd+} (S_0 to Z_a)	Switching Speed				24	36			ns	$V_{CC} = 5.0\ V$, $C_L = 15$ pF, See Figure 8
t_{pd-} (S_0 to Z_a)	Switching Speed				24	36			ns	

*Pulse tested

A.C. CHARACTERISTICS

SWITCHING WAVEFORMS

All inputs are outputs of TTL MIC9000 series gates loaded with 15 pF. All outputs are loaded with the same capacitance (referred to as C_L) and only with capacitance.

t_{pd}; S_0 to Z_a
CONDITIONS
Pins 3, 12 = GND.
Pin 11 = V_{CC}

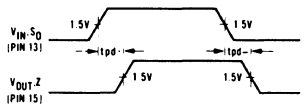


Fig. 8

t_{pd}; S_0 to $\overline{Z}_a$
CONDITIONS
Pins 3, 12 = GND.
Pin 11 = V_{CC}

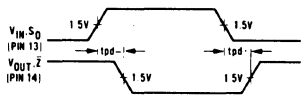


Fig. 9

t_{pd}; I_{a0} to $\overline{Z}_a$
CONDITIONS
Pins 3, 13 = GND.

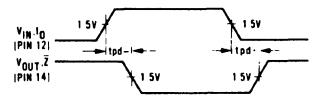


Fig. 10

SWITCHING CHARACTERISTICS

TURN OFF DELAY TIME VERSUS AMBIENT TEMPERATURE (S_0 to Z_a)

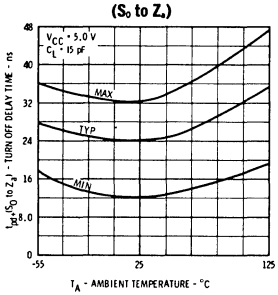


Fig. 11

TURN ON DELAY TIME VERSUS TEMPERATURE (S_0 to Z_a)

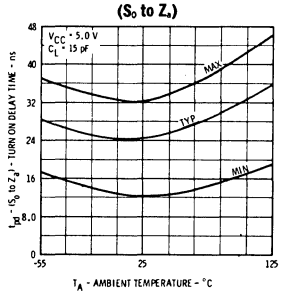


Fig. 12

TURN OFF DELAY TIME VERSUS AMBIENT TEMPERATURE (I_{0a} to $\overline{Z}_a$)

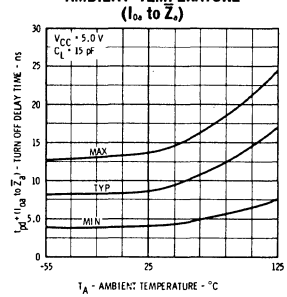


Fig. 13

TURN ON DELAY TIME VERSUS AMBIENT TEMPERATURE (I_{0a} to $\overline{Z}_a$)

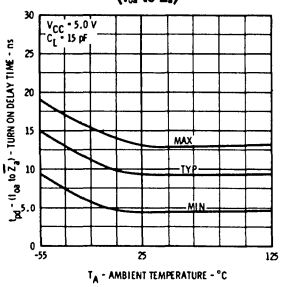


Fig. 14

TURN OFF DELAY TIME VERSUS AMBIENT TEMPERATURE (S_0 to $\overline{Z}_a$)

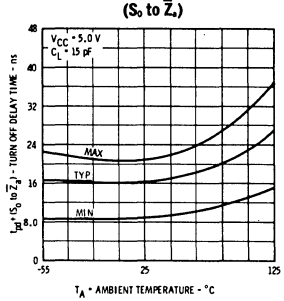


Fig. 15

TURN ON DELAY TIME VERSUS AMBIENT TEMPERATURE (S_0 to $\overline{Z}_a$)

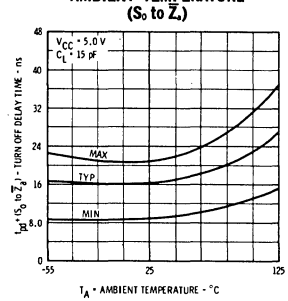


Fig. 16

APPLICATIONS

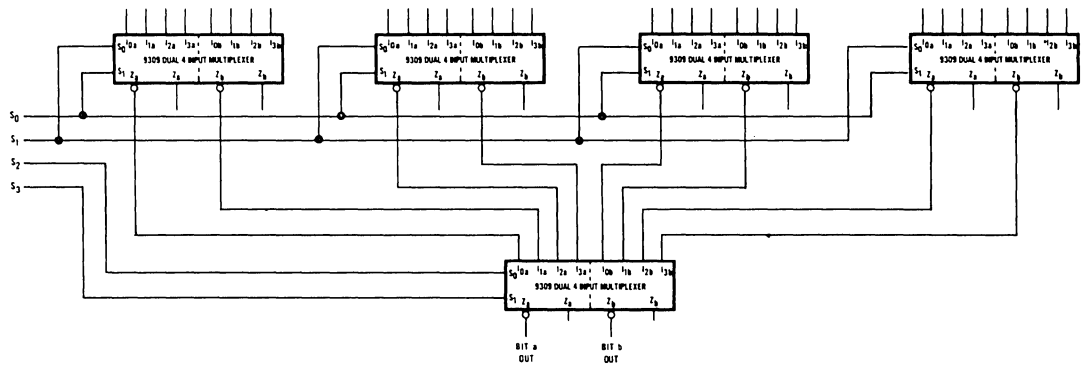
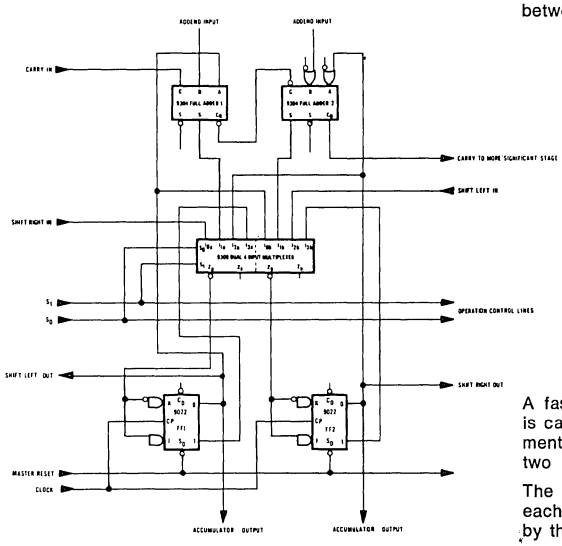


Fig. 12 — MULTIPLEXING TWO BITS FROM SIXTEEN SOURCES

This diagram shows the interconnection of five MIC9309 dual four bit multiplexers to provide switching of two bits of data from one of sixteen words onto a two bit data buss. The selection of which word will be transferred to the buss is made by the address supplied to the S_0, S_1, S_2 and S_3 inputs. As an example: if twelve bit words are to be transferred to a twelve bit buss, the above diagram would be repeated six times. Notice that the negative outputs are used at both levels resulting in the assertion output (negation of the negation) at a higher speed due to the fact that the through delay is less on the negation output.

If the word selecting address is held in four TTL flip flops (two dual packages) enough load capability is available to select between sixteen, sixteen bit words.



OPERATION CODE LIST

S_0	S_1	INSTRUCTION
0	0	SHIFT LEFT
1	0	ADD
0	1	SHIFT RIGHT
1	1	COMPLEMENT

H = "1", L = "0"

Fig. 13 — GENERAL PURPOSE ACCUMULATOR

A fast, general purpose accumulator for computer applications is capable of : 1) shift left; 2) add; 3) shift right and 4) complement operations. Only three packages are required to construct two stages of the general purpose accumulator shown above.

The D input capability of the MIC9022 is utilized here to allow each flip flop of the accumulator to accept the data as presented by the MIC9309 multiplexer.

Under the operation code instructions the multiplexer provides an input to the MIC9022 from: 1) adjacent stage to the right for a shift left operation; 2) adjacent stage to the left for a shift right operation; 3) output of adders for add operation and 4) Q outputs of MIC9022 for the complement operation. The operation code at the right of Figure 13 shows the instruction codes to perform the various operations. The accumulator should be capable of 20-25MHz operation.

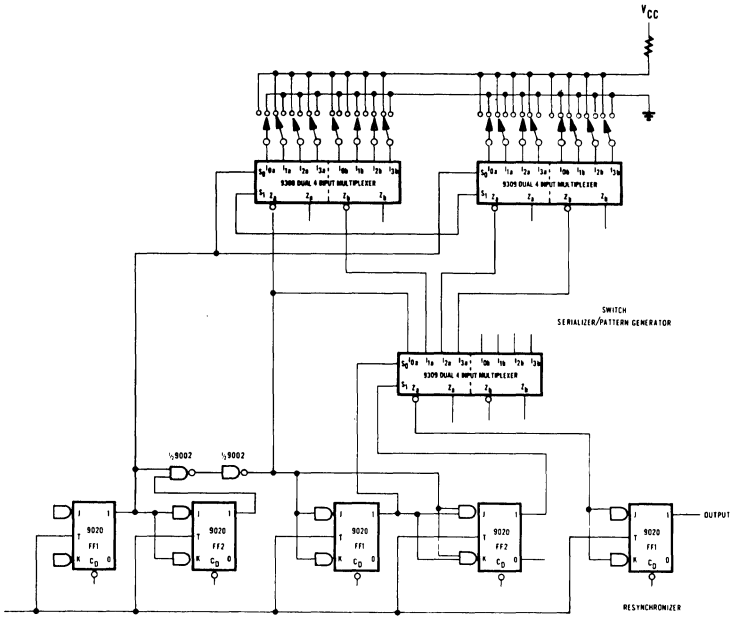


Fig. 14 — 16-BIT PATTERN GENERATOR

This application illustrates the use of MIC9309 and MIC9020 in the design of one channel of a 16 bit pattern generator. Each channel requires ½ MIC9020, ½ MIC9002 and 2½ MIC9309. Each channel consists of a switch serializer/pattern generator and resynchronizer sections with a modulo 16 binary counter common to all channels.

The two least significant bits and two most significant bits of the counter control the first and second stages of multiplexing respectively. In this manner four bits are multiplexed on each of the four lines from the first stage to the second stage. Every four clock times a new input line containing four multiplexed bits is selected by the second stage of the serializer thus serializing the 16 input bits from the switches.

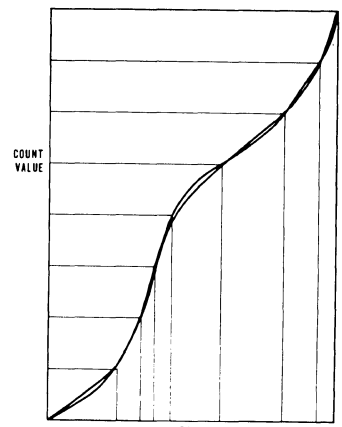
The resynchronizer flip flop is used to eliminate decoding spikes.

SPECIAL ORDERING CODE

Temperature Range:
−55°C to +125°C, add -1 to MIC number.
0°C to +75°C, add -5 to MIC number.

Case Style:
¼" x ⅜" Flat Pack, add "B" following last digit.
Ceramic Dual In-Line, 16 leads, add "D" following last digit.

Example:
MIC9309-1D is −55°C to +125°C. Temperature range in Ceramic Dual-In-Line, 16 lead package.
Flat-pack and Dual-In-Line packages have same pin configuration.



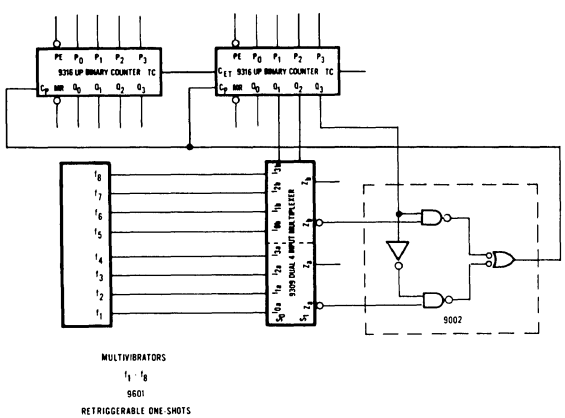


Fig. 15 — NON-LINEAR COUNTER

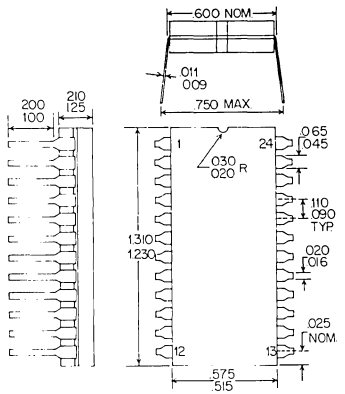
The rate of the non-linear counter depends on the multivibrator clock frequency selected under control of the three most significant bits of the counter. This makes the count rate a function of both the count value of counter and frequency of clock multivibrator selected.

Clock multiplexing is accomplished by a MIC9309 dual 4-input multiplexer and one MIC9002 quad gate. Eight line segments representing clock rates of the multivibrators may be adjusted in slope to approximate a non-linear function.

MSI ONE-OF-SIXTEEN DECODER

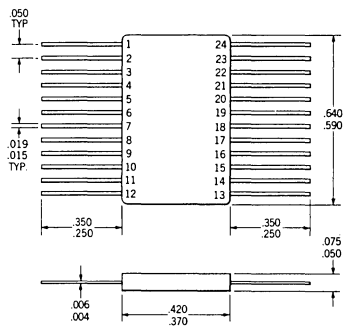
- **Multi-function capability**
- **Mutually exclusive outputs**
- **Guaranteed fanout of 10 TTL loads over the full temperature range and supply voltage ranges**
- **High capacitive drive capability**
- **Demultiplexing capability**
- **Typical power dissipation of 175 mW**
- **The input/output characteristics provide easy interfacing with DTL, 930 and TTL 54/7400 and 9300 families**
- **All ceramic "Hermetic" 24-pin dual in-line package**
- **Input clamp diodes limit high speed line termination effects**
- **Two input enable gate**

DUAL IN-LINE PACKAGE

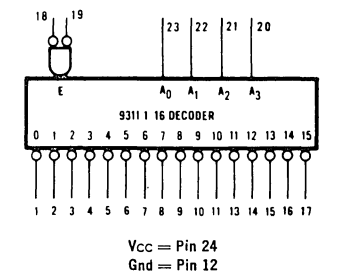


NOTES: All dimensions are in inches. Leads are intended for insertion in hole rows on .600 centers. They are purposely shipped with "positive" misalignment to facilitate insertion. Board drilling dimensions should equal your practice for .020 inch diameter lead. Leads are gold-plated Kovar. Package weight is 6.5 grams.

FLAT PACKAGE



LOGIC SYMBOL



V_{CC} = Pin 24
Gnd = Pin 12

The MIC9311 is a multi-purpose decoder designed to accept four inputs and provide 16 mutually exclusive outputs. The circuit uses TTL for high speed and high fan-out capability, and is compatible with all members of the 930 DTL, 54/7400 and 9300 families.

ABSOLUTE MAXIMUM RATINGS

(above which the useful life may be impaired)

CHARACTERISTICS		UNITS
Storage Temperature	−65 to +150	°C
Temperature (Ambient) Under Bias	−55 to +125	°C
V_{CC} Pin Potential to Ground Pin	−0.5 to +7	Volts
Voltage Applied to Outputs for high output state	−0.5 V to +V_{CC}	value
Input Voltage (D.C.)	−0.5 to +5.5	Volts

FUNCTIONAL DESCRIPTION — The 9311 decoder accepts four active high BCD inputs and provides 16 mutually exclusive active low outputs, as shown by Figure 1. The active low outputs facilitate memory addressing when inverting drivers are used between decoder and memory elements such as the 9033.

The most significant A_3 input produces a useful inhibit function when the 9311 is used as a 1 out of 8 decoder.

ELECTRICAL CHARACTERISTICS ($T_A = -55°C$ to $+125°C$, $V_{CC} = 5.0\ V \pm 10\%$) See Note 1

SYMBOL	CHARACTERISTICS	LIMITS −55°C MIN.	−55°C MAX.	+25°C MIN.	+25°C TYP.	+25°C MAX.	+125°C MIN.	+125°C MAX.	UNITS	CONDITIONS
V_{OH}	Output High Voltage	2.4		2.4	2.7		2.4		Volts	$V_{CC} = 4.5\ V$, $I_{OH} = -0.6\ mA$
V_{OL}	Output Low Voltage		0.4		0.2	0.4		0.4	Volts	$V_{CC} = 4.5\ V$, $I_{OL} = 12.4\ mA$ $V_{CC} = 5.5\ V$, $I_{OL} = 16.0\ mA$
V_{IH}	Input High Voltage	2.0		1.7			1.4		Volts	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.8			0.9		0.8	Volts	Guaranteed input low threshold for all inputs
I_F	Input Load Current		−1.6		−1.10	−1.6		−1.6	mA	$V_{CC} = 5.5\ V$, $V_F = 0.4\ V$
			−1.24		−0.97	−1.24		−1.24	mA	$V_{CC} = 4.5\ V$
I_R	Input Leakage Current				15	60		60	μA	$V_{CC} = 5.5\ V$, $V_R = 4.5\ V$
I_{PD}	V_{CC} Current				35	55			mA	$V_{CC} = 5.0\ V$
t_{pd+}	Turn Off Delay A Input to Output				23	35			ns	$V_{CC} = 5.0\ V$ $C_L = 15\ pF$ See test circuit
t_{pd-}	Turn On Delay A Input to Output				20	30			ns	
t_{pd+}	Turn Off Delay E Input to Output				17	26			ns	
t_{pd-}	Turn On Delay E Input to Output				16	21			ns	

Note 1: Units are pulse tested.

TRUTH TABLE

Eo	EI	A_0	A_1	A_2	A_3	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
H	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	L	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	H	L	L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	H	H	L	L	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	L	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H
L	L	H	H	H	L	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H
L	L	H	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H
L	L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H
L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H
L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H
L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L

H = High Voltage Level
L = Low Voltage Level
X = Level Does Not Affect Output

TTL INPUT LOAD AND DRIVE FACTORS

INPUTS	LOADING
All Inputs	1 U.L.

OUTPUTS	DRIVE FACTOR
All Outputs	10 U.L.

(1 U.L. = TTL Gate Input Load)

INPUT LOAD AND DRIVE FACTORS

GRADE	INPUTS	LOADING
59	All Inputs	12/11
51	All Inputs	12/10

GRADE	OUTPUTS	DRIVE FACTOR
59	All Outputs	120/94
51	All Outputs	120/78

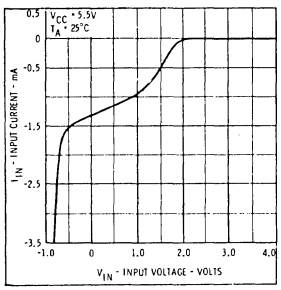
ELECTRICAL CHARACTERISTICS ($T_A = 0°C$ to $+75°C$, $V_{CC} = 5.0\ V \pm 5\%$) See Note 1

SYMBOL	CHARACTERISTICS	LIMITS 0°C MIN.	0°C MAX.	+25°C MIN.	+25°C TYP.	+25°C MAX.	+75°C MIN.	+75°C MAX.	UNITS	CONDITIONS
V_{OH}	Output High Voltage	2.4		2.4	3.0		2.4		Volts	$V_{CC} = 4.75\ V$, $I_{OH} = -0.6\ mA$
V_{OL}	Output Low Voltage		0.45		0.2	0.45		0.45	Volts	$V_{CC} = 4.75\ V$, $I_{OL} = 14.1\ mA$ $V_{CC} = 5.25\ V$, $I_{OL} = 16.0\ mA$
V_{IH}	Input High Voltage	1.9		1.8			1.6		Volts	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.85			0.85		0.85	Volts	Guaranteed input low threshold for all inputs
I_F	Input Load Current		−1.6		−1.0	−1.6		−1.6	mA	$V_{CC} = 5.25\ V$, $V_F = 0.45\ V$
			−1.41		−0.9	−1.41		−1.41	mA	$V_{CC} = 4.75\ V$
I_R	Input Leakage Current				15	60		60	μA	$V_{CC} = 5.25\ V$, $V_R = 4.5\ V$
I_{PD}	V_{CC} Current				35	60			mA	$V_{CC} = 5.0\ V$
t_{pd+}	Turn Off Delay A Input to Output			10	23	40			ns	$V_{CC} = 5.0\ V$ $C_L = 15\ pF$ See test circuit
t_{pd-}	Turn On Delay A Input to Output			7.0	20	35			ns	
t_{pd+}	Turn Off Delay E Input to Output			10	17	31			ns	
t_{pd-}	Turn On Delay E Input to Output			7.0	17	26			ns	

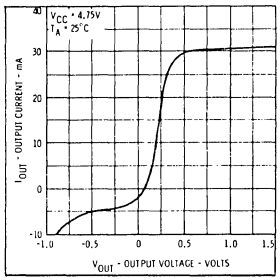
Note 1: Units are pulse tested.

TYPICAL INPUT AND OUTPUT CHARACTERISTICS

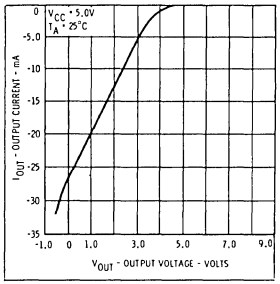
INPUT CURRENT VERSUS INPUT VOLTAGE

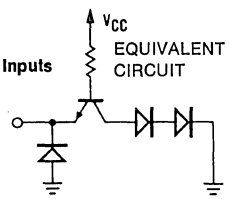


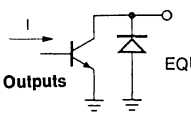
OUTPUT CURRENT VERSUS OUTPUT VOLTAGE OUTPUT LOW

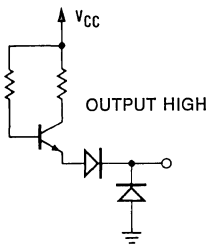


OUTPUT CURRENT VERSUS OUTPUT VOLTAGE OUTPUT HIGH





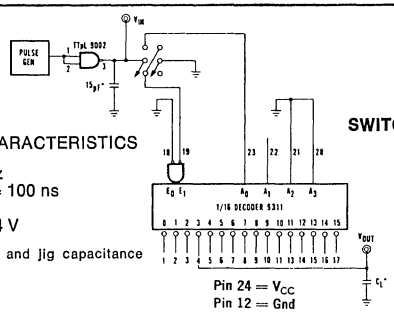




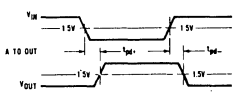
PULSE GEN CHARACTERISTICS

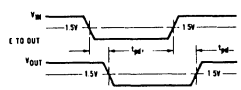
Freq. ≈ 1 MHz
Pulse Width ≈ 100 ns
$t_r = t_f \leq 15$ ns
Amplitude ≈ 4 V

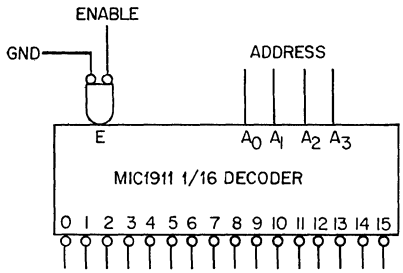
*Includes all probe and jig capacitance



SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



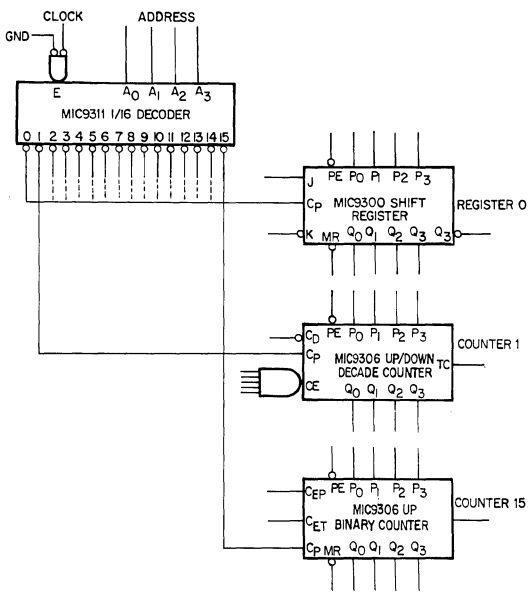




DECODE ANY BCD CODE

Decode any BCD code using a 9311 element. Any 4 bit BCD code may be decoded by selecting outputs, examples are shown in the table.

DECIMAL DIGIT	OUTPUT SELECTION			
	BCD CODE			
	8421	5421	EXCESS 3	GRAY
0	0	0	3	0
1	1	1	4	1
2	2	2	5	3
3	3	3	6	2
4	4	4	7	6
5	5	8	8	7
6	6	9	9	5
7	7	10	10	4
8	8	11	11	12
9	9	12	12	13

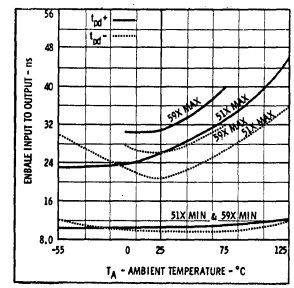


CLOCK DEMULTIPLEXING

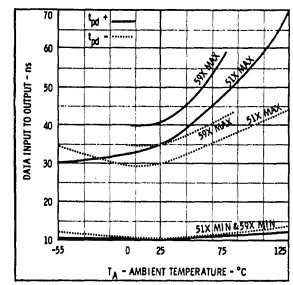
The 9311 can be used as a clock demultiplexer. The binary address designates to which register or counter the clock is sent. Up to 5 register counter stages can be driven by one decoder output allowing word lengths of 20 bits to be controlled. Any sequential circuit in the 9300 MSI family can be used in this configuration.

SWITCHING PERFORMANCE

PROPAGATION DELAY ENABLE INPUT TO OUTPUT VERSUS TEMPERATURE



PROPAGATION DELAY DATA INPUT TO OUTPUT VERSUS TEMPERATURE



SPECIAL ORDERING CODE

Temperature Range:
−55° C to +125° C, add -1 to MIC number.
0° C to +75° C, add -5 to MIC number.

Case Style:
½" x ⅜" Flat Pack, add "B" following last digit.
Ceramic Dual In-Line, 24 leads, add "D" following last digit.

Example:
MIC9311-1D is −55°C to +125°C. Temperature range in Ceramic Dual-In-Line, 24 lead package.
Flat-pack and Dual-In-Line packages have same pin configuration.

MSI EIGHT-INPUT MULTIPLEXER

- **Multifunction Capability**
- **25 ns Through Delay**
- **On-Chip Select Logic Decoding**
- **Fully Buffered Complementary Outputs**
- **The Input/Output Characteristics Provide Easy Interfacing with DTL930, TTL9000, TTL7400 and MSI Families**
- **Input Clamp Diodes Limit High Speed Termination Effects**

The MIC9312 is a monolithic, high speed, eight input digital multiplexer circuit. It provides in one package the ability to select one bit of data from up to eight sources. The MIC9312 can be used as a universal function generator to generate any logic function of four variables. Both assertion and negation outputs are provided. TTL circuitry with active pullups on the outputs provides high speed, high fanout operation and is compatible with all DTL and TTL digital integrated circuits.

ABSOLUTE MAXIMUM RATINGS

(above which the useful life may be impaired)

CHARACTERISTICS		UNITS
Storage Temperature	−65°C to +150	°C
Temperature (Ambient) Under Bias	−55°C to +125	°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7	Volts
Voltage applied to Output when output is high	0 V to $+V_{CC}$	value
Input Voltage (DC) (See Note 1)	−0.5 V to +5.5	Volts
Input Current (DC) (See Note 1)	−30 mA to +5	mA
Current into Output when output is low	+30	mA

Note 1: Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

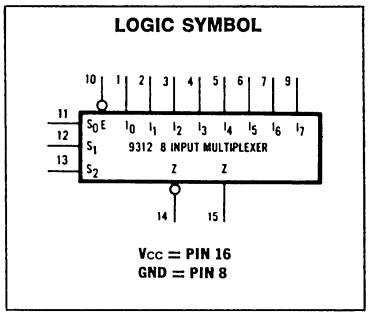


Fig. 1

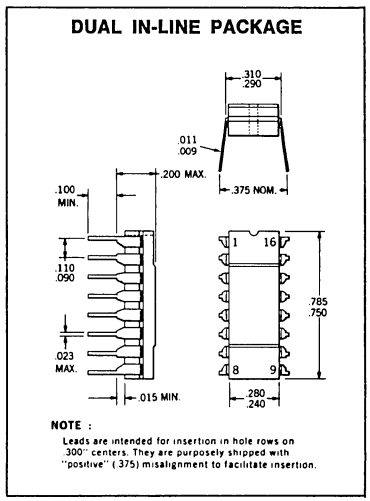


Fig. 2

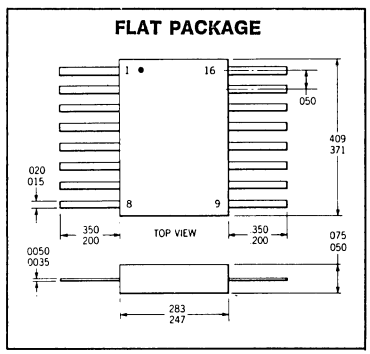


Fig. 3

LOADING RULES

INPUTS	LOADING
All Inputs	1 U.L.

1 U.L. = 1 TTμL Unit Load
1 U.L. is defined by the entries I_K and I_F in the table on page 3.

OUTPUTS	FAN-OUT	
	High State	Low State
$\bar{Z}$	18	9
Z	20	10

Fig. 4

FUNCTIONAL DESCRIPTION — The MIC9312 is a logical implementation of a single pole - 8 position switch with the switch position controlled by the state of three select inputs, S_0, S_1, S_2. Both assertion and negation outputs are provided. The enable input (E) is active low. When it is not activated the negation output is high and the assertion output is low regardless of all other inputs. The logic function provided at the output is:

$Z = E \cdot (I_0 \cdot \bar{S}_0 \cdot \bar{S}_1 \cdot \bar{S}_2 + I_1 \cdot S_0 \cdot \bar{S}_1 \cdot \bar{S}_2 + I_2 \cdot \bar{S}_0 \cdot S_1 \cdot \bar{S}_2 + I_3 \cdot S_0 \cdot S_1 \cdot \bar{S}_2 + I_4 \cdot \bar{S}_0 \cdot \bar{S}_1 \cdot S_2 + I_5 \cdot S_0 \cdot \bar{S}_1 \cdot S_2 + I_6 \cdot \bar{S}_0 \cdot S_1 \cdot S_2 + I_7 \cdot S_0 \cdot S_1 \cdot S_2)$.

The MIC9312 provides the ability, in one package, to select from eight sources of data or control information. By proper manipulation of the inputs, the MIC9312 can provide any logic function of four variables and its negation. Thus any number of random topic elements used to generate unusual truth tables can be replaced by one MIC9312.

TRUTH TABLE

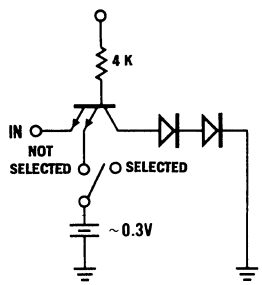
E	S_2	S_1	S_0	I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7	$\bar{Z}$	Z
H	X	X	X	X	X	X	X	X	X	X	X	H	L
L	L	L	L	L	X	X	X	X	X	X	X	H	L
L	L	L	L	H	X	X	X	X	X	X	X	L	H
L	L	L	H	X	L	X	X	X	X	X	X	H	L
L	L	L	H	X	H	X	X	X	X	X	X	L	H
L	L	H	L	X	X	L	X	X	X	X	X	H	L
L	L	H	L	X	X	H	X	X	X	X	X	L	H
L	L	H	H	X	X	X	L	X	X	X	X	H	L
L	L	H	H	X	X	X	H	X	X	X	X	L	H
L	H	L	L	X	X	X	X	L	X	X	X	H	L
L	H	L	L	X	X	X	X	H	X	X	X	L	H
L	H	L	H	X	X	X	X	X	L	X	X	H	L
L	H	L	H	X	X	X	X	X	H	X	X	L	H
L	H	H	L	X	X	X	X	X	X	L	X	H	L
L	H	H	L	X	X	X	X	X	X	H	X	L	H
L	H	H	H	X	X	X	X	X	X	X	L	H	L
L	H	H	H	X	X	X	X	X	X	X	H	L	H

H = High voltage level
L = Low voltage level
X = Level does not affect output

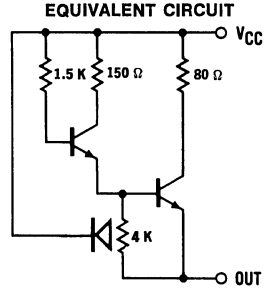
Fig. 5

TYPICAL INPUT AND OUTPUT CHARACTERISTICS

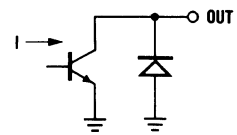
EQUIVALENT INPUT CIRCUIT



OUTPUT HIGH EQUIVALENT CIRCUIT



OUTPUT LOW EQUIVALENT CIRCUIT



INPUT CURRENT VERSUS INPUT VOLTAGE

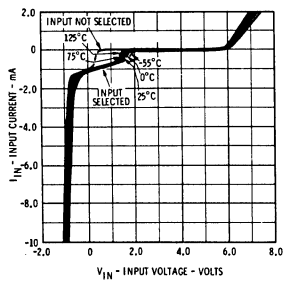


Fig. 6

OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (OUTPUT HIGH)

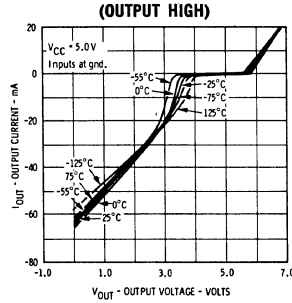


Fig. 7

OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (OUTPUT LOW)

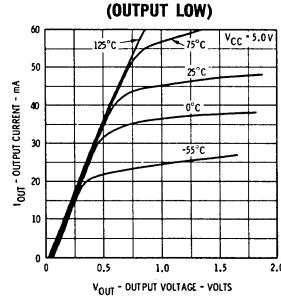


Fig. 8

ELECTRICAL CHARACTERISTICS* (MIC9312-1X) ($T_A = -55°C$ to $+125°C$, $V_{CC} = 5.0\ V \pm 10\%$)

SYMBOL	CHARACTERISTICS	LIMITS −55°C MIN.	LIMITS −55°C MAX.	LIMITS +25°C MIN.	LIMITS +25°C TYP.	LIMITS +25°C MAX.	LIMITS +125°C MIN.	LIMITS +125°C MAX.	UNITS	CONDITIONS
V_{OH}	Output High Voltage	2.4		2.4	2.7		2.4		Volts	$V_{CC} = 4.5\ V$ $I_{OH} = -1.2$ mA (Pin 15) $V_{CC} = 4.5\ V$ $I_{OH} = -1.08$ mA (Pin 14) Inputs at threshold voltages (V_{IL} or V_{IH}) as per truth table
V_{OL}	Output Low Voltage		0.4		0.21	0.4		.04	Volts	$V_{CC} = 5.5\ V$ $I_{OL} = 16.0$ mA (Pin 15) $I_{OL} = 14.4$ mA (Pin 14) $V_{CC} = 4.5\ V$ $I_{OL} = 12.4$ mA (Pin 15) $I_{OL} = 11.2$ mA (Pin 14) Inputs at threshold voltages (V_{IL} or V_{IH}) as per truth table
V_{IH}	Input High Voltage	2.0		1.7			1.4		Volts	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.8			0.9		0.8	Volts	Guaranteed input low threshold for all inputs
I_F (all inputs)	Input Load Current		−1.6 −1.24		−1.1 −0.85	−1.6 −1.24		−1.6 −1.24	mA mA	$V_{CC} = 5.5\ V$ $V_F = 0.4\ V$ $V_{CC} = 4.5\ V$ Input Selected
I_R (all inputs)	Input Leakage Current				15	60		60	μA	$V_{CC} = 5.5\ V$ $V_R = 4.5\ V$ Input not selected
I_{PDH}	V_{CC} Current		40		27	40		40	mA	$V_{CC} = 5.0\ V$
t_{pd+} (S_0 to Z)	Switching Speed				23	34			ns	$V_{CC} = 5.0\ V$, See Page 4
t_{pd-} (S_0 to Z)	Switching Speed				25	36			ns	$C_L = 15$ pF

*Pulse tested

ELECTRICAL CHARACTERISTICS* (MIC9312-5X) ($T_A = 0°C$ to $+75°C$, $V_{CC} = 5.0\ V \pm 5\%$)

SYMBOL	CHARACTERISTICS	LIMITS 0°C MIN.	LIMITS 0°C MAX.	LIMITS +25°C MIN.	LIMITS +25°C TYP.	LIMITS +25°C MAX.	LIMITS +75°C MIN.	LIMITS +75°C MAX.	UNITS	CONDITIONS
V_{OH}	Output High Voltage	2.4		2.4	3.0		2.4		Volts	$V_{CC} = 4.75\ V$ $I_{OH} = -1.2$ mA (Pin 15) $V_{CC} = 4.75\ V$ $I_{OH} = -1.08$ mA (Pin 14) Inputs at threshold voltages (V_{IL} or V_{IH}) as per truth table
V_{OL}	Output Low Voltage		0.45		0.21	0.45		0.45	Volts	$V_{CC} = 5.25\ V$ $I_{OL} = 16.0$ mA (Pin 15) $I_{OL} = 14.4$ mA (Pin 14) $V_{CC} = 4.75\ V$ $I_{OL} = 14.1$ mA (Pin 15) $I_{OL} = 12.7$ mA (Pin 14) Inputs at threshold voltages (V_{IL} or V_{IH}) as per truth table
V_{IH}	Input High Voltage	1.9		1.8			1.6		Volts	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.85			0.85		0.85	Volts	Guaranteed input low threshold for all inputs
I_F (all inputs)	Input Load Current		−1.6 −1.41		−1.0 −0.91	−1.6 −1.41		−1.6 −1.41	mA mA	$V_{CC} = 5.25\ V$ $V_F = 0.45\ V$ $V_{CC} = 4.75\ V$ Input Selected
I_R (all inputs)	Input Leakage Current				15	60		60	μA	$V_{CC} = 5.25\ V$ $V_R = 4.5\ V$ Input not selected
I_{PDH}	V_{CC} Current		43		27	43		43	mA	$V_{CC} = 5.0\ V$
t_{pd+} (S_0 to Z)	Switching Speed				23	34			ns	$V_{CC} = 5.0\ V$, See Page 4
t_{pd-} (S_0 to Z)	Switching Speed				25	36			ns	$C_L = 15$ pF

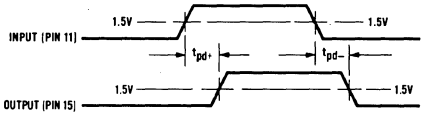
*Pulse tested

A.C. CHARACTERISTICS

A.C. CHARACTERISTICS

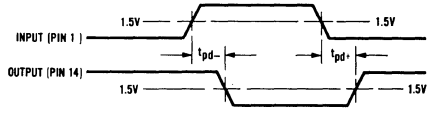
All measurements are made with V_{CC} = 5.0 V applied to pin 16 and with pin 8 grounded. The active input is driven by a MIC9002 TTL gate with the output loaded with 15 pF. Both outputs of the MIC9312 are loaded with 15 pF.

t_{pd}: S_0 to Z



Other Conditions: Pins 1, 8, 10, 12, 13 = Gnd
Pin 2 = Vcc through 1.0 kΩ
Pin 16 = Vcc

t_{pd}: I_0 to $\overline{Z}$



Other Conditions: Pins 8, 10, 11, 12, 13 = Gnd
Pin 16 = Vcc

TURN OFF DELAY VERSUS AMBIENT TEMPERATURE; S_0 to Z

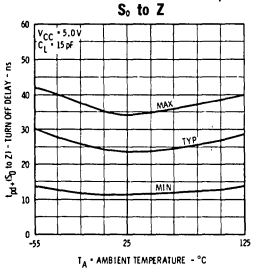


Fig. 9

TURN ON DELAY VERSUS AMBIENT TEMPERATURE; S_0 to Z

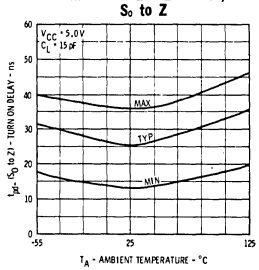


Fig. 10

TURN OFF DELAY VERSUS AMBIENT TEMPERATURE; I_0 to $\overline{Z}$

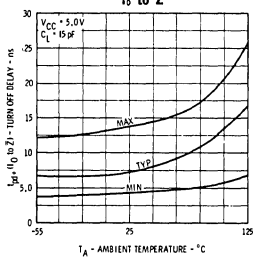


Fig. 11

TURN ON DELAY VERSUS AMBIENT TEMPERATURE; I_0 to $\overline{Z}$

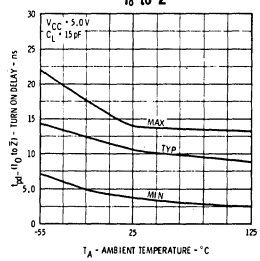
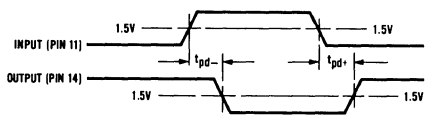


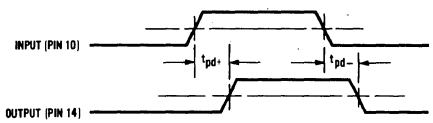
Fig. 12

t_{pd}: S_0 to $\overline{Z}$



Other Conditions: Pins 1, 8, 10, 12, 13 = Gnd
Pin 2 = Vcc through 1.0 kΩ
Pin 16 = Vcc

t_{pd}: E to $\overline{Z}$



Other Conditions: Pins 8, 11, 12, 13 = Gnd
Pin 1 = Vcc through 2.0 kΩ
Pin 16 = Vcc

TURN OFF DELAY VERSUS AMBIENT TEMPERATURE; S_0 to $\overline{Z}$

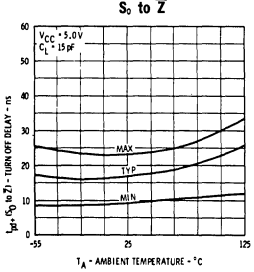


Fig. 13

TURN ON DELAY VERSUS AMBIENT TEMPERATURE; S_0 to $\overline{Z}$

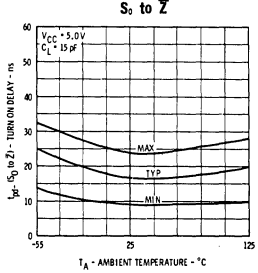


Fig. 14

TURN OFF DELAY VERSUS AMBIENT TEMPERATURE; E to $\overline{Z}$

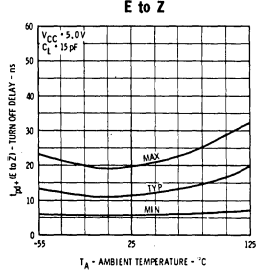


Fig. 15

TURN ON DELAY VERSUS AMBIENT TEMPERATURE; E to $\overline{Z}$

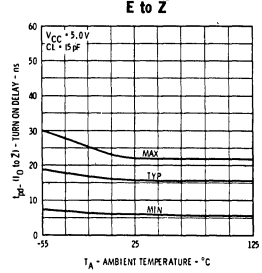


Fig. 16

APPLICATIONS

A MULTI-PORT MEMORY MODULE

The four bit by eight word multi-port memory module shown in the diagram below uses only thirteen MSI packages; four MIC9308 24 pin dual four bit latches, eight MIC9312 eight input multiplexers, and one MIC9301 one-out-of-ten decoder.

The module as shown is capable of simultaneously reading from two independently specified locations and writing into a third independently selected location. The necessary enables are provided so that a number of these modules may be connected together to produce a larger memory. As an example a sixteen bit by sixty-four word memory would require thirty-two of the modules shown below.

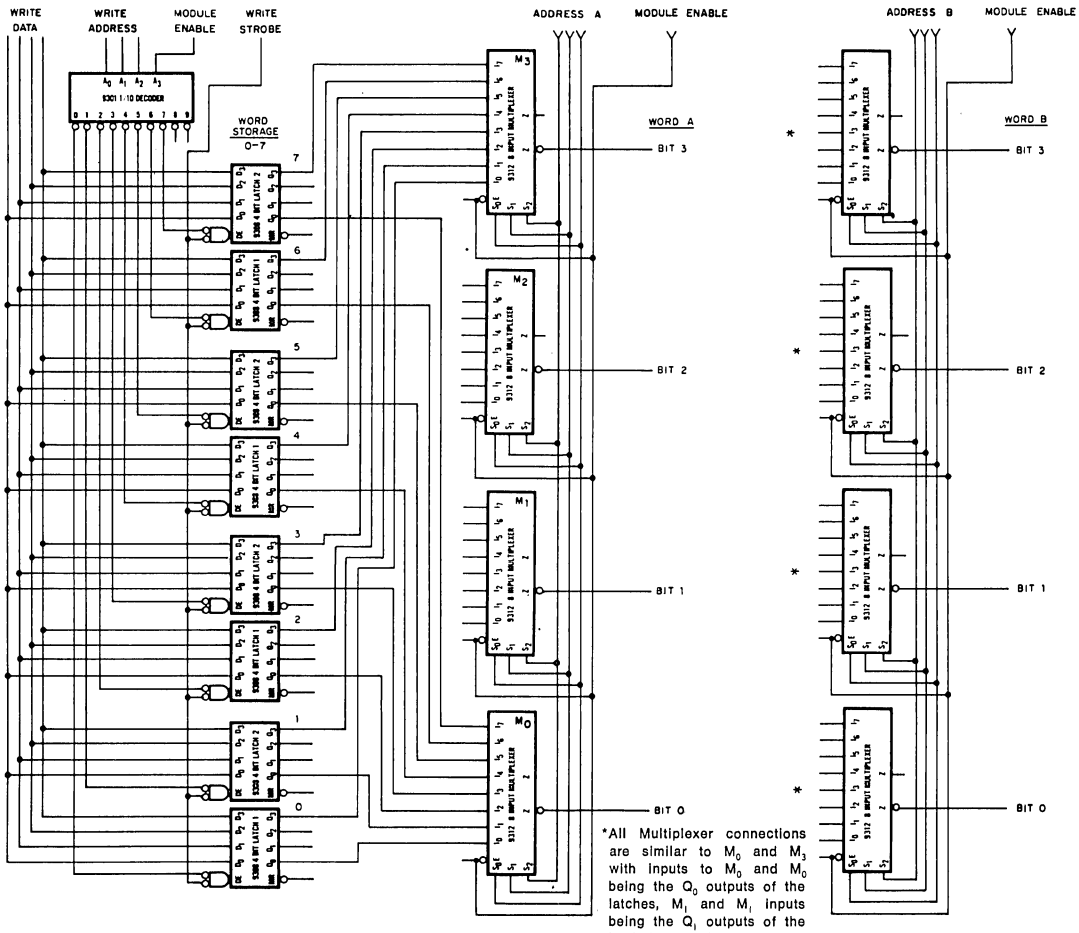
By connecting this type of memory to a function generator unit, a processor could be constructed that would execute three address instructions at a very high speed on the data contained in this type of memory. In order to utilize the speed of the memory the instructions would also have to be contained in fast semiconductor memory.

SPECIAL ORDERING CODE

Temperature Range:
−55°C to +125°C, add -1 to MIC number.
0°C to +75°C, add -5 to MIC number.

Case Style:
¼" x ⅜" Flat Pack, add "B" following last digit.
Ceramic Dual In-Line, 16 leads, add "D" following last digit.

Example:
MIC9312-1D is −55°C to +125°C. Temperature range in Ceramic Dual-In-Line, 16 lead package.
Flat-pack and Dual-In-Line packages have same pin configuration.



*All Multiplexer connections are similar to M_0 and M_3 with inputs to M_0 and M_0 being the Q_0 outputs of the latches, M_1 and M_1 inputs being the Q_1 outputs of the latch, M_2 and M_2 inputs being Q_0 outputs of the latch, etc.

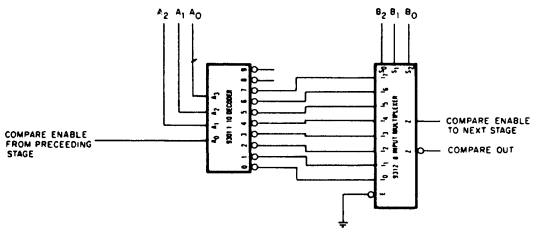
Fig. 17

APPLICATIONS

3 BIT COMPARATOR

Three bits of data to be compared are supplied to the address and select inputs of the MIC9301 and MIC9312 respectively. If A_0, A_1, A_2, and B_0, B_1, B_2 compare, the mutually exclusive active low output of the MIC9301 1/10 decoder and the selected input of the MIC9312 multiplexer will be coincidental and COMPARE OUT will be high. . The COMPARE ENABLE must be low to permit compare operation.

3 BIT COMPARATOR



INTERCONNECTION DIAGRAM FOR 9 BITS

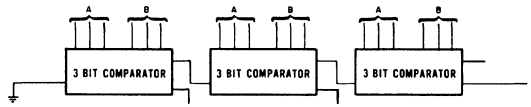


Fig. 18

IMPLEMENTING ANY FOUR-VARIABLE BOOLEAN FUNCTION

The MIC9312 eight input multiplexer can (in addition to performing its nominal function) produce any Boolean function of four variables without any additional elements if both the assertion and negation of one of the variables are present. If an assertion and negation are not present, one inverter may be required.

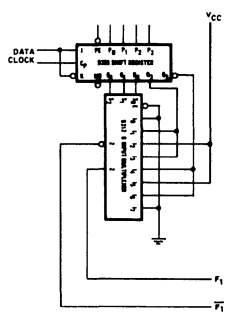
The procedure for implementing a four-variable function, along with an example, is shown in the attached diagram. First, consider the function in terms of a Karnaugh map. If the Q_0, Q_1 and Q_2 variable are connected to the S_0, S_1 and S_2 inputs of the MIC9312 then the Karnaugh map will be split, as shown, into eight sections, with each section corresponding to an input to the MIC9312. In order to implement the function each input of the MIC9312 is connected to one of the following four signals: ground, V_{CC}, the assertion, or negation of the fourth variable.

The contents of the two squares associated with an input, on the Karnaugh map, determine which connection is made to that input. If both squares contain a zero, ground should be connected to the input; if both squares contain a one, the input should be connected to V_{CC}. If the two squares contain a one and a zero then either the assertion or negation of the fourth variable will be required to implement the function. If the single one is located in the square associated with the assertion of the fourth variable then the assertion of the assertion of the fourth variable is connected to that input, and vice versa.

Shown in the illustration below is a MIC9312 decoding the condition of a MIC9300, producing a one output whenever the register contains two or more transitions. The truth table, Karnaugh map and the connection to the MIC9312 for this function are also shown in the illustration.

In many applications, using the MIC9312 to implement general logic functions of four variables will result in a sizeable reduction in package count. In many cases use of the MIC9312 with additional gates to produce functions of more than four variables will also reduce the package count.

The concept of using the MIC9312 eight input-multiplexer as a general logic function generator is described by S. S. Yau and C. K. Tang of Northwestern University in a paper presented at the 1968 Spring Joint Computer Conference in Atlantic City, New Jersey.



Q_0	Q_1	Q_2	Q_3	F_1
0	0	0	0	0
0	0	0	1	0
0	0	1	0	1
0	0	1	1	0
0	1	0	0	1
0	1	0	1	1
0	1	1	0	1
0	1	1	1	0
1	0	0	0	0
1	0	0	1	1
1	0	1	0	1
1	0	1	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	0	0
1	1	1	1	0

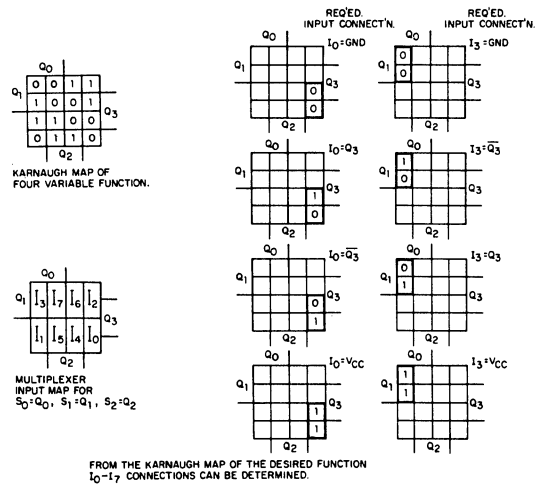


Fig. 19

MSI 4-BIT BINARY COUNTER

The MIC9316 is a high speed synchronous 4-bit binary decade counter. It is a synchronously presettable, multifunctional MSI building block useful in a large number of counting, digital integration, and conversion applications. Several stages of synchronous operation are obtainable with no external gating packages required through an internal carry look-ahead counting technique.

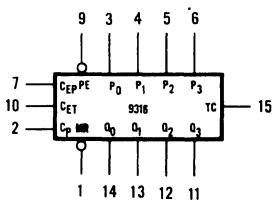
- **Synchronous Counting and Parallel Entry**
- **Decoded Terminal Count**
- **Built-In Carry Circuitry**
- **Typical Power Dissipation of 300 mW**
- **The Input/Output Characteristics Provide Easy Interfacing with DTL930, TTL9000, TTL7400 and MSI Families**
- **All Ceramic Hermetic 16 Pin Dual In-Line Package and Flat Package**
- **Input Diode Clamps Limit High Speed Line Termination Effects**

ABSOLUTE MAXIMUM RATINGS

(above which the useful life may be impaired)

CHARACTERISTICS		UNITS
Storage Temperature	−65°C to +150	°C
Temperature (Ambient) Under Bias	−55°C to +125	°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7	Volts
Voltage Applied to Outputs for high output state	−0.5 V to V_{CC}	value
Input Voltage (D.C.)	−0.5 V to +5.5	Volts

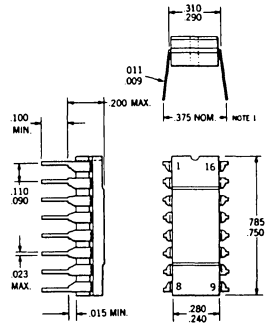
LOGIC DIAGRAM



V_{CC} = Pin 16
Gnd = Pin 8

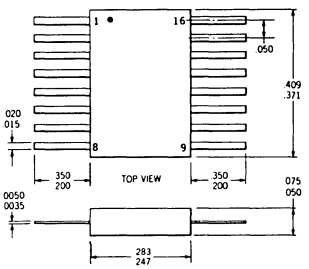
PHYSICAL DIMENSIONS

DUAL IN-LINE PACKAGE



NOTE:
1. Leads are intended for insertion in hole rows on .300" centers. They are purposely shipped with "positive" (.375) misalignment to facilitate insertion.

FLAT PACKAGE



FUNCTIONAL DESCRIPTION — A clock buffer and inverter drives the four clocked RS master-slave flip flops in parallel, so that synchronous operation is obtained. When the clock input (CP) is low, the slave is steady, but data can enter the master via the R and the S inputs. During the low to high transition of CP, first the data inputs (R and S) are inhibited, so that a later change in the input data will not affect the master; secondly, the now trapped information in the master is transferred to the slave and is reflected at the outputs. When the transfer is completed both the master and the slave are steady as long as the clock input remains high, and regardless of the logic state at any other input to the device. During the high to low transition of the clock input, first the transfer path from master to slave are inhibited, leaving the slave steady in its present state, secondly, the data inputs (R and S) are enabled so that new data can enter the master. As a result of this synchronous operation higher clock frequency is possible and much less external logic is required in most applications. Some restrictions are placed on the manner of selection. First, the transition of CEP or CET from high to low or of $\overline{PE}$ from low to high may only be done when CP is high. The remaining transitions may be made by following the setup and release times specified under "Switching Characteristics." The asynchronous $\overline{MR}$ clears the counter independent of any other input.

Note: CE (count enable) = CEP · CET
TC = CET · Q_0 · Q_1 · Q_2 · Q_3

SPECIAL ORDERING CODE

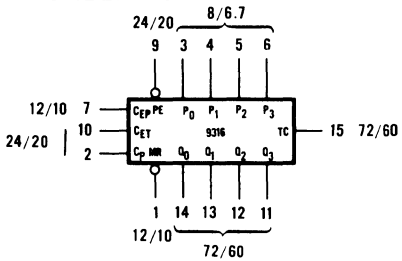
Temperature Range:
−55°C to +125°C, add -1 to MIC number.
0°C to +75°C, add -5 to MIC number.

Case Style:
¼" x ⅜" Flat Pack, add "B" following last digit.
Ceramic Dual In-Line, 16 leads, add "D" following last digit.

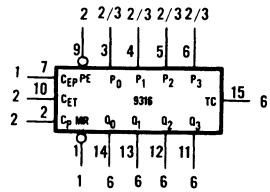
Example:
MIC9316-1D is −55°C to +125°C. Temperature range in Ceramic Dual-In-Line, 16 lead package. Flat-pack and Dual-In-Line packages have same pin configuration.

LOADING RULES

CCSL LOAD AND DRIVE FACTORS



TTL LOAD AND DRIVE FACTORS



ELECTRICAL CHARACTERISTICS (MIC9316-1X) (T_A = −55°C to +125°C, V_{CC} = 5.0 V ±10%)

SYMBOL	CHARACTERISTICS	LIMITS −55°C MIN.	LIMITS −55°C MAX.	LIMITS +25°C MIN.	LIMITS +25°C TYP.	LIMITS +25°C MAX.	LIMITS +125°C MIN.	LIMITS +125°C MAX.	UNITS	CONDITIONS & COMMENTS
V_{OH}	Output High Voltage	2.4		2.4	2.7		2.4		Volts	V_{CC} = 4.5 V, I_{OH} = −0.36 mA
V_{OL}	Output Low Voltage		0.4		0.2	0.4		0.4	Volts	V_{CC} = 5.5 V, I_{OL} = 9.6 mA V_{CC} = 4.5 V, I_{OL} = 7.44 mA
V_{IH}	Input High Voltage	2.0		1.7			1.4		Volts	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.8			0.9		0.8	Volts	Guaranteed input low threshold for all inputs
I_F	Input Load Current $\overline{MR}$, CEP		−1.6		−1.0	−1.6		−1.6	mA	
2 I_F	Input Load Current CP, $\overline{PE}$, CET		−3.2		−2.0	−3.2		−3.2	mA	V_{CC} = 5.5 V V_F = 0.4 V
⅔ I_F	Input Load Current P_0, P_1, P_2, P_3		−1.07		−0.7	−1.07		−1.07	mA	
I_R	Input Leakage Current $\overline{MR}$, CEP		60		10	60		60	μA	
2 I_R	Input Leakage Current CP, $\overline{PE}$, CET		120		20	120		120	μA	V_{CC} = 5.5 V V_R = 4.5 V
⅔ I_R	Input Leakage Current P_0, P_1, P_2, P_3		40		7.0	40		40	μA	

ELECTRICAL CHARACTERISTICS (MIC9316-5X) ($T_A = 0°C$ to $+75°C$, $V_{CC} = 5.0\ V \pm 5\%$)

SYMBOL	CHARACTERISTICS	LIMITS						UNITS	CONDITIONS & COMMENTS
		0°C		+25°C			+75°C		
		MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.	
V_{OH}	Output High Voltage	2.4		2.4	3.0		2.4		Volts	$V_{CC} = 4.75\ V$, $I_{OH} = -0.36\ mA$
V_{OL}	Output Low Voltage		0.45		0.2	0.45		0.45	Volts	$V_{CC} = 5.25\ V$, $I_{OL} = 9.6\ mA$ $V_{CC} = 4.75\ V$, $I_{OL} = 8.5\ mA$
V_{IH}	Input High Voltage	1.9		1.8			1.6		Volts	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.85			0.85		0.85	Volts	Guaranteed input low threshold for all inputs
I_F	Input Load Current $\overline{MR}$, CEP		−1.6		−1.0	−1.6		−1.6	mA	
$2\ I_F$	Input Load Current CP, $\overline{PE}$, CET		−3.2		−2.0	−3.2		−3.2	mA	$V_{CC} = 5.25\ V$ $V_F = 0.4\ V$
$⅔\ I_F$	Input Load Current P_0, P_1, P_2, P_3		−1.07		−0.7	−1.07		−1.07	mA	
I_R	Input Leakage Current $\overline{MR}$, CEP		60		10	60		60	μA	
$2\ I_R$	Input Leakage Current CP, $\overline{PE}$, CET		120		20	120		120	μA	$V_{CC} = 5.25\ V$ $V_R = 4.5\ V$
$⅔\ I_R$	Input Leakage Current P_0, P_1, P_2, P_3		40		7.0	40		40	μA	

SWITCHING CHARACTERISTICS ($T_A = 25°C$)

SYMBOL	CHARACTERISTICS	MIN.	TYP.	MAX.	UNITS	CONDITIONS & COMMENTS
t_{pd+} (Q)	Turn-Off Delay		20		ns	$V_{CC} = 5.0\ V$ $C_L = 15\ pF$ (Fig. 1)
t_{pd-} (Q)	Turn-On Delay		15		ns	
t_{pd+} (TC)	Turn-Off Delay for TC		35		ns	
t_{pd-} (TC)	Turn-On Delay for TC		20		ns	
t_s(CE)	Set-Up Time for CE		14		ns	$V_{CC} = 5.0\ V$
t_r (CE)	Release Time for CE		12		ns	$C_L = 15\ pF$ (Fig. 2)
t_s	Set-Up Time for Data		18		ns	$V_{CC} = 5.0\ V$ $C_L = 15\ pF$ (Fig. 3)
t_r	Release Time for Data		17		ns	
t_s ($\overline{PE}$)	Set-Up Time for $\overline{PE}$		30		ns	
t_r ($\overline{PE}$)	Release Time for $\overline{PE}$		28		ns	
t_{pd-} ($\overline{MR}$)	Turn-On Delay for $\overline{MR}$		33		ns	$V_{CC} = 5.0\ V$, $C_L = 15\ pF$ (Fig. 4)
t_{P+}	Propagation Delay for CET to TC		14		ns	$V_{CC} = 5.0\ V$, $C_L = 15\ pF$ (Fig. 5)

SET-UP TIME: t_s is defined as the minimum time required for the logic level to be present at the logic input prior to the clock transition from low to high in order for the flip-flop(s) to respond.

RELEASE TIME: t_r is defined as the maximum time allowed for the logic level to be present at the logic input prior to the clock transition from low to high in order for the flip-flop(s) not to respond.

SWITCHING TIME WAVEFORMS

Fig. 1

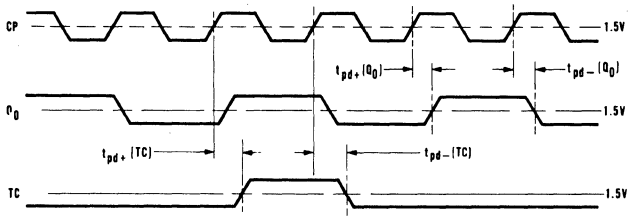


Fig. 2

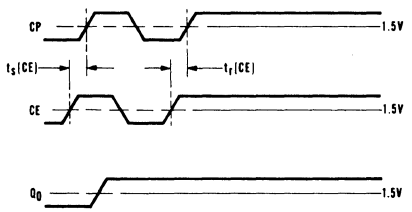


Fig. 3

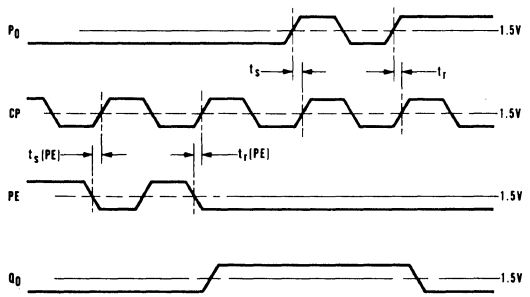


Fig. 4

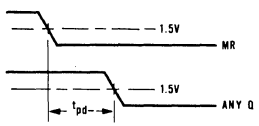
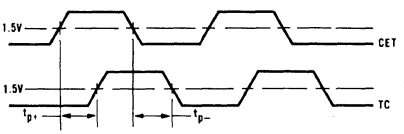
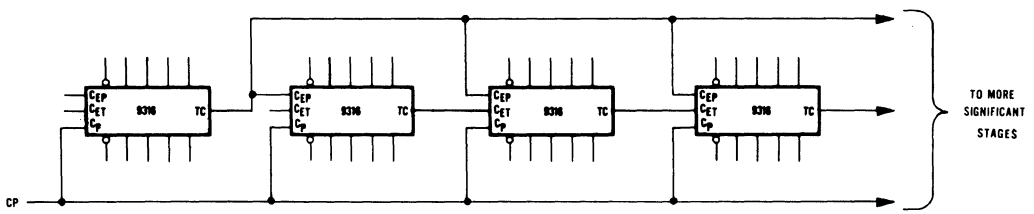


Fig. 5



APPLICATIONS



SYNCHRONOUS COUNTING SCHEME

MSI QUAD TWO-INPUT MULTIPLEXER

- **Multifunction Capability**
- **20 ns Through Delay**
- **On-Chip Select Logic Decoding**
- **Fully Buffered Outputs**
- **The Input/Output Characteristics Provide Easy Interfacing with ITT DTL 930, ITT TTL9000, MSI and other DTL and TTL Families.**
- **Input Clamp Diodes Limit High Speed Termination Effects.**

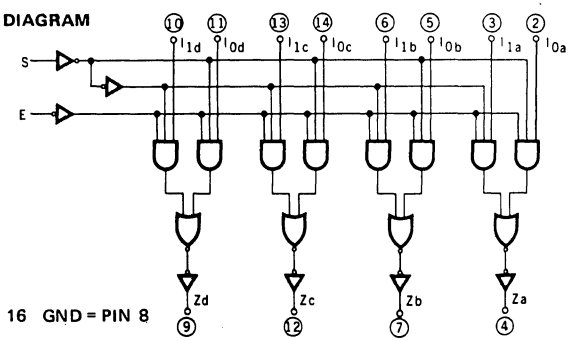
The ITT9322 is a monolithic, high speed, quad two-input digital multiplexer circuit, constructed with the ITT epitaxial process. It consists of four multiplexing circuits with common select and enable logic, each circuit contains two inputs and one output. The circuit uses TTL for high speed, high fanout operation and is compatible with all other members of the DTL and TTL family of digital integrated circuits.

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

CHARACTERISTICS		UNITS
Storage Temperature	−65°C to +150	°C
Temperature (Ambient) Under Bias	−55°C to +125	°C
V_{CC} Pin Potential to Ground Pin	0.5 V to +7.0	V
Voltage Applied to Output when output is high	0 V to +V_{CC}	value
Input Voltage (DC) (See Note 1)	−0.5 V to +5.5	V
Input Current (DC) (See Note 1)	−30 mA to +5	mA
Current into Output when output is low	+30	mA

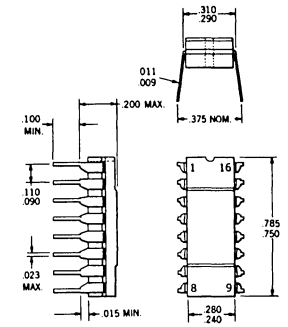
Note 1 – either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

LOGIC DIAGRAM



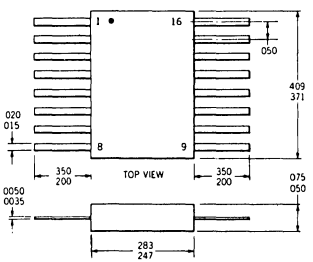
V_{CC} = PIN 16 GND = PIN 8

DUAL IN-LINE PACKAGE



NOTE :
Leads are intended for insertion in hole rows on .300" centers. They are purposely shipped with "positive" (.375) misalignment to facilitate insertion.

FLAT PACKAGE



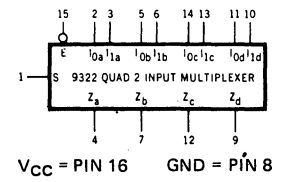
SPECIAL ORDERING CODE

Temperature Range:
1 = −55° + 125°C
5 = 0° to +75C

Package:
B = Flat Pack
D = Dual In-Line, 16 leads

Example:
MIC9322 - 1B means operating temperature range of −55° to +125°C, supplied in a Flat Pack

LOGIC SYMBOL



V_{CC} = PIN 16 GND = PIN 8

ELECTRICAL CHARACTERISTICS* (T_A = –55°C to +125°C, V_{CC} = 5.0 V ± 10%)

SYMBOL	CHARACTERISTICS	LIMITS –55°C MIN.	LIMITS –55°C MAX.	LIMITS +25°C MIN.	LIMITS +25°C TYP.	LIMITS +25°C MAX.	LIMITS +125°C MIN.	LIMITS +125°C MAX.	UNITS	CONDITIONS
V_{OH}	Output High Voltage	2.4		2.4	2.7		2.4		Volts	V_{CC} = 4.5 V I_{OH} = –1.2 mA Inputs at threshold voltages (V_{IL} or V_{IH}) as per truth table
V_{OL}	Output Low Voltage		0.4		0.21	0.4		0.4	Volts	V_{CC} = 5.5 V I_{OL} = 16.0 mA V_{CC} = 4.5 V I_{OL} = 12.4 mA Inputs at threshold voltages (V_{IL} or V_{IH}) as per truth table
V_{IH}	Input High Voltage	2.0		1.7			1.4		Volts	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.8			0.9		0.8	Volts	Guaranteed input low threshold for all inputs
I_F (all inputs)	Input Load Current		–1.6		–1.1	–1.6		–1.6	mA	V_{CC} = 5.5 V V_F = 0.4 V
			–1.24		–0.85	–1.24		–1.24	mA	V_{CC} = 4.5 V Input selected
I_R (all inputs)	Input Leakage Current				8.0	60		60	µA	V_{CC} = 5.5 V V_R = 4.5 V
I_{PDH}	V_{CC} Current		43		30	43		43	mA	V_{CC} = 5.0 V All inputs high
t_{pd+} (S to Z_a)	Switching Speed				17	25			ns	V_{CC} = 5.0 V, C_L = 15 pF, See Figure (A)
t_{pd-} (S to Z_a)	Switching Speed				20	27			ns	

*Pulse Tested

ELECTRICAL CHARACTERISTICS* (T_A = 0°C to +75°C, V_{CC} = 5.0 V ± 5%)

SYMBOL	CHARACTERISTICS	LIMITS 0°C MIN.	LIMITS 0°C MAX.	LIMITS +25°C MIN.	LIMITS +25°C TYP.	LIMITS +25°C MAX.	LIMITS +125°C MIN.	LIMITS +125°C MAX.	UNITS	CONDITIONS
V_{OH}	Output High Voltage	2.4		2.4	3.0		2.4		Volts	V_{CC} = 4.75 V I_{OH} = –1.2 mA Inputs at threshold voltages (V_{IL} or V_{IH}) as per truth table
V_{OL}	Output Low Voltage		0.45		0.21	0.45		0.45	Volts	V_{CC} = 5.25 V I_{OL} = 16.0 mA V_{CC} = 4.75 V I_{OL} = 14.1 mA Inputs at threshold voltages (V_{IL} or V_{IH}) as per truth table
V_{IH}	Input High Voltage	1.9		1.8			1.6		Volts	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.85			0.85		0.85	Volts	Guaranteed input low threshold for all inputs
I_F (all inputs)	Input Load Current		–1.6		–1.0	–1.6		–1.6	mA	V_{CC} = 5.25 V V_F = 0.45 V
			–1.41		–0.91	–1.41		–1.41	mA	V_{CC} = 4.75 V Input selected
I_R (all inputs)	Input Leakage Current				8.0	60		60	µA	V_{CC} = 5.25 V V_R = 4.5 V
I_{PDH}	V_{CC} Current		45		30	45		45	mA	V_{CC} = 5.0 V All inputs high
t_{pd+} (S to Z_a)	Switching Speed				17	30			ns	V_{CC} = 5.0 V, C_L = 15 pF, See Figure (A)
t_{pd-} (S to Z_a)	Switching Speed				20	31			ns	

*Pulse Tested

FUNCTIONAL DESCRIPTION – The MIC9322 quad two input multiplexer is a member of the ITT family of compatible Medium Scale Integrated (MSI) digital building blocks. It provides this family with the ability to select four bits of either data or control from two sources, in one package. The enable input ($\overline{E}$) is active low. When not activated all outputs (Z) are low regardless of all other inputs.

The MIC9322 quad two input multiplexer is the logical implementation of a four-pole two-position switch, with the position of the switch being set by the logic levels supplied to the one select input. The logic equations for the outputs are shown below:

$Z_a = E \cdot (I_{1a} \cdot S + I_{0a} \cdot \overline{S})$ $\quad Z_b = E \cdot (I_{1b} \cdot S + I_{0b} \cdot \overline{S})$

$Z_c = E \cdot (I_{1c} \cdot S + I_{0c} \cdot \overline{S})$ $\quad Z_d = E \cdot (I_{1d} \cdot S + I_{0d} \cdot \overline{S})$

A common use of the MIC9322 would be the moving of data from a group of registers to four common output busses. The particular register from which the data came would be determined by the state of the select input. A less obvious use is a function generator. The MIC9322 can generate four functions of two variables with one variable common. This is useful for implementing gating functions.

TRUTH TABLE
Identical for Each Multiplexer

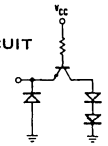
ENABLE	SELECT INPUT	INPUTS		OUTPUT
$\overline{E}$	S	I_{OX}	I_{IX}	Z_X
H	X	X	X	L
L	H	X	L	L
L	H	X	H	H
L	L	L	X	L
L	L	H	X	H

L = low voltage level
H = high voltage level
X = either high or low logic level.

LOADING RULES
(1 U.L. = 1 TTL gate input load)

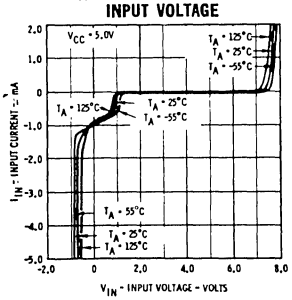
INPUTS	LOADING	
$I_{0a}, I_{1a}, I_{0b}, I_{1b}, I_{0c}, I_{1c}, I_{0d}, I_{1d}$ S, E	1 U.L.	
OUTPUTS	FANOUT AT LOGIC LEVEL HIGH	LOW
Z_a, Z_b, Z_c, Z_d	20 U.L.	10 U.L.

INPUT EQUIVALENT CIRCUIT

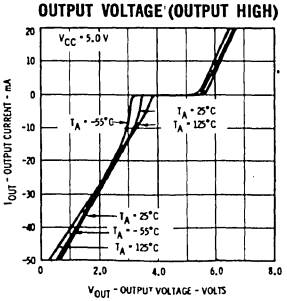


TYPICAL INPUT AND OUTPUT CHARACTERISTICS

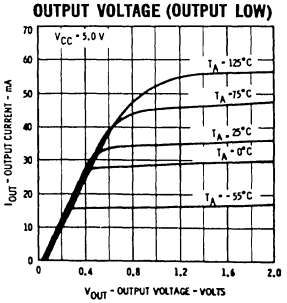
INPUT CURRENT VERSUS INPUT VOLTAGE



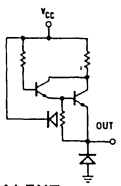
OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (OUTPUT HIGH)



OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (OUTPUT LOW)



OUTPUT EQUIVALENT CIRCUIT (Output High)



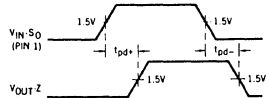
OUTPUT EQUIVALENT CIRCUIT (Output Low)

A. C. CHARACTERISTICS

SWITCHING WAVEFORMS – All inputs are outputs of TTL 9000 series gates loaded with 15 pF. All outputs are loaded with the same capacitance (referred to as C_L) and only with capacitance.

t_{pd}; S to Z_a

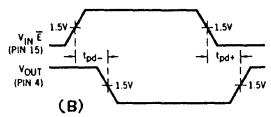
CONDITIONS — Pins 2, 15 = GND
Pin 3 = V_{CC}



(A)

t_{pd}; $\overline{E}$ to Z_a

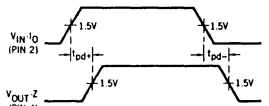
CONDITIONS — All Other Inputs High



(B)

t_{pd}; I_{0a} to Z_a

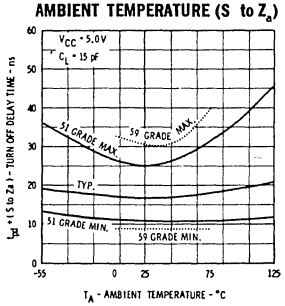
CONDITIONS—Pins 1, 15 = GND.



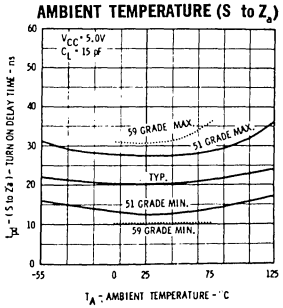
(C)

SWITCHING CHARACTERISTICS

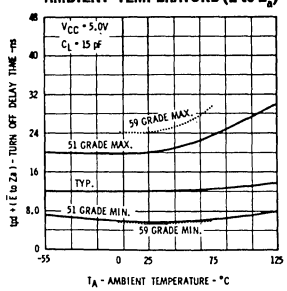
TURN OFF DELAY TIME VERSUS AMBIENT TEMPERATURE (S to Z_a)



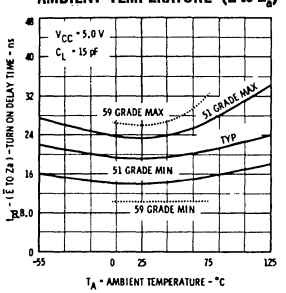
TURN ON DELAY TIME VERSUS AMBIENT TEMPERATURE (S to Z_a)



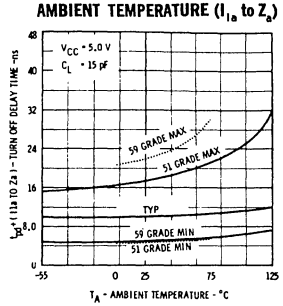
TURN OFF DELAY TIME VERSUS AMBIENT TEMPERATURE ($\overline{E}$ to Z_a)



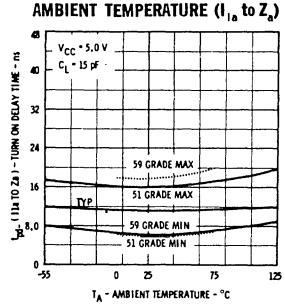
TURN ON DELAY TIME VERSUS AMBIENT TEMPERATURE ($\overline{E}$ to Z_a)



TURN OFF DELAY TIME VERSUS AMBIENT TEMPERATURE (I_{1a} to Z_a)

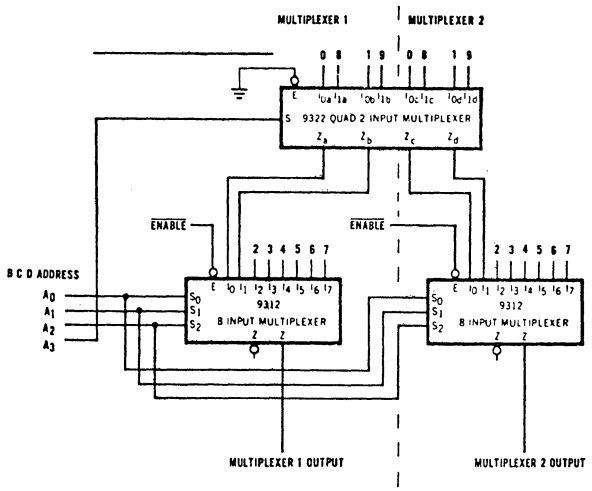


TURN ON DELAY TIME VERSUS AMBIENT TEMPERATURE (I_{1a} to Z_a)

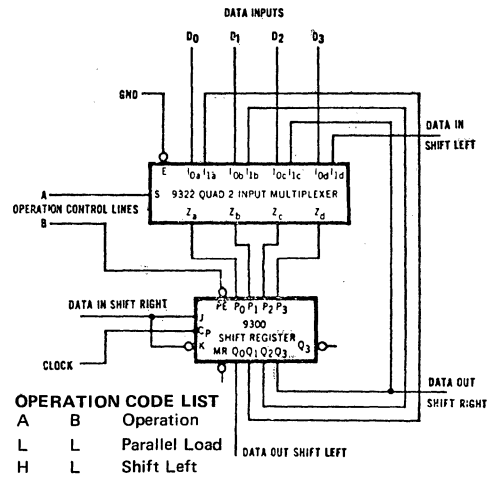


APPLICATIONS

DUAL 10 INPUT MULTIPLEXER



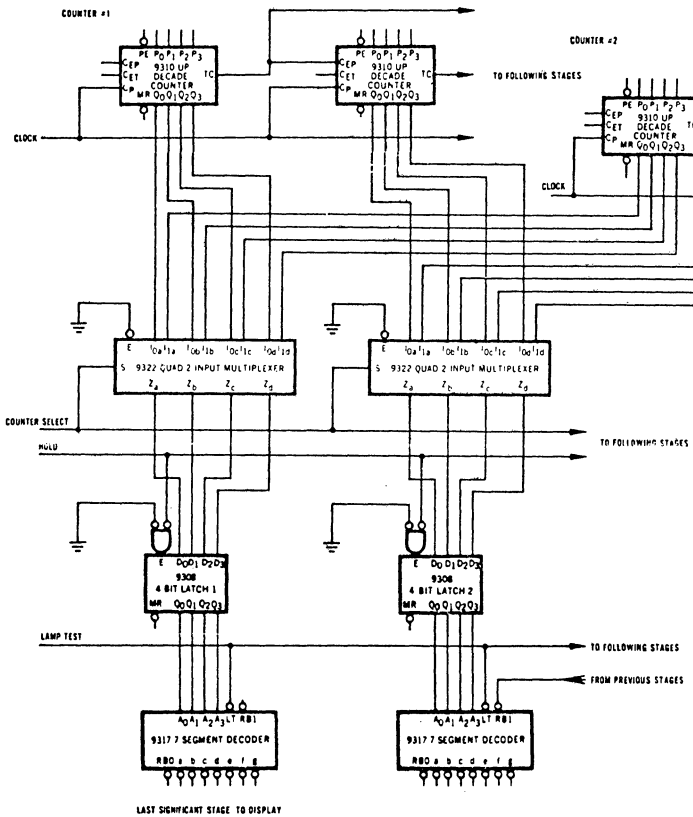
SHIFT LEFT, SHIFT RIGHT, PARALLEL LOAD REGISTER



OPERATION CODE LIST

A	B	Operation
L	L	Parallel Load
H	L	Shift Left
L	H	Shift Right
H	H	Shift Right

This register will shift left, shift right, and load 4 bits of parallel data according to the operation code applied to A and B.



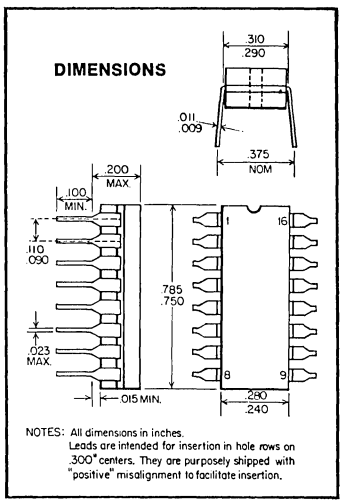
APPLICATIONS

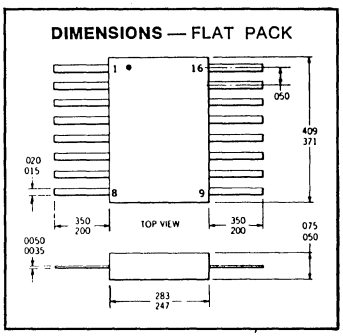
REGISTER SELECTION

The 9322 can be used to select parallel data from two multiple bit sources. Illustrated above is a counting and display system where the 9322 selects the content of one of the counters for display.

MSI DUAL 8-BIT SHIFT REGISTER

- 20 MHz Shift Frequency
- Two Input Multiplexer Provided at Data Input of Each Register
- Gated Clock Input Circuitry
- Both True and Complementary Outputs Provided from Last Bit of Each Register
- Asynchronous Master Reset Common to Both Registers
- Typical Power Dissipation of 300 mW
- Compatible with TTL and DTL families
- Input Diode Clamping

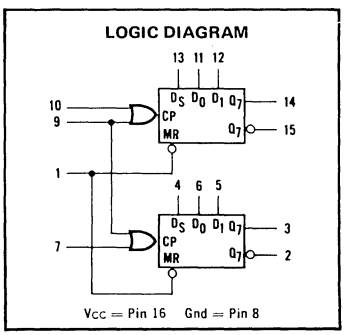




The ITT9328 is a high speed serial storage element providing sixteen bits of storage in the form of two eight bit registers that will shift at greater than 20 MHz rates. The multi-functional capability of this device is provided by several features: 1) Additional gating is provided at the input to both shift registers so that the input is easily multiplexed between two sources. 2) The clock of each register may be provided separately or together. 3) Both the true and complementary outputs are provided from each eight bit register, and both registers may be master cleared from a common input.

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

CHARACTERISTICS	UNITS
Storage Temperature . . . . . −65°C to +150	°C
Temperature (Ambient) Under Bias . . . . . −55°C to + 125	°C
Vcc Pin Potential to Ground Pin . . . . . −0.5V to + 7	V
Voltage Applied to Outputs for high output state . −0.5V to + Vcc	value
Input Voltage (D.C.) . . . . . −0.5V to + 5.5	V



SPECIAL ORDERING CODE

Temperature Range:
1 = −55° + 125°C
5 = 0° to +75C

Package:
B = Flat Pack
D = Dual In-Line, 16 leads

Example:
ITT9328 - 1B means operating temperature range of −55° to +125°C, supplied in a Flat Pack

FUNCTIONAL DESCRIPTION — The two 8 bit shift registers have a common clock input (pin 9) and separate clock inputs (pins 10 & 7). The clocking of each register is controlled by the OR function of the separate and the common clock input. Each register is composed of eight clocked RS master-slave flip-flops and a number of gates. The clock OR gate drives the eight clock inputs of the flip-flop in parallel. When the two clock inputs (the separate and the common) to the OR gate are low, the slave latches are steady, but data can enter the master latches via the R and S input. During the first low to high transition of either, or both simultaneously, of the two clock inputs, the data inputs (R and S) are inhibited so that a later change in input data will not affect the master; then the now trapped information in the master is transferred to the slave. When the transfer is complete, both the master and the slave are steady as long as either or both clock inputs remain high. During the high to low transition of the last remaining high clock input, the transfer path from master to slave is inhibited first, leaving the slave steady in its present state; second the data inputs (R and S) are enabled so that new data can enter the master. Either of the clock inputs can be used as clock inhibit inputs by applying a logic high signal. Each 8 bit shift register has a two input multiplexer in front of the serial data input. The two data inputs Do and D1 are controlled by the data select input Ds following the Boolean expression:

Serial data in: $S_D = D_S D_O + D_S D_I$

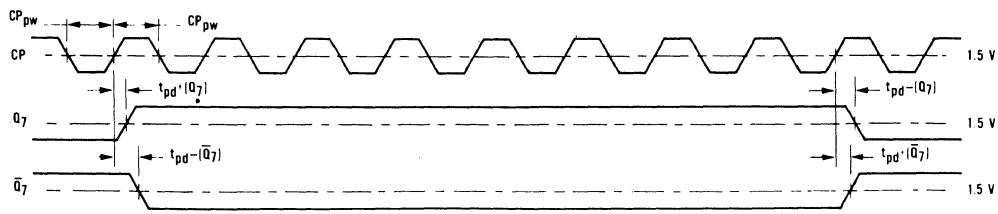
An asynchronous master reset is provided which, when activated by a low logic level, will clear all sixteen stages independently of any other input signal.

	INPUT	FAN IN
	$\overline{MR}$, D_O·D_I	1 Unit Load
LOADING RULES	Separate CP (pins & & 10)	1.5 Unit Loads
(1 U.L. = TTL	D_S	2 Unit Loads
input gate load)	Common CP (pin 9)	3 Unit Loads
	OUTPUT	FAN OUT
	Q_7, $\overline{Q}_7$	6 Unit Loads

ELECTRICAL CHARACTERISTICS (T_A = −55°C to + 125°C, V_{CC} = 5.0V ± 10%)

		LIMITS							
		−55°C		+ 25°C			+ 125°C		
SYMBOL	CHARACTERISTICS	MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.	UNITS	TEST CONDITIONS
V_{OH}	Output High Voltage	2.4		2.4	2.7		2.4		Volts	V_{CC}=4.5V,I_{OH}=−0.36mA
V_{OL}	Output Low Voltage		0.4		0.2	0.4		0.4	Volts	V_{CC}=5.5V,I_{OL}=9.6mA V_{CC}=4.5V,I_{OL}=7.44mA
V_H	Input High Voltage	2.0		1.7			1.4		Volts	Guaranteed input high threshold for all inputs
V_L	Input Low Voltage		0.8			0.9		0.8	Volts	Guaranteed input low threshold for all inputs
I_F	Input Load Current (MR, D_O·D_I)		−1.6		−1.0	−1.6		−1.6	mA	
1.5I_F	Input Load Current (separate CP pins 7 & 10		−2.4		−1.5	−2.4		−2.4	mA	V_{CC}=5.5V
2 I_F	Input Load Current (D_S)		−3.2		−2.0	−3.2		−3.2	mA	V_F=0.4V
3 I_F	Input Load Current (common CP pin 9)		−4.8		−3.0	−4.8		−4.8	mA	
I_p	Input Leakage Current (MR, D_O·D_1)		60		10	60		60	μA	
1.5I_p	Input Leakage Current (separate CP pins 7 & 10)		90		15	90		90	μA	V_{CC}=5.5V
2 I_p	Input Leakage Current (D_S)		120		20	120		120	μA	V_R=4.5V
3 I_p	Input Leakage Current (common CP pin 9)		1801		30	180		180	μA	
I_{PD}	Power Dissipation		365		300	365		365	mW	V_{CC}=5.0V

SWITCHING WAVEFORMS



Note: Q_7 is connected to D_1. Other clock is grounded.

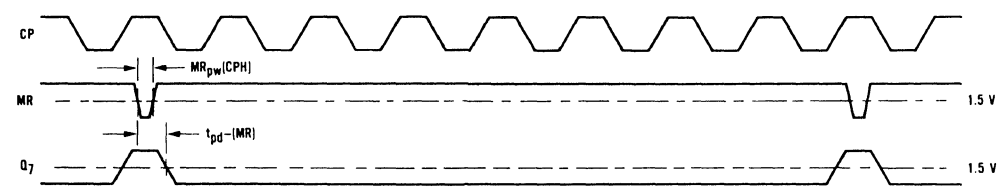
Fig. 1

ELECTRICAL CHARACTERISTICS (T_A = 0°C to + 75°C, V_{cc} = 5.0V ± 5%)

SYMBOL	CHARACTERISTICS	LIMITS 0°C MIN.	MAX.	+ 25°C MIN.	TYP.	MAX.	+ 75°C MIN.	MAX.	UNITS	TEST CONDITIONS
V_{OH}	Output High Voltage	2.4		2.4	3.0		2.4		Volts	V_{CC}=4.75V, I_{OH}=−0.36mA
V_{OL}	Output Low Voltage		0.45		0.2	0.45		0.45	Volts	V_{CC}=5.25V, I_{OL}=9.6mA V_{CC}=4.75V, I_{OL}=8.5mA
V_{IH}	Input High Voltage	1.9		1.8			1.6		Volts	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.85			0.85		0.85	Volts	Guaranteed input low threshold for all inputs
I_F	Input Load Current (MR,D_o,D_1)		−1.6		−1.0	−1.6		−1.6	mA	
1.5I_F	Input Load Current (separate CP pins 7 & 10)		−2.4		−1.5	−2.4		−2.4	mA	V_{CC}=5.25V
2 I_F	Input Load Current (D_S)		−3.2		−2.0	−3.2		−3.2	mA	V_F=0.4V
3 I_F	Input Load Current (common CP pin 9)		−4.8		−3.0	−4.8		−4.8	mA	
I_R	Input Leakage Current (MR,D_o,D_1)		60		10	60		60	μA	
1.5 I_R	Input Leakage Current (separate CP pins 7 & 10)		90		15	90		90	μA	V_{CC}=5.25V
2 I_R	Input Leakage Current (D_S)		120		20	120		120	μA	V_R=4.5V
3 I_R	Input Leakage Current (common CP pin 9)		180		30	180		180	μA	
I_{PD}	Power Dissipation		365		300	365		365	mW	V_{CC}=5.0V

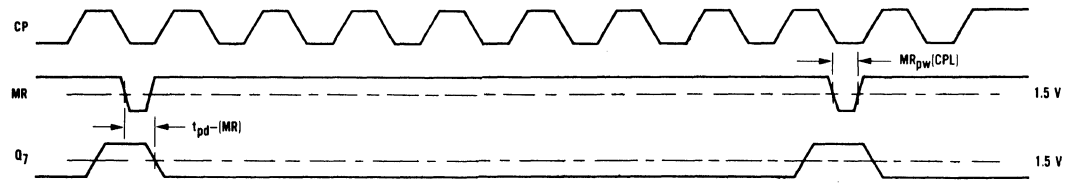
SWITCHING CHARACTERISTICS (T_A= 25°C)

SYMBOL	CHARACTERISTICS	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
t_{pd}−(Q_7& Q_7	Turn-Off Delay (clock to output)		13		ns	V_{cc}=5.0V, C_L=15 pF Fig.1
t_{pd}−(Q_7&$\bar{Q}_7$)	Turn-On Delay (clock to output)		22		ns	
t_{pd}−(MR)	Turn-On Delay (Master reset to output)		35		ns	V_{cc}=5.0V, C_L=15pF Fig. 2 & 3
CP_{pw}	Min. Clock Pulse Width		14		ns	V_{cc}=5.0V, C_l=15 pF Fig. 1
MR_{pw}(CPH)	Min. Master Reset pulse width with clock high		15		ns	V_{cc}5.0V, C_L=15 pF Fig. 2
MR_{pw}(CPL)	Min. Master Reset pulse width with clock low		28		ns	V_{cc}=5.0V, C_L=15pF Fig. 3



Note: D_S, D_1, D_o, are high. Other clock input is grounded.

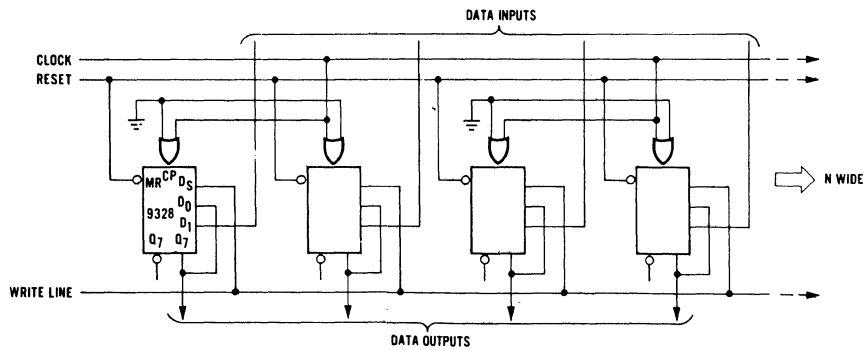
Fig. 2



Note: D_S, D_1, D_0 are high. Other clock input is grounded.

Fig. 3

APPLICATION:



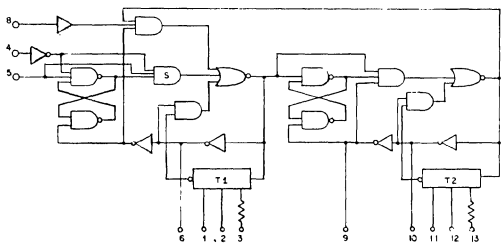
N-BIT BY 8-WORD HIGH-SPEED MEMORY

ANNOUNCEMENT OF ADDITIONAL PRODUCTS EXCLUSIVELY ITT'S

Data Sheets are being prepared on products listed below. Write for your copies.

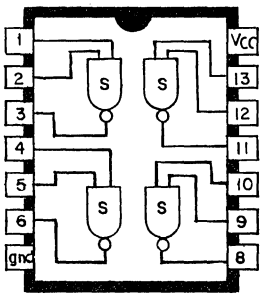
54124/74124 - UNIVERSAL PULSE GENERATOR

- Specially designed for clock and delayed pulse generation
- 2 cascaded multivibrators for delayed pulse
- Gated feedback for high stability controlled oscillation
- No jitter self-start
- Positive Schmitt trigger input

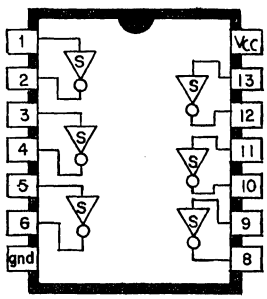


54135/74135, 54137/74137 - QUAD/HEX NAND SCHMITT TRIGGERS

- High input impedance - compatible with 54/74L, MOS, HLL and high voltage transducers, etc.
- Temperature compensated thresholds
- Input load factor 1/4 unit load
- 15 V input rating
- 54135/74135 pin compatible with 54/7400 and 54/74132
- 54137/74137 pin compatible with 54/7404 and 54/7414



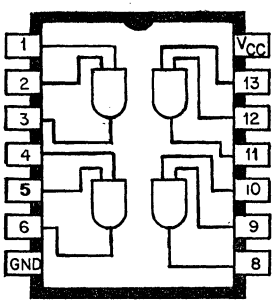
54/74135



54/74137

54130/74130, 54131/74131 - QUAD 2 I/P AND POWER DRIVERS

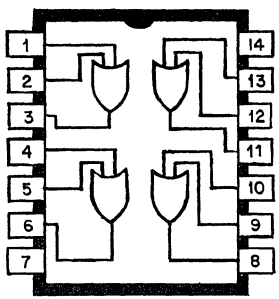
- 100 mA I_{sink}
- 54130/74130 30 V open collector rating
- 54131/74131 15 V open collector rating
- Pin compatible with 54/7408
- V_{OL} at 100 mA = 0.4 V max



54/74130-131

54138/74138, 54139/74139 - QUAD 2 I/P OR POWER DRIVERS

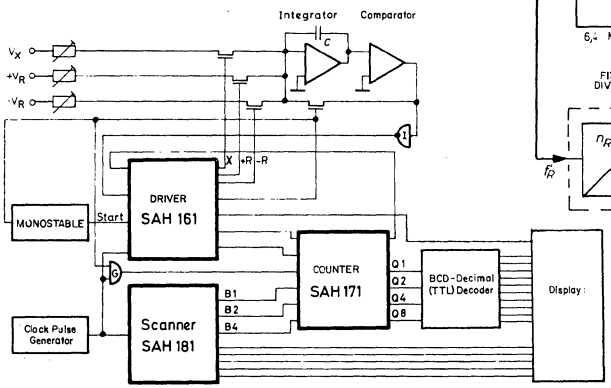
- 100 mA I_{sink}
- 54138/74138 30 V open collector rating
- 54139/74139 15 V open collector rating
- Pin compatible with 54/7432
- V_{OL} at 100 mA = 0.4 V max



54/74138-139

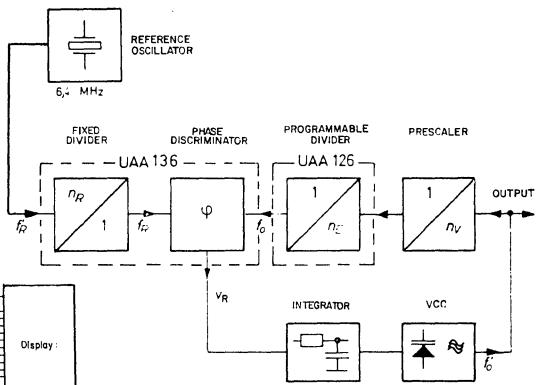
SAH 161, SAH 171, SAH 181 - DIGITAL VOLTMETER KIT

- Kit consists of 3 MOS-LSI Circuits for use in Digital Voltmeters and similar analog to Digital Convertors
- SAH 161 is the clock generator and driver circuit
- SAH 171 is the counter and memory circuit
- SAH 181 is the scanner and display driver
- The use of these three circuits together with a minimum of external components results in a low cost high performance digital voltmeter



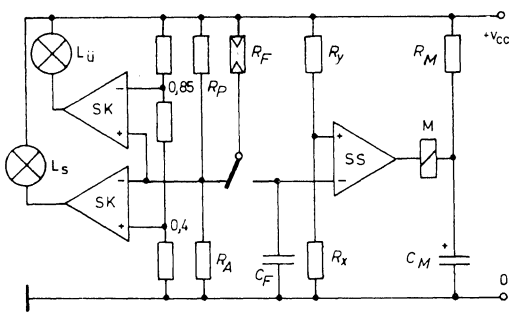
UAA 126, UAA 136 - PHASE SYNCHRONIZED MULTICHANNEL OSCILLATOR KIT

- For use as frequency synthesizer in mobile transmitters/receivers
- 410 channels spaced 25 KHz from 9.25 to 19.5 MHz
- UAA 126 is a programmable divider
- UAA 136 is a fixed divider, phase discriminator
- Can be used for other frequency ranges by using suitable pre-scalers or mixers



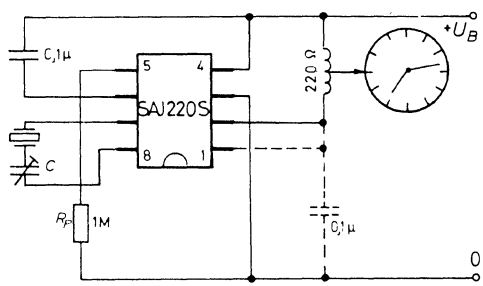
UAA 110 - STILL CAMERA CIRCUIT

- Monolithic integrated circuit for use in still cameras
- Controls exposure under varying light conditions
- Output capability to show need to use a tripod
- Battery monitor



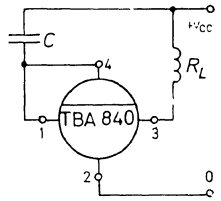
SAJ 220 - FAMILY OF QUARTZ WATCH AND CLOCK CIRCUITS

- Low power/low voltage bipolar technology
- Family offers circuits for use in watches and clocks driven from a quartz crystal
- On chip oscillator, 15 stages and output motor driver on one chip
- Available with different output pulse widths and in micro dip and mini dip packages



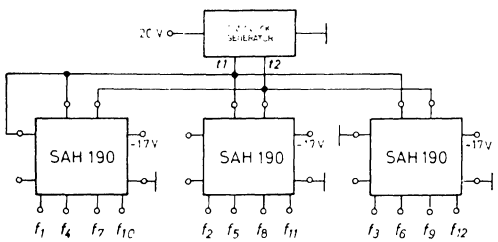
TBA 840 - SINGLE COIL WATCH REGULATOR

- Single monolithic circuit for driving and regulating watches having a single-coil movement
- For use with mercury or silver oxide monocells
- Also usable with tuning fork oscillator watches
- Available in micro-three pin packages



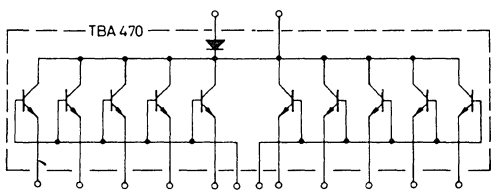
SAH 190 - MOS TOP OCTAVE ELECTRONIC ORGAN TONE GENERATOR

- High accuracy. Less than ±0.003% against tempered tone scale
- Option I allows switching to half or full tone lower
- Option II allows output frequency change by a complete octave
- A full top octave requires three identical devices
- Outputs compatible to drive SAJ 110 seven-stage divider



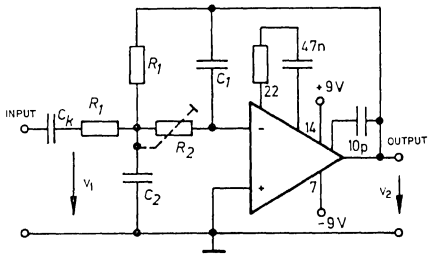
TBA 470 - TEN STAGE GATE. e. g. ELECTRONIC ORGANS

- Allows use of single mechanical contact instead of 10 per key
- Each of the ten separate emitter tone signals are summed at common collector
- Check suppression capability



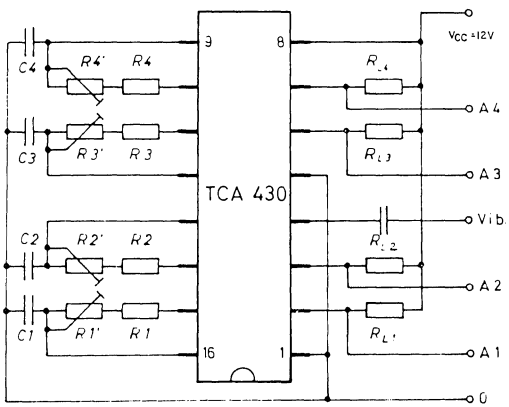
TCA 250 - DUAL ACTIVE FILTER AMPLIFIER

- Dual amplifier circuit designed specifically for active filter applications in audio frequency range
- For use in 2nd order low pass filter using one stage or as a 4th order low pass filter using both stages
- Adjustable roll-off characteristic



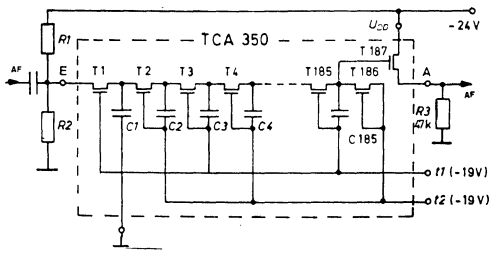
TCA 430 - QUAD-OSCILLATOR (TONE GENERATOR FOR ELECTRONIC ORGANS

- One monolithic chip contains 4 RC oscillators and designed for use in several organ applications
- Three circuits provide a low cost top octave generator with outputs compatible with the SAJ 110 seven-stage frequency divider
- TCA 430 is temperature neutral, thus, accuracy is a function of external R&C
- Separate pin for simultaneous vibrator



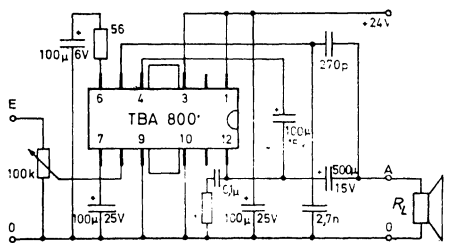
TCA 350 - ANALOG SHIFT REGISTER (DELAY LINE)

- 185 stage "bucket-brigade" delay line for audio frequency signals
- Uses symmetrical clock inputs up to 500 KHz
- Delay can be varied. $t = \frac{185}{2.fclock}$



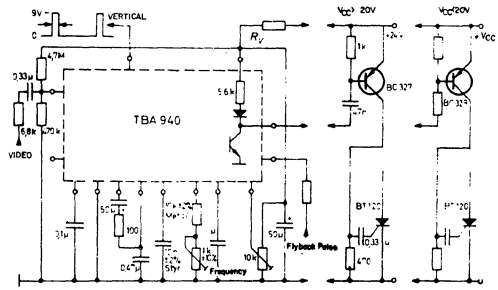
TBA 800 -5 WATTS AUDIO AMPLIFIER

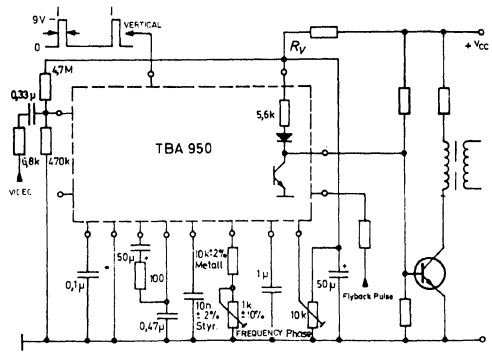
- Monolithic circuit providing 5 watts into 16 Ω at V_{CC} = 24 volts
- For use in Radio, TV and Phono applications
- Uses popular heat tab package designed for on-board heat dissipation



TBA 940, TBA 950 - TV HORIZONTAL DEFLECTION SYSTEMS

- Each circuit contains oscillator and all other functions of TV Horizontal deflection system up to driver
- TBA 940 designed for Thyristor (SCR) Deflection
- TBA 950 designed for Transistor Deflection
- Video recorder drive capability





ITT's 300 Digital Integrated Circuits are designed for applications where a high degree of DC and AC noise immunity is required. The family includes a full complement of gates, inverters, expanders, flip flops, counters and decoders.

ITT HLL is available in in both industrial and military temperature ranges, in both 12v V_{CC} and 15v V_{CC} versions.

ITT 300 Series finds application in electrostatic copy machines, industrial systems such as injection molding or automated welder control, and military systems operating under the most severe conditions where errors caused by noise are intolerable. By virtue of its 12v nominal V_{CC} with relative insensitivity to supply variations, HLL is a perfect choice for automotive applications. In general, any system which previously required relays for logic can benefit from the many capabilities of ITT 300 Series.

- 3.5v guaranteed D.C. noise margin
- 16 pin ceramic or plastic dual in line packages
- 15 volt logic swing or 12 volt logic swing available
- Buffered outputs on all elements
- Insensitivity to short noise pulses
- Choice of full or limited temperature ranges
- Interface with discrete components and Linear I.C.
- Line driving and receiving capabilities

NAND GATES/INVERTERS

ITT 321 QUAD 2 INPUT NAND GATE (ACTIVE PULL-UP)
ITT 322 DUAL 5 INPUT NAND GATE (ACTIVE PULL-UP)
ITT 323 QUAD 2 INPUT NAND GATE (OPEN COLLECTOR)
ITT 324 QUAD 2 INPUT NAND GATE (PASSIVE PULL-UP)
ITT 325 DUAL 2 INPUT, DUAL 3 INPUT NAND GATE (ACTIVE PULL-UP)
ITT 326 DUAL 2 INPUT, DUAL 3 INPUT NAND GATE (PASSIVE PULL-UP)
ITT 332 QUAD INVERTER, DUAL 2 INPUT NAND GATE (OPEN COLLECTOR)
ITT 333 QUAD INVERTER, DUAL 2 INPUT NAND GATE (PASSIVE PULL-UP)
ITT 334 HEX INVERTER WITH STROBE (OPEN COLLECTOR)
ITT 335 HEX INVERTER WITH STROBE (PASSIVE PULL-UP)

BUFFERS

ITT 301 DUAL 5 INPUT NAND BUFFER (ACTIVE PULL-UP)
ITT 302 QUAD 2 INPUT NAND BUFFER (OPEN COLLECTOR)
ITT 303 QUAD 2 INPUT NAND BUFFER (PASSIVE PULL-UP)

AND - OR - INVERT GATES

ITT 341 DUAL 2 WIDE, 2 INPUT AND-OR-INVERT GATE (ACTIVE PULL-UP)
ITT 344 DUAL 2 WIDE, 2 INPUT AND-OR-INVERT GATE (W/OUTPUT EXPANDER)

EXPANDERS

ITT 331 DUAL 5 INPUT EXPANDER

FLIP-FLOPS

ITT 311 MASTER/SLAVE FLIP-FLOP
ITT 312 DUAL J-K FLIP-FLOP
ITT 342 DUAL ONE SHOT MULTIVIBRATOR
ITT 370 QUAD D FLIP-FLOP (LATCH)

INTERFACE ELEMENTS

ITT 361 DUAL HIGH LEVEL TO DTL/TTL INTERFACE
ITT 362 DUAL DTL/TTL TO HIGH LEVEL INTERFACE
ITT 363 QUAD DTL/TTL TO HIGH LEVEL INTERFACE

DECODERS

ITT 380 ONE-OF-TEN DECODER/DRIVER
ITT 381 ONE-OF-TEN DECODER

COUNTERS

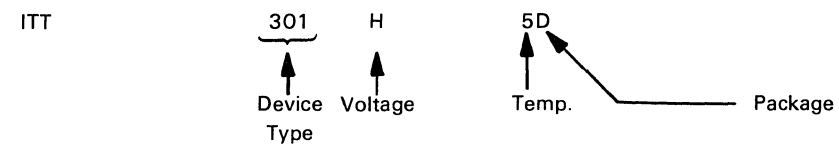
ITT 371 DECADE COUNTER
ITT 372 HEXADECIMAL COUNTER

ABSOLUTE MAXIMUM RATINGS

Characteristics	Units
Storage Temperature Range	
Ceramic	-65°C to +150 °C
Plastic	-55°C to +100 °C
Operating Temperature Range	
ITT300-1D	−55°C to +125 °C
ITT300-1D1	−55°C to +125 °C
ITT300-5D	−30°C to +85 °C
ITT300-5D1	−30°C to +75 °C
Lead Temperature, 1/16 inch from case, 10 seconds maximum	300 °C
Supply Voltage - Continuous	+16.5 Volts
Supply Voltage - Pulsed <0.1 second	+18 Volts
Input Voltage - (exclusive of expanders)	
12V Version	−0.5V to +16.5 Volts
15V Version	−0.5V to +18.0 Volts
Input Voltage - expanders	0 V to +6.0 Volts
Voltage applied to output	−0.5V to +16.5 Volts
Sink Current at T_A =25°C, continuous	
301 & 302	80 mA
All other types	15 mA
Surge Sink Current at T_A =25°C, <1 sec.	
301 & 302	100 mA
All other types	20 mA
Output Short Circuit Duration to GND	Continuous

ORDERING INFORMATION

The full type number designates temperature range, voltage and package as follows:



Part No.	TEMP RANGE	V_{CC}(Nominal)	PACKAGE	CROSS REFERENCE ITT (obsolete)	CROSS REFERENCE TELEDYNE
ITT 3xx −5N	−30°C to +85°C	12V	Plastic Dip	5N	CJ
ITT 3xxH−5N	−30°C to +70°C	15V	Plastic Dip	5N1	AJ
ITT 3xx −5D	−30°C to +85°C	12V	Ceramic Dip	5D	CL
ITT 3xxH−5D	−30°C to +70°C	15V	Ceramic Dip	5D1	AL
ITT 3xx −1D	−55°C to +125°C	12V	Ceramic Dip	1D	BL
ITT 3xxH−1D	−55°C to +125°C	15V	Ceramic Dip	1D1	ML

PARAMETER	DEFINITION	12V VERSION (V_{CC} = +12V ±1V)	15V VERSION (V_{CC} = +15V ±1V)	TEST CONDITIONS
V_{IL}	Input threshold voltage, low	5.0V MIN	5.0V MIN	Guaranteed input low threshold for all inputs except 311 T_2 = 4.8V MIN at 15V
V_{IH}	Input threshold voltage, high (except 311 $\overline{S}$ and $\overline{R}$)	6.5V MAX	6.5V MAX	Guaranteed input high threshold for all inputs (except 311 $\overline{S}$ and $\overline{R}$)
	V_{IH} of 311 $\overline{S}$ and $\overline{R}$ inputs	7.0V MAX	7.0V MAX	Guaranteed V_{IH} of 311 $\overline{S}$ and $\overline{R}$ inputs
I_{IL}	Input current, low; 1 unit load	2.1 mA MAX	2.6 mA MAX	At V_{CC} MAX with V_{IN} = V_{OL1} MAX
I_{IH}	Input leakage current; 1 unit load	10 μA MAX	10 μA MAX	At V_{CC} MAX with V_{IN} = V_{CC} MAX
V_{OL}	Output low voltage (see loading table on data sheet for applicable V_{OL}			
	V_{OL1} - generally applicable	1.5V MAX	1.8V MAX	I_{OL} = F.O. x UL
	V_{OL2} - 301 buffer only	1.8V MAX	2.0V MAX	I_{OL} = F.O. x UL At V_{CC} MIN with
	V_{OL3} - open collector types	0.4V MAX	0.4V MAX	I_{OL} = F.O. x UL V_{IL} = 5.0V, V_{IH} = 6.5V
	V_{OL4} - 380 decoder only	1.2V MAX	1.2V MAX	I_{OL} = 30 mA
V_{OH}	Output high voltage of all devices	10.0V MIN	13.0V MIN	At V_{CC} MIN, V_{IL} = 5.0V, V_{IH} = 6.5V; I_{OH} = F.O. x UL
I_{OH}	Output high source of active pullup devices current of 301	5.0mA MIN 15 mA MIN	5.0 mA MIN 15 mA MIN	At V_{CC} nominal, V_{IL} = 5.0V, V_{IH} = 6.5V; V_{OH} = 7.0V for 12V VERSION, 9.5V for 15V VERSION
V_{MAX}	Output high breakdown voltage of the following devices			At I_{MAX} of
	302 and 323 gates	13.0V MIN	16.5V MIN	4 mA At V_{CC} MAX, V_{IL} = 5.0V
	332 and 334 inverters	20.0V MIN	24.0V MIN	4 mA V_{IH} = 6.5V, with
	380 decoder	24.0V MIN	24.0V MIN	0.5 mA I_{MAX} forced into input
	381 decoder	15.0V MIN	15.0V MIN	0.5 mA
I_{CEX1}	Output high leakage current of open collector devices	25 μA MAX	25 μA MAX	At V_{CC} MAX, V_{IL} = 5.0V, V_{IN} = 6.5V; V_{CEX} = V_{CC} MAX
V_{CC} MAX	TEST SUPPLY VOLTAGE	13.0V	16.0V	
V_{CC} MIN	TEST SUPPLY VOLTAGE	11.0V	14.0V	
V_{CC} NOM	TEST SUPPLY VOLTAGE	12.0V	15.0V	

F.O. is fanout in unit loads (UL). Unit loadings are given in the pin tables on the individual data sheets. A unit load for ITT 300 Series is defined by the above input specifications.

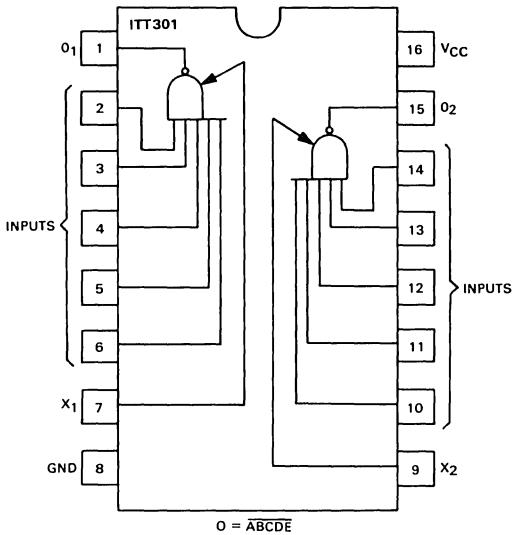
SUMMARY OF DEVICE PROPAGATION DELAYS AND WORST-CASE SUPPLY CURRENTS

Device	Delay Range (nanoseconds)		Worst-Case I_{CC}(mA) 12V	15V
301 dual 5-input power NAND gate	240	400	48	68
302 quad 2-input power NAND gate (OC)	240	600	40	60
303 quad 2-input power NAND gate (PP*)	240	600	49	70
311 master/slave flip-flop	250	820	18	25
312 dual J-K or S-R flip-flop	230	600	30	40
321 quad 2-input NAND gate	200	300	15	20
322 dual 5-input NAND gate	190	550	8	11
323 quad 2-input NAND gate (OC)	160	400	5.5	8
324 quad 2-input NAND gate (PP)	200	600	28	40
325 2,2,3,3-input NAND gate	200	300	15	20
326 2,2,3,3-input NAND gate (PP)	200	600	28	40
331 dual 5-input gate expander			4.2	5.2
332 hex inverter gate (OC)	140	350	28	42
333 hex inverter gate (PP)	140	350	42	60
334 strobed hex inverter (OC)	140	350	28	42
335 strobed hex inverter (PP)	140	350	42	60
341 dual 2-input AND-OR-INVERT gate	150	410	11	15
342 dual monostable multivibrator	160	260	17	23
344 dual exclusive-OR gate	200	600	10	14
361 dual input interface	230	325	8	11
362 dual output interface	100	400	10	13
363 quad output interface	240	600	51	64
370 quad latch	500	500	38	48
371 decade counter	200	800	41	53
372 hexadecimal counter	200	800	41	53
380 BCD to decade decoder/driver	NA	NA	30	38
381 BCD to decade decoder	300	500	30	38

NOTE: Only the shortest and longest delays are listed for each device.
See the device data sheets for all input-output propagation delays.

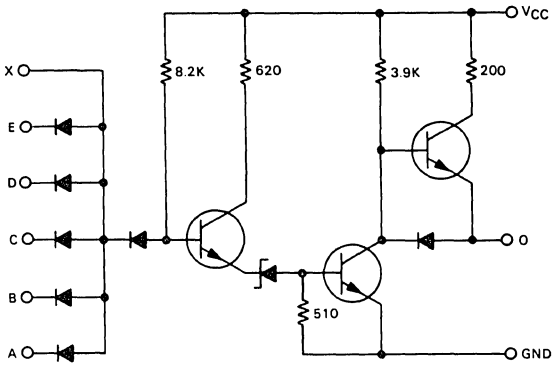
The ITT 301 is an active pull-up element featuring high current capability in both the high and low state. It is an excellent choice for driving long transmission lines, as a system clock driver, or for driving any load with high capacitance or inductance.

PIN CONFIGURATION



$O = \overline{ABCDE}$

SCHEMATIC (EACH GATE)

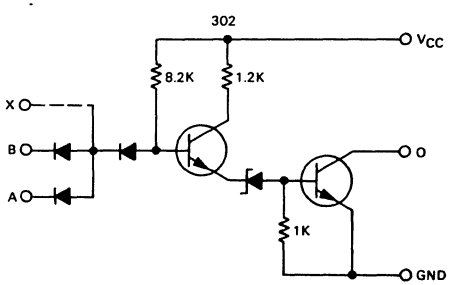


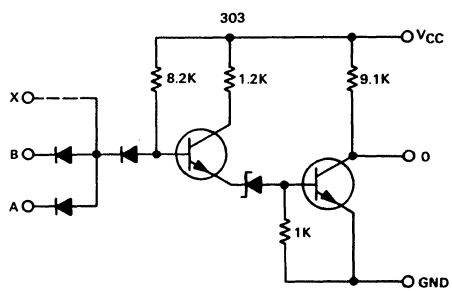
PINS	FUNCTION	LOADING
A-E	Inputs	1 UL
X	Expanders	
O	Outputs	20 UL at V_{OL1} (12V or 15V) 30 UL at V_{OL2} (12V) 25 UL at V_{OL2} (15V)

* Each diode tied to X_1 or X_2 is 1 unit load.

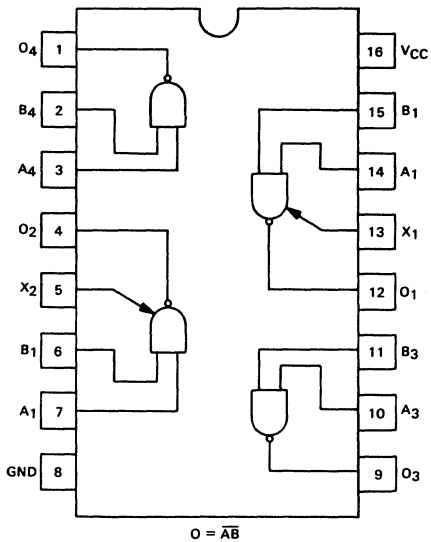
The ITT 302 and 303 are open collector and passive pull-up, respectively, power gates with high current sinking capability. Both devices are "wire-or" capable and find application as lamp drivers or high-fanout gates.

SCHEMATIC





PIN CONFIGURATION



PINS	FUNCTION	LOADING
A,B	Inputs	1 UL
X	Expanders	
O	Outputs	5 UL at V_{OL1} 20 UL at V_{OL1}

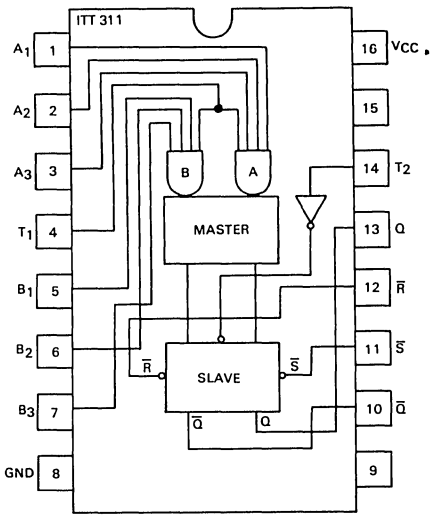
20 unit loads handled with correct external resistor

302 handles 10 TTL loads at V_{OL3}

* Each diode tied to X_1 or X_2 is 1 unit load.

The ITT 311 is a universal HLL flip-flop. It has separate clocks which allow two-phase (dual inhibit) operation, direct set and reset inputs, six data inputs, and is level sensitive. It can be operated as a J-K flip-flop by external wiring and features active outputs.

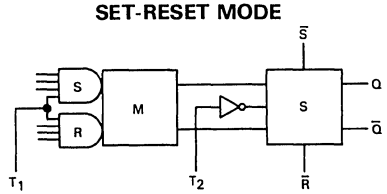
PIN CONFIGURATION



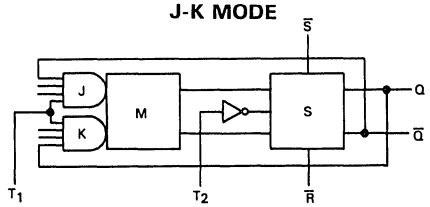
PINS	FUNCTION	LOADING
A,B	Data inputs	1 UL
T_1	Clock input	2 UL
T_2	Clock input	1 UL
$\bar{S}$,$\bar{R}$	Direct $\bar{S}$-$\bar{R}$ inputs	1 UL
Q,$\bar{Q}$	Outputs	5 UL at V_{OL1}

CIRCUIT DIAGRAM

SET-RESET MODE



J-K MODE



J-K OPERATION

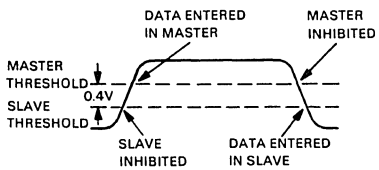
A	B	Q^{n+1}
L	L	Q^n
L	H	L
H	L	H
H	H	$\bar{Q}^n$

S-R OPERATION

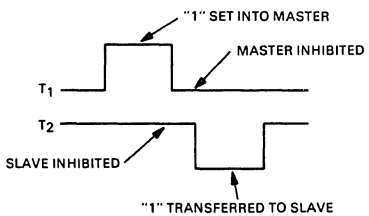
A	B	Q^{n+1}
L	L	Q^n
L	H	L
H	L	H
H	H	X

X = Undetermined

SINGLE-PHASE TIMING

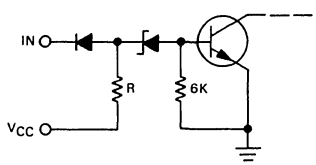


TWO-PHASE TIMING



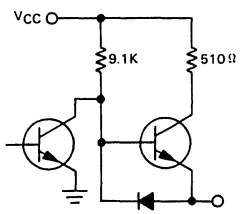
SCHEMATIC

TYPICAL INPUT



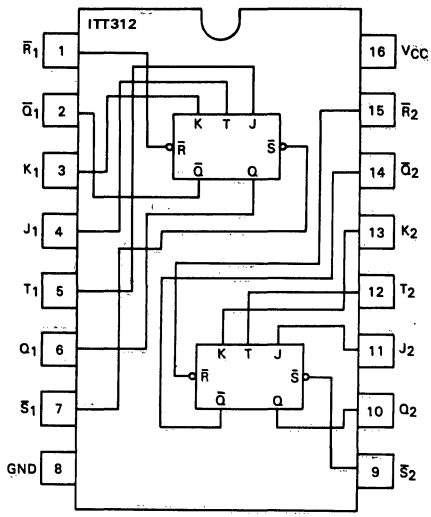
R = 8.2K ON A, B, $\bar{S}$, $\bar{R}$, T_2
R = 4.1K ON T_1

TYPICAL OUTPUT



Two completely separated J-K flip-flops are incorporated on one 312 chip. Each flip-flop has its own separate clock, set, and reset inputs. The device clock is negative edge sensitive, requiring a clock fall time of 3 volts per microsecond or faster. Active-high outputs are provided.

PIN CONFIGURATION



TRUTH TABLE

S-R MODE

$\overline{S}$	$\overline{R}$	Q
H	H	X
H	L	L
L	H	H
L	L	H

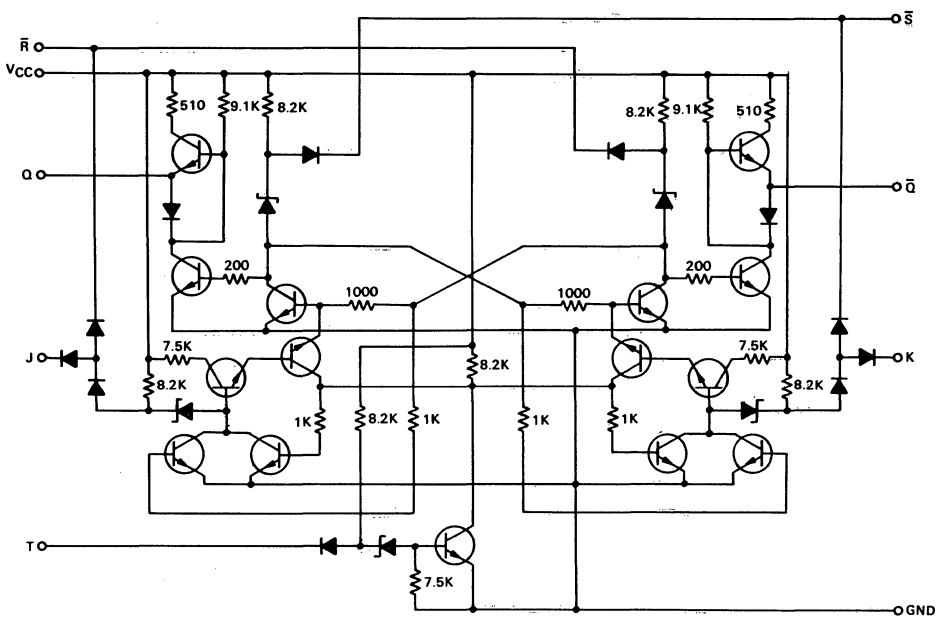
J-K MODE

J	K	Q^{n+1}
L	L	Q^n
L	H	L
H	L	H
H	H	$\overline{Q}^n$

X = Indeterminate state

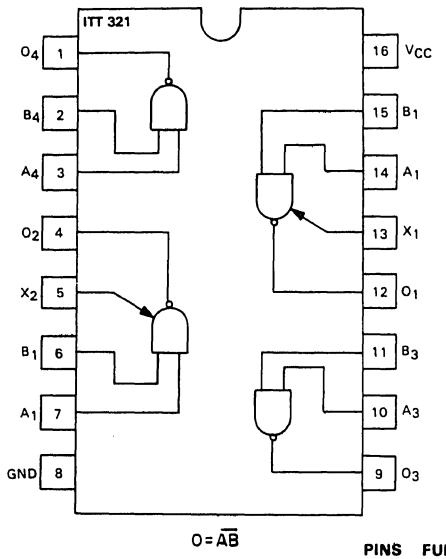
PINS	FUNCTION	LOADING
J,K	J-K inputs	1 UL
T	Clock inputs	1 UL
$\overline{S},\overline{R}$	Direct $\overline{S}$-$\overline{R}$ inputs	2 UL
Q,$\overline{Q}$	Outputs	5 UL at V_{OL1}

SCHEMATIC (EACH FLIP-FLOP)



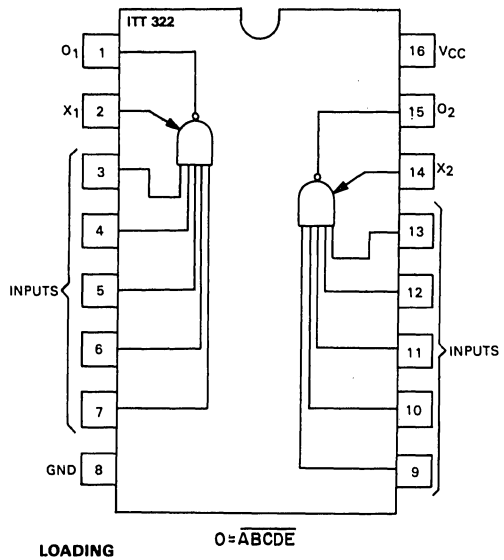
The ITT 321, 322, 325, and 341 make up the active - output group of HLL gates. Active-high outputs have high source current capability for driving lines of moderate length or high capacitance loads.

PIN CONFIGURATION



$O = \overline{AB}$

PIN CONFIGURATION

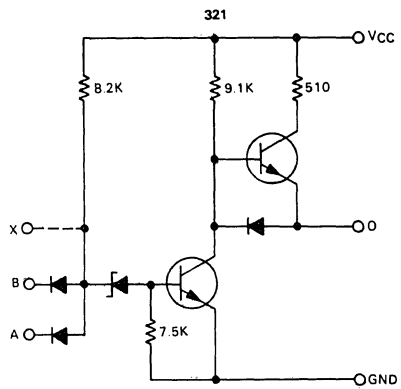


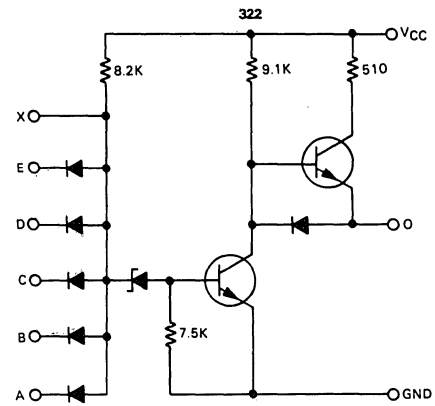
$O = \overline{ABCDE}$

PINS	FUNCTION	LOADING
A-E	Inputs	1 UL
X	Expanders	*
O	Outputs	5 UL at V_{OL1}

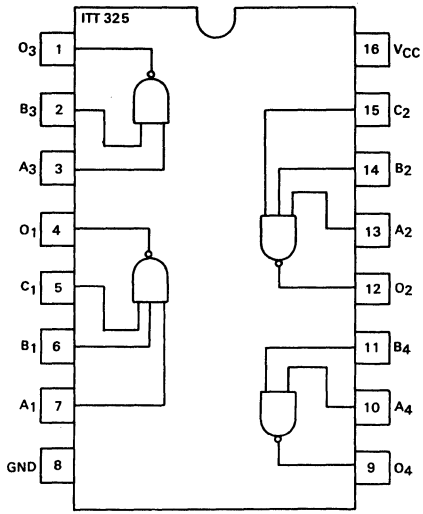
* Each diode tied to X_1 or X_2 is 1 unit load.

SCHEMATIC (EACH GATE)





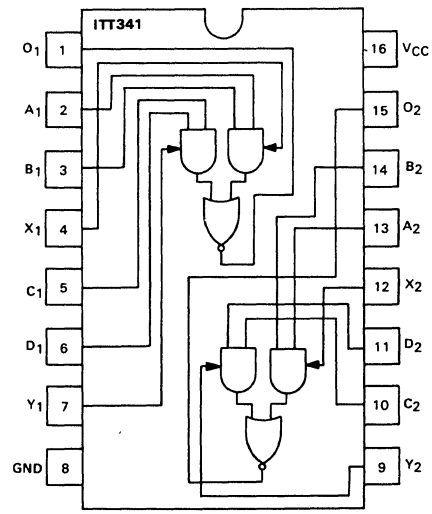
PIN CONFIGURATION



$O = \overline{AB}$ $O = \overline{ABC}$

PINS	FUNCTION	LOADING
A-C	Inputs	1 UL
O	Outputs	5 UL at V_{OL1}

PIN CONFIGURATION

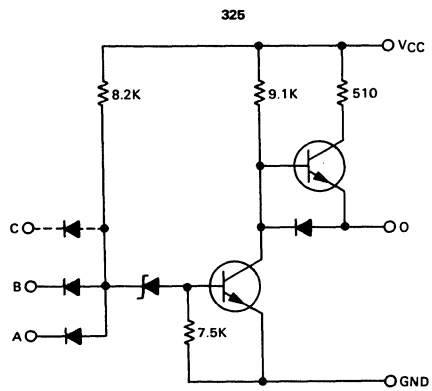


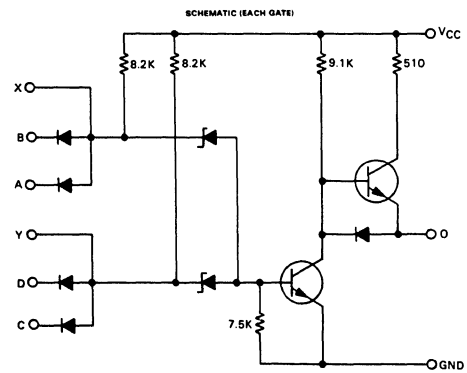
$O = \overline{AB \& CD}$

PINS	FUNCTION	LOADING
A-D	Inputs	1 UL
X	Expanders	
O	Outputs	5 UL at V_{OL1}

* Each diode tied to X_1 or X_2 is 1 unit load.

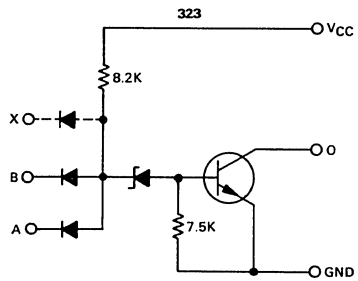
SCHEMATIC (EACH GATE)



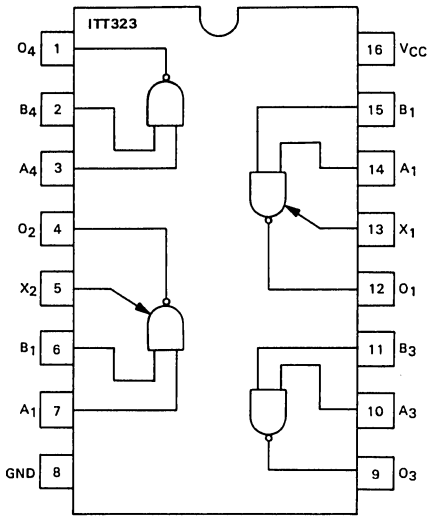


The ITT 323, 332, and 334 are HLL's open-collector gates. Open, or uncommitted, collectors can be , or connected through an appropriate pull-up resistor to a power supply other than that used for the HLL gate. This capability allows open-collector devices to interface directly to DTL, TTL, or MOS, or to drive small indicator lamps or relays directly.

SCHEMATIC



PIN CONFIGURATION

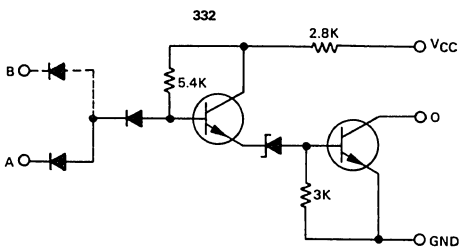


$O = \overline{AB}$

PINS	FUNCTION	LOADING
A,B	Inputs	1 UL
X	Expanders	*
O	Outputs	5 UL at V_{OL1}

*Each diode tied to X_1 or X_2 is 1 unit load

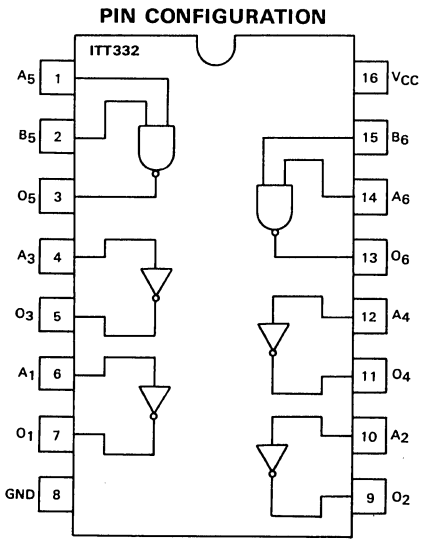
SCHEMATIC



PINS	FUNCTION	LOADING
A,B	Inputs	1 UL
O	Outputs	5 UL at V_{OL1}
		7 UL at V_{OL1}

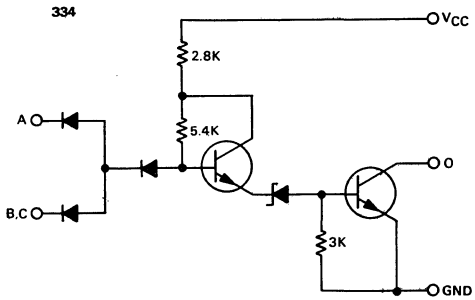
Either device handles 7 unit loads with correct external pullup resistor.

PIN CONFIGURATION

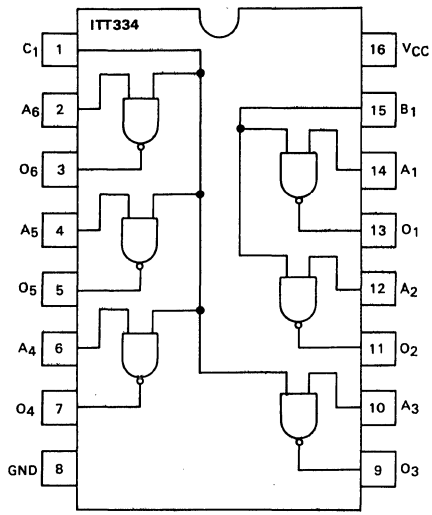


$O = \overline{A}$
$O = \overline{AB}$

SCHEMATIC



PIN CONFIGURATION

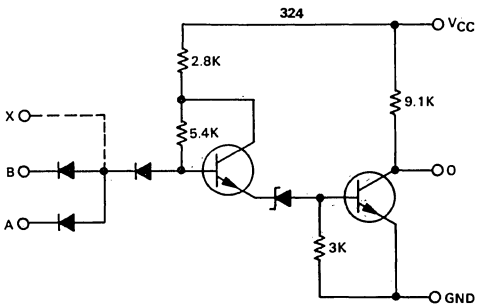


PINS	FUNCTION	LOADING
A	Data inputs	1 UL
B	Strobe input	2 UL
C	Strobe input	4 UL
O	Outputs	5 UL at V_{OL1} 7 UL at V_{OL2}

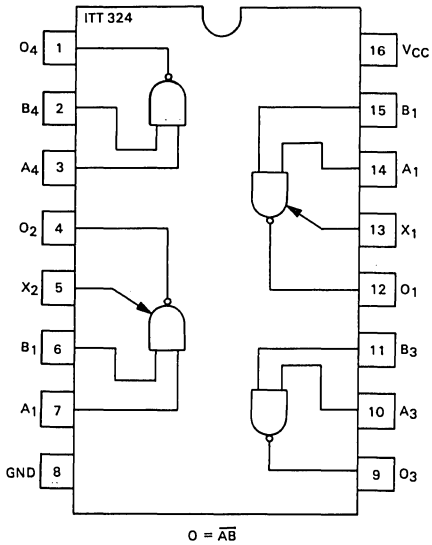
Either device handles 7 unit loads if correct external resistor is used

The ITT 324, 326, 333, and 335 employ 9.1K passive pull-up resistors on the chip. Passive pull-up has as its main advantage the wire-or capability, so these gates find wide application in internal logic systems.

SCHEMATIC



PIN CONFIGURATION



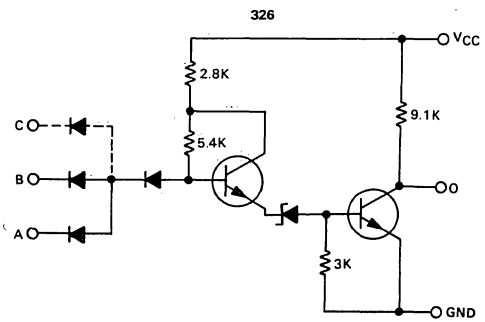
$O = \overline{AB}$

PINS	FUNCTION	LOADING
A,B	Inputs	1 UL
X	Expanders	*
O	Outputs	5 UL at V_{OL1} 7 UL V_{OL1}

* Each diode tied to X_1 or X_2 is 1 unit load

324 handles 7 unit loads with external pullup resistor.

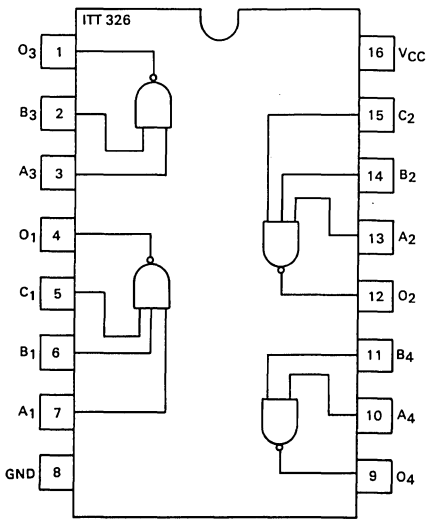
SCHEMATIC



PINS	FUNCTION	LOADING
A-C	Inputs	1 UL
O	Outputs	5 UL at V_{OL1} 7 UL at V_{OL1}

326 handles 7 unit loads with external pullup resistor.

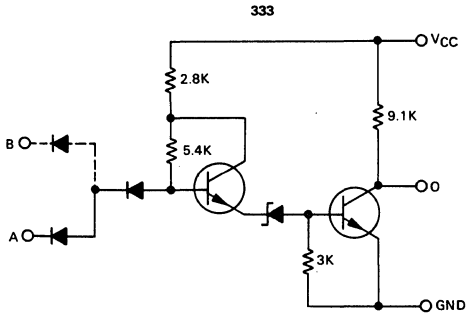
PIN CONFIGURATION



$O = \overline{ABC}$
$O = \overline{AB}$

ITT333 – QUAD INVERTER, DUAL 2-INPUT NAND GATE
ITT335 – STROBED HEX INVERTER

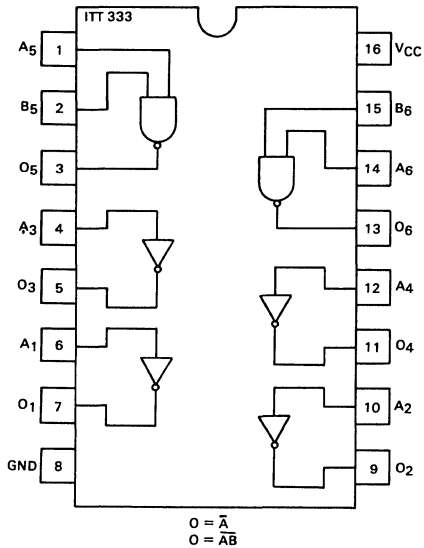
SCHEMATIC



PINS	FUNCTION	LOADING
A,B	Inputs	1 UL
O	Outputs	5 UL at V_{OL1} 7 UL at V_{OL1}

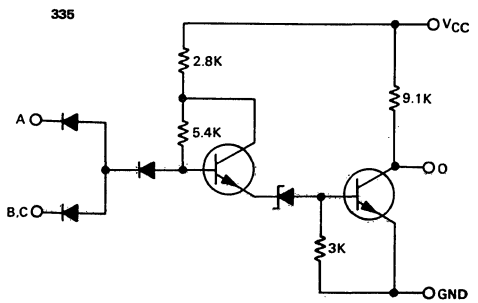
Device handles 7 unit loads if correct external resistor is used.

PIN CONFIGURATION



$O = \overline{A}$
$O = \overline{AB}$

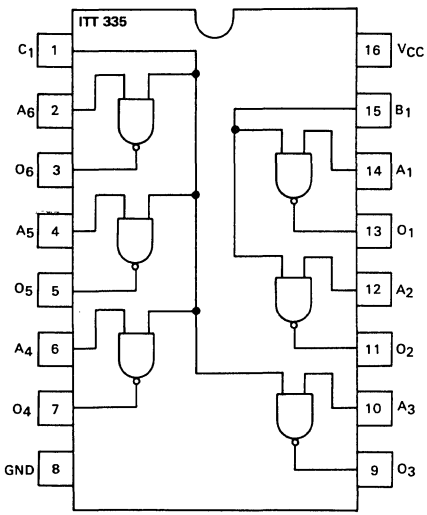
SCHEMATIC



PINS	FUNCTION	LOADING
A	Data inputs	1 UL*
B	Strobe input	2 UL
C	Strobe input	4 UL
O	Outputs	5 UL at V_{OL1} 7 UL at V_{OL2}

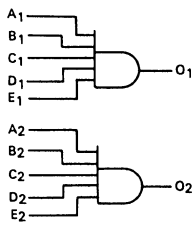
*Device handles 7 unit loads if correct external resistor is used.

PIN CONFIGURATION

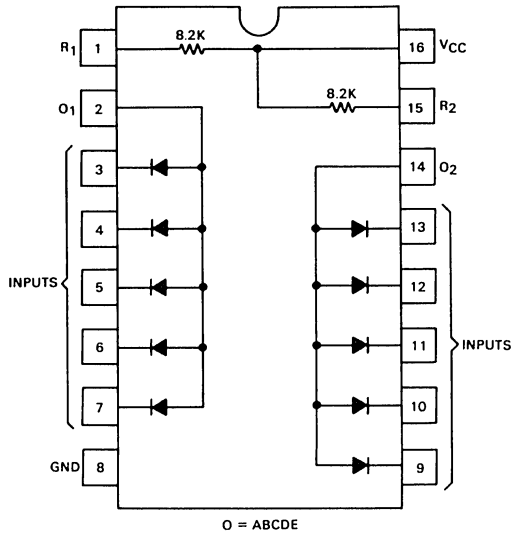


The ITT 331 consists of two arrays of HLL input diodes which are used on the expander inputs of HLL devices. Two 8.2.K nominal resistors are also available on the chip, allowing the 331 to be used as a second level dual 5-input AND gate.

LOGIC DIAGRAM



PIN CONFIGURATION



PINS	FUNCTION	LOADING
A-E	Inputs	1 UL
O	Outputs	

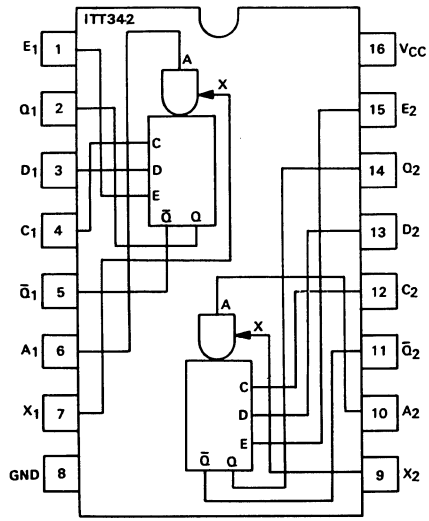
Two completely independent one-shots are provided on the 342 chip. Each one shot has an expandable trigger and provides complimentary output pulses of any length, as determined by an external timing capacitor. Outputs are active-high.

The 342 is triggered on the positive going edge of the input pulse. Maximum operating frequency is limited by the pulse width and recovery time of the particular circuit application. An external timing capacitor is required in conjunction with an internal or external timing resistor.

Pulse width is determined by the formula PW~ 0.7 RC, with PW in Nanoseconds, R in ohms, and C in Picofarads. The timing capacitor C has no restriction on value, but the timing resistor should be held between 2 and 6.2 KΩ. An internal 20 Km ±25% resistor is provided for normal applications.

Recovery time is given by $T_R = 3C$ with T_R in Nanoseconds and C in Picofarads. This is the time required to recharge the timing capacitor to the proper voltage.

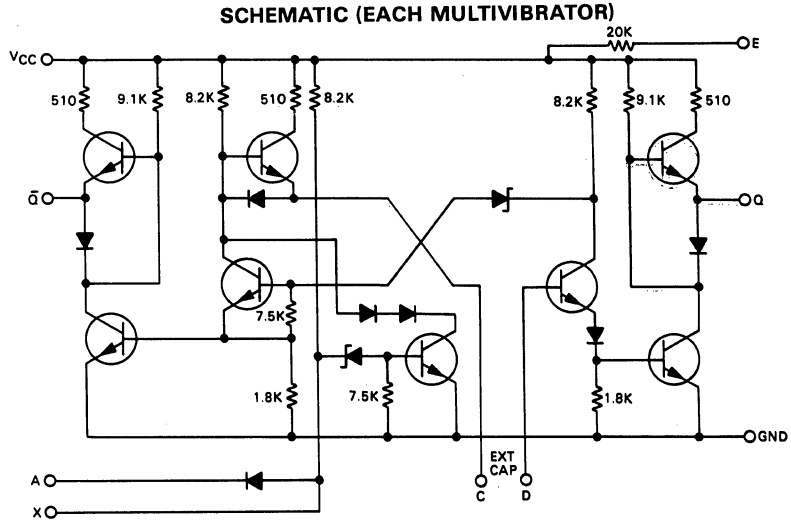
PIN CONFIGURATION



PINS	FUNCTION	LOADING
A	Trigger inputs	1 UL
C-E	Timing network	N.A.
X	Expanders	
Q,Q̄	Outputs	5 UL at V_{OL1}

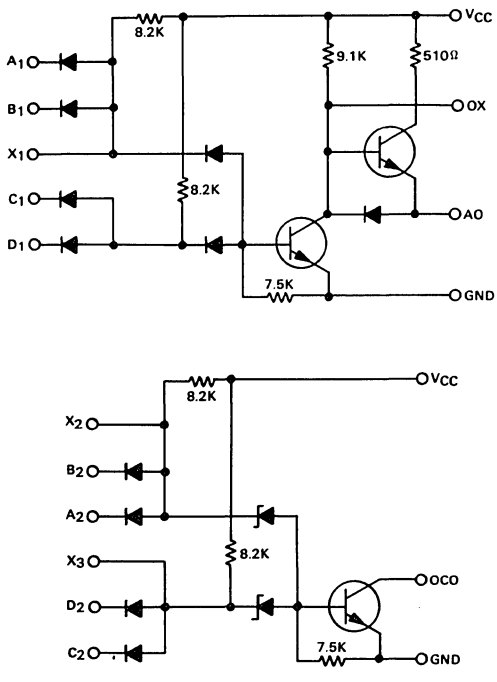
* Each diode tied to X_1 or X_2 is 1 unit load.

SCHEMATIC (EACH MULTIVIBRATOR)



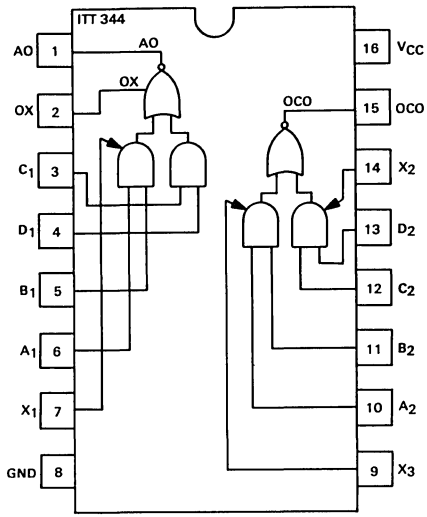
The ITT 344 is an extremely versatile gate. The output expander allows the device to be wired-or with other passive pullup or open-collector devices, and still retain the desirable characteristics of an active-pullup output.

SCHEMATIC



V_{CC} and ground are shown separated in the schematic for clarity. The device has common V_{CC} and ground pins.

PIN CONFIGURATION

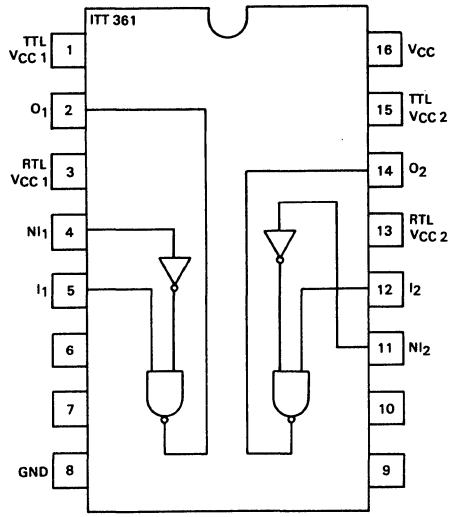


O = AB AND CD

PINS	FUNCTIONS	LOADING
A-D	Inputs	1 UL
AO	Active output	5 UL at V_{OL1}
OX	Output expander	5 UL at V_{OL1}
OCO	Open collector	N.A. 5 UL at V_{OL1} 7 UL at V_{OL2}

The ITT 361, 362 and 363 are designed to directly interface HLL with other, low threshold logic families - TTL, DTL, RTL and DCTL. The 361 and 362 have both inverting and non-inverting interface capability, while the 363 functions as a NAND interface. Only one input per gate of the 361 or 362 should be used at any one time, with other inputs tied to remove them from the circuit to avoid possible ambiguous outputs.

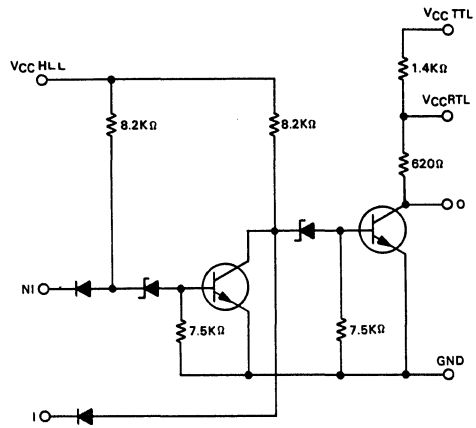
PIN CONFIGURATION



PINS	FUNCTION	LOADING
I	Inverting input	1 UL
NI	Noninverting input	1 UL
O	Output	*

*See specifications

SCHEMATIC



361 INTERFACE SPECIFICATIONS

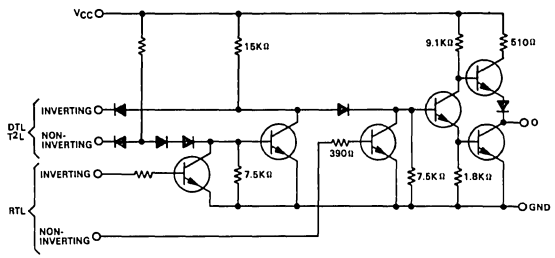
Outputs connected for TTL, over applicable temperature range

V_{OL} = 0.4V at I_{OL} = 6.4 mA, V_{CC} = 5.5V
V_{OH} = 2.4V at I_{OH} = −160 va, V_{CC} = 4.5V

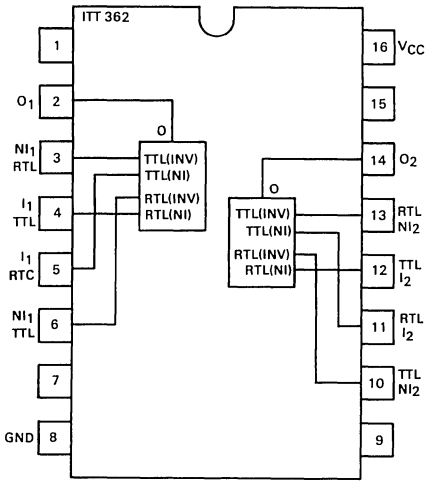
Outputs connected for RTL — V_{CC} = 3.0V

	Full Temp Range			Limited Temp Range		
Temp °C	−55	+25	+125	−30	+25	+85
V_{OL} @ 6 mA	0.33V	0.3V	0.35V	0.33V	0.3V	0.35V
H_{OH}	1.01V	0.85V	0.675V	0.9	0.85	0.76
I_{OH}	−2.5 mA	−2.5 mA	−2.3 mA	−2.3 mA	−2.2 mA	−2.0 mA

SCHEMATIC



PIN CONFIGURATION



362 INTERFACE SPECIFICATIONS

Inputs connected for TTL, over applicable temp range

I_R = 10Ua
$-I_F$ = −1.6 mA
V_{IH} = 2.0V
V_R = 4.0V
V_F = 0.4V
V_{IL} = 0.8V

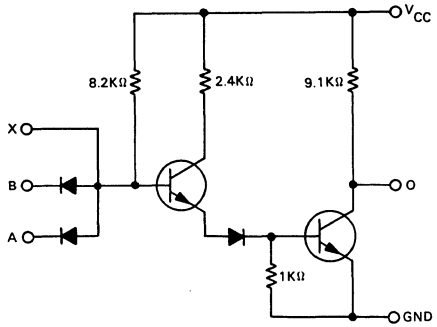
PINS	FUNCTIONS	LOADING
O	Output	5 UL*
Inputs	See schematic	See specs

*Fanout is 5 HLL unit loads at V_{OH} = 8.5V and V_{CC} = 11.0V, or at V_{OH} = 11.5V and V_{CC} = 14.0V.

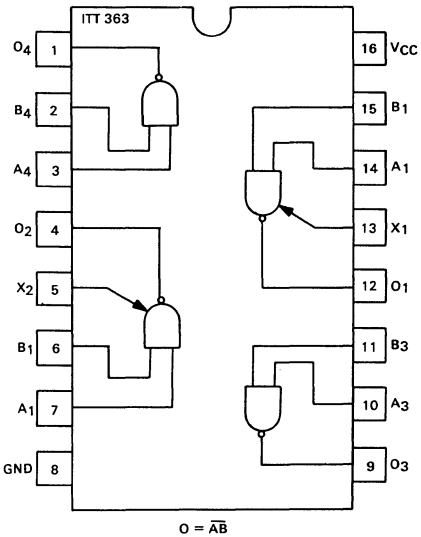
Inputs connected for RTL

	°C Full Temp Range			°C Limited Temp Range		
	−55	+25	+125	−30°	+25°	+85°
I_R(Ua)	495	440	470	460	440	470
V_R	1.01V	0.85V	0.675V	0.95	0.85	0.70
V_F	0.71	0.5	0.32	0.6	0.5	0.38
$-I_F$	−1.0Ua	−1.0Va	−10.0Ua	−1.0Ua	−1.0Va	−10.0Ua

SCHEMATIC



PIN CONFIGURATION



INTERFACE SPECIFICATIONS

$I_R = 10\,U_a$ $V_R = 4.0V$ $V_{CC} = 13V$ OR $16V$
$-I_F = 2.4mA$ $V_F = 0.4V$ $V_{CC} = 13V$
$-I_F = 3.0mA$ $V_F = 0.4V$ $V_{CC} = 16V$
$V_{IL} = 0.8V$ $V_{IH} = 2.0V$

features active outputs.

PINS	FUNCTIONS	LOADING
A,B	TTL inputs	1 TTL load
X	Expanders	*
O	Outputs	5 UL at V_{OL1} 20 UL at V_{OL1}

*TTL expander input loading applies

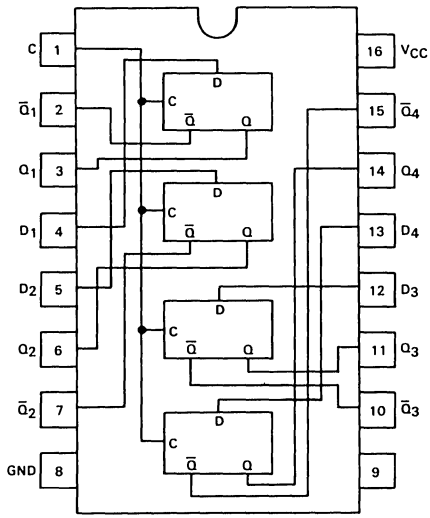
Four D-type flip-flops utilizing a common clock line make up the 370. Each flip-flop has complimentary passive pull up outputs with a single D input. This circuit is ideal as a quad latch for temporary storage of 4-bit binary numbers.

Data is transferred from D inputs to outputs when the clock line is low. With the clock line high, output data is held and D inputs are ignored.

TRUTH TABLE

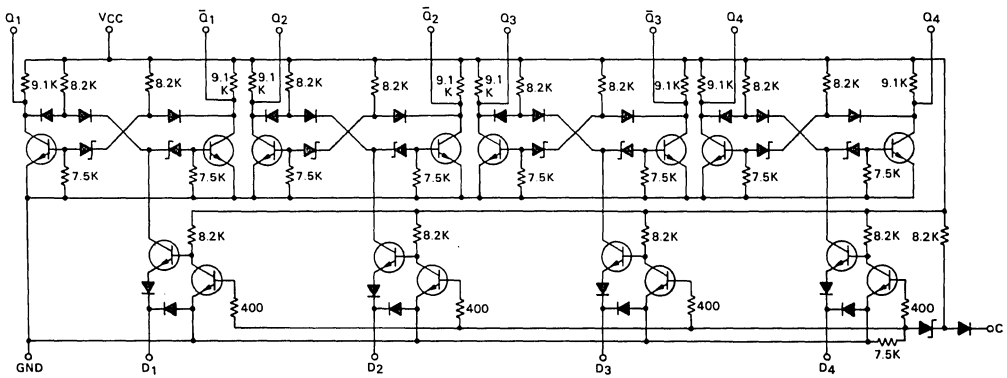
C	D	Q^{n+1}
1	1	Q^n
1	0	Q^n
0	1	1
0	0	0

PIN CONFIGURATION



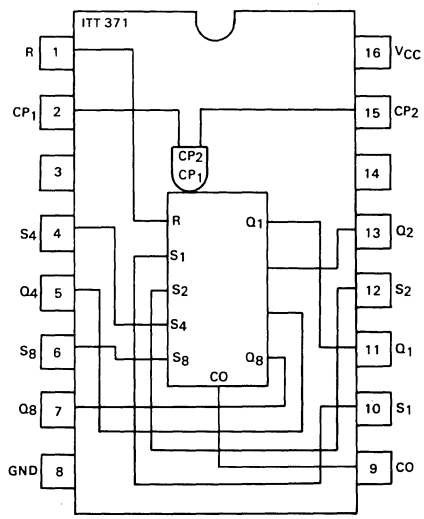
PINS	FUNCTION	LOADING
D	Data inputs	2 UL
C	Clock input	1 UL
Q,$\bar{Q}$	Outputs	5 UL at V_{OL1}

SCHEMATIC



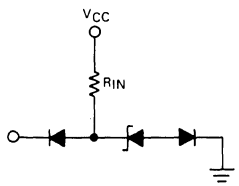
The ITT 371 HLL MSI counter generates BCD on its outputs. It has direct set inputs for each of its four internal flip-flops and a common reset. Two clock inputs are provided, facilitating the input ENABLE function. A ninth count output is provided as a carry output for cascading 371's so a decimal number of any size may be generated. The passive outputs are ideal inputs to the 380 Series BCD decoders.

PIN CONFIGURATION

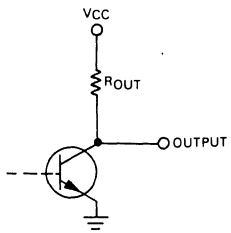


PINS	FUNCTION	LOADING
CP	Clock inputs	2 UL
R	Direct reset input	1 UL
S	Direct set input	1/2 UL
CO	Carry output	2 UL
Q	Outputs	5 UL at V_{OL1}

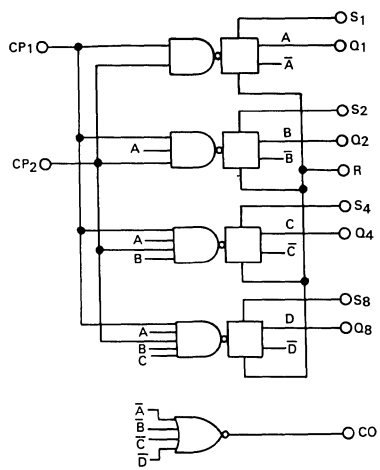
TYPICAL INPUT



TYPICAL OUTPUT



LOGIC DIAGRAM



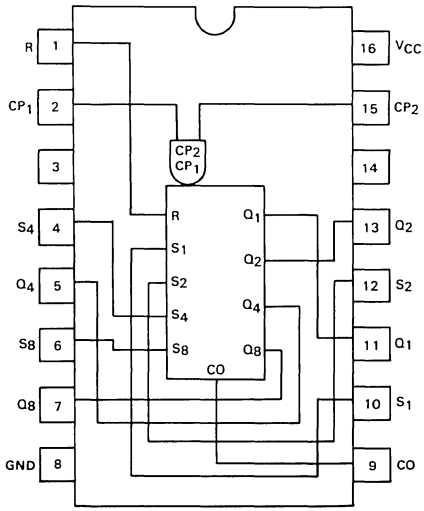
INPUT	R_{IN}
CP_1 CP_2	5 KΩ TYP.
RESET	5 KΩ TYP.
ALL SETS	20 KΩ TYP.

OUTPUT	R_{OUT}
Q_1 Q_2	9.1 KΩ TYP.
$Q_3 + Q_4$	
CO	9.1 KΩ TYP.

The ITT 372 is identical to the ITT 371 except its outputs are coded in the standard 4-bit binary (1-2-4-8) code.
Operation of the 372 is identical to that of the 371. Internal construction produces divide-by-sixteen operation.

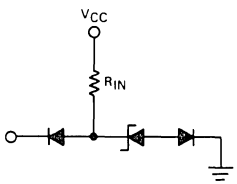
The 371 is level sensitive, counting as the clock goes low. Holding either clock low will inhibit the count sequence. Direct set or reset is accomplished by switching the desired input high. All unused direct set and reset inputs must be grounded.

PIN CONFIGURATION

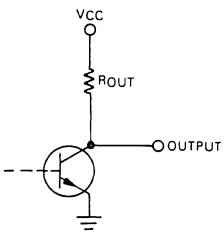


PINS	FUNCTION	LOADING
CP	Clock inputs	2 UL
R	Direct reset input	1 UL
S	Direct set input	1/2 UL
CO	Carry output	2 UL
Q	Outputs	5 UL at V_{OL1}

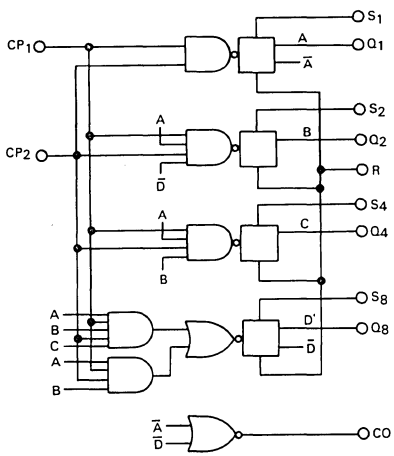
TYPICAL INPUT



TYPICAL OUTPUT



LOGIC DIAGRAM

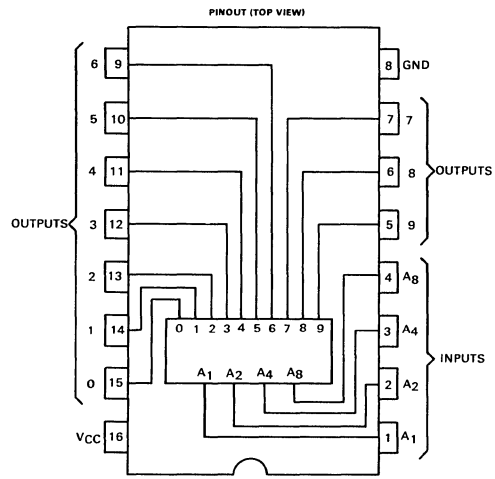


INPUT	R_{IN}
CP_1 CP_2	5 KΩ TYP.
RESET	5 KΩ TYP.
ALL SETS	20 KΩ TYP.

OUTPUT	R_{OUT}
Q_1 Q_2	9.1 KΩ TYP.
$Q_3 + Q_4$	
CO	9.1 KΩ TYP.

The 380 and 381 decode standard BCD (1-2-4-8) inputs to produce a low state on one of the ten open collector outputs. Internal design insures that no ambiguous outputs are produced, turning off all outputs when addressed by input codes for 10-15. The 380 is intended to drive small lamps directly or can be used with various interface buffering schemes. The 381 is identical to the 380 with the exception of its output ratings and is intended for use as an internal circuit element.

PIN CONFIGURATION



TRUTH TABLE

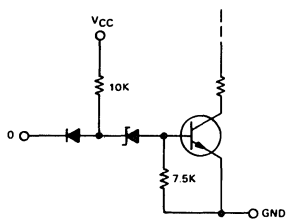
INPUTS				OUTPUTS								
A_1	A_2	A_4	A_8	0	1	2	3	4	5	6	7	8	9
0	0	0	0	0	1	1	1	1	1	1	1	1	1
1	0	0	0	1	0	1	1	1	1	1	1	1	1
0	1	0	0	1	1	0	1	1	1	1	1	1	1
1	1	0	0	1	1	1	0	1	1	1	1	1	1
0	0	1	0	1	1	1	1	0	1	1	1	1	1
1	0	1	0	1	1	1	1	1	0	1	1	1	1
0	1	1	0	1	1	1	1	1	1	0	1	1	1
1	1	1	0	1	1	1	1	1	1	1	0	1	1
0	0	0	1	1	1	1	1	1	1	1	1	0	1
1	0	0	1	1	1	1	1	1	1	1	1	1	0
0	1	0	1	1	1	1	1	1	1	1	1	1	1
1	1	0	1	1	1	1	1	1	1	1	1	1	1
0	0	1	1	1	1	1	1	1	1	1	1	1	1
1	0	1	1	1	1	1	1	1	1	1	1	1	1
0	1	1	1	1	1	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1	1	1	1	1

Table on Page 54

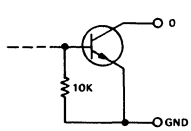
PINS	FUNCTION	LOADING
A	BCD inputs	1 UL
0-9	Outputs	

*Unit loading does not apply

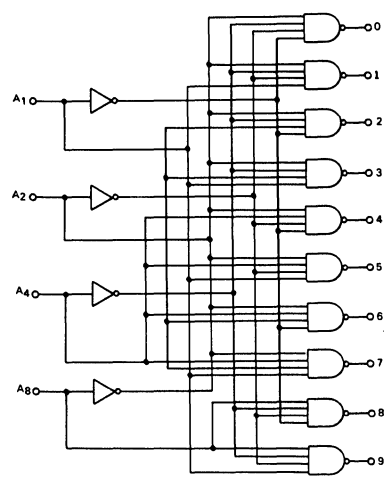
TYPICAL INPUT



TYPICAL OUTPUT



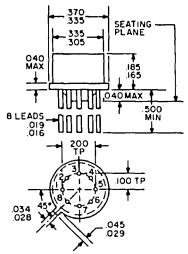
LOGIC DIAGRAM



HIGH PERFORMANCE OPERATIONAL AMPLIFIER

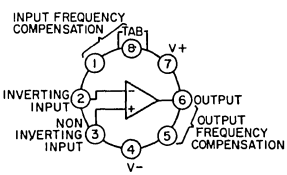
- Tight Transient Response Specs
- Low Input Offset Voltage
- Large Input Common Mode Range
- High Output Voltage Swing

DIMENSIONS
SIMILAR TO TO-5



NOTE: DIMENSIONS AS PER LATEST JS-10 COMMITTEE.
ALL DIMENSIONS IN INCHES.
LEADS ARE GOLD-PLATED KOVAR.
PACKAGE WEIGHT IS .863 GRAMS.

CONNECTION DIAGRAM
(Top View)



NOTE: PIN 4 CONNECTED TO CASE.

The MIC 709-A is a high-gain operational amplifier constructed on a single silicon chip using the ITT Planar epitaxial process. It features low offset, high input impedance, large input common mode range, high output swing under load and low power consumption. The device displays exceptional temperature stability and will operate over a 14-36 voltage range with little degradation of performance. The amplifier is intended for use in DC servo systems, high impedance analog computers, in low-level instrumentation applications and for the generation of special linear and nonlinear transfer functions. The 709A is a direct plug in replacement for the 709.

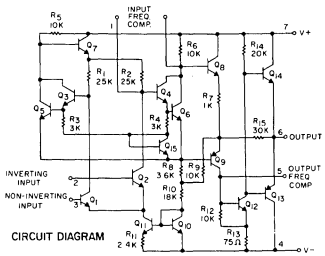
ABSOLUTE MAXIMUM RATINGS

CHARACTERISTICS		UNITS
Supply Voltage	36	Volts
Internal Power Dissipation (Note 1)	300	mW
Differential Input Voltage	±5.0	Volts
Input Voltage	±10	Volts
Output Short-Circuit Duration ($T_A = 25°C$)	5	sec
Storage Temperature Range	−65 to +150	°C
Operating Temperature Range	−55 to +125	°C
Lead Temperature (Soldering, 60 sec)	300	°C

NOTE 1: Rating applies for case temperatures to +125°C; derate linearly at 5.6 mW/°C for ambient temperatures above +95°C.

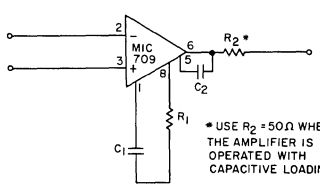
ELECTRICAL CHARACTERISTICS ($T_A = +25°C$, $\pm 9V \leq V_S \leq \pm 15V$ unless otherwise noted)

PARAMETER (see definitions)	MIN.	TYP.	MAX.	UNITS	CONDITIONS
Input Offset Voltage		0.6	2.0	mV	$R_S \leq 10K\Omega$
Input Offset Current		10	50	nA	
Input Bias Current		100	200	nA	
Input Resistance	350	700		KΩ	
Output Resistance		150		Ω	
Power Consumption		75	108	mW	$V_S = \pm 15V$
Transient Response					$V_{in} = 20mV$, $R_L = 2K\Omega$,
Risetime			1.5	μs	$C_1 = 5000$ pF, $R_1 = 1.5$ KΩ,
					$C_2 = 200$pF, $R_2 = 50\Omega$
Overshoot			30	%	$C_L \leq 100$pF
The following specifications apply for $-55°C \leq T_A \leq +125°C$:					
Input Offset Voltage			3.0	mV	$R_S \leq 10K\Omega$
Average Temperature Coefficient		1.8	10	μV/°C	$R_S = 50\Omega$ $T_A = +25°C$ TO $T_A = +125°C$
of Input Offset Voltage		1.8	10	μV/°C	$R_S = 50\Omega$ $T_A = +25°C$ TO $T_A = -55°C$
		2.0	15	μV/°C	$R_S \leq 10K\Omega$ $T_A = +25°C$ TO $T_A = +125°C$
		4.8	25	μV/°C	$R_S = 10K\Omega$ $T_A = +25°C$ TO $T_A = -55°C$
		0.08	0.5	nA/°C	$T_A = +25°C$ TO $T_A = +125°C$
		0.45	2.8	nA/°C	$T_A = +25°C$ TO $T_A = +55°C$
Large-Signal Voltage Gain					$V_S = \pm 15V$, $R_L \geq 2K\Omega$,
	25,000		70,000		$V_{out} = \pm 10V$
Output Voltage Swing	±12	±14		V	$V_S = \pm 15V$, $R_L \geq 10K\Omega$
	±10	±13		V	$V_S = \pm 15V$, $R_L \geq 2K\Omega$
Input Voltage Range	±8.0			V	$V_S = \pm 15V$
Common Mode Rejection Ratio	80	110		db	$R_S \leq 10K\Omega$
Supply Voltage Rejection Ratio		40	100	μV/V	$R_S \leq 10K\Omega$
Supply Current		2.1	3.0	mA	$T_A = +125°C$, $V_S = \pm 15V$
		2.7	4.5	mA	$T_A = -55°C$, $V_S = \pm 15V$
Power Consumption		63	90	mA	$T_A = +125°C$, $V_S = \pm 15V$
		81	135	mA	$T_A = -55°C$, $V_S = \pm 15V$
Input Offset Current		35	50	nA	$T_A = +125°C$
		40	250	nA	$T_A = -55°C$
Input Bias Current		300	600	nA	$T_A = -55°C$
Input Resistance	85	170		kΩ	

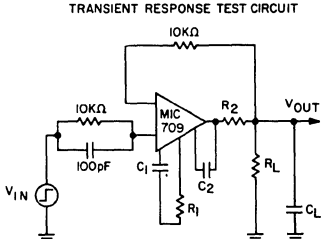


CIRCUIT DIAGRAM

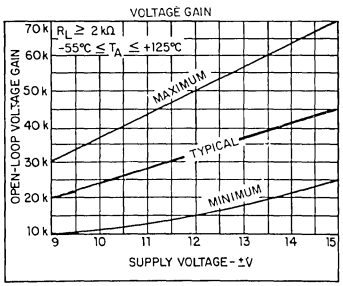
FREQUENCY COMPENSATION CIRCUIT

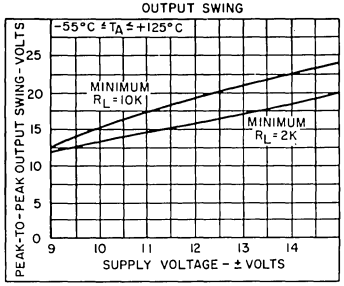


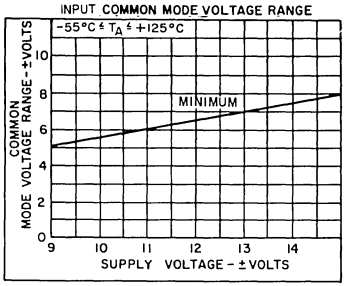
TRANSIENT RESPONSE TEST CIRCUIT



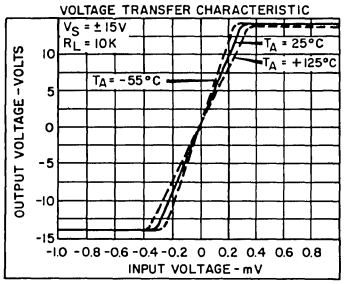
GUARANTEED ELECTRICAL CHARACTERISTICS

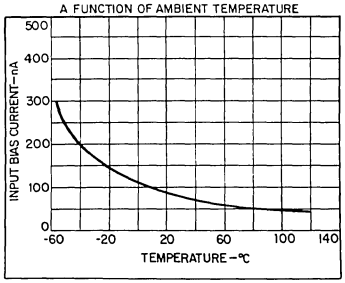


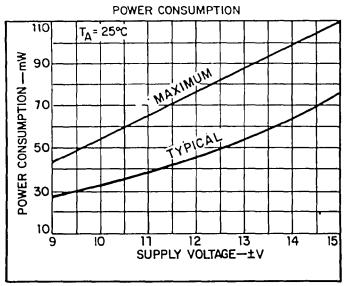


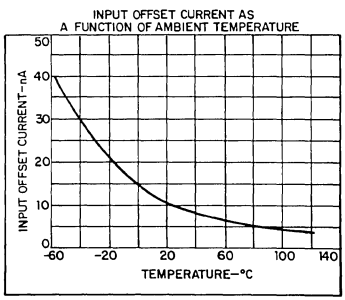


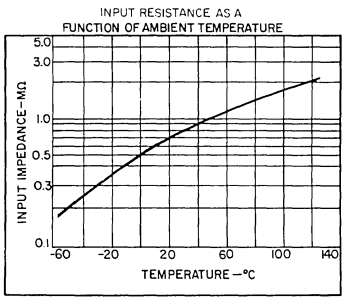
TYPICAL PERFORMANCE CURVES

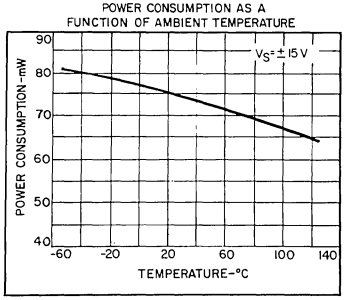


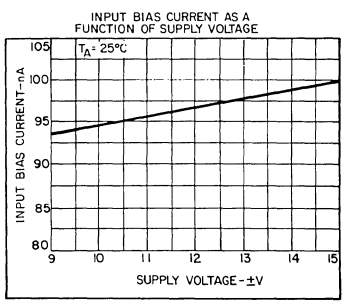


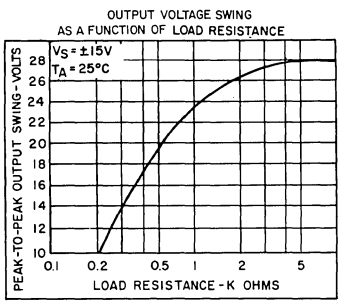


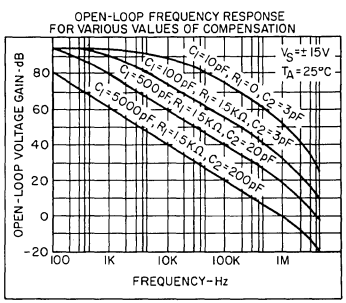




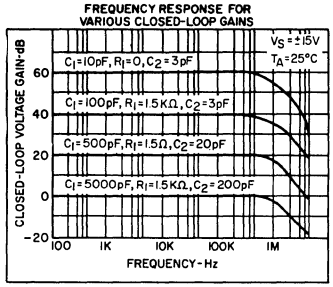


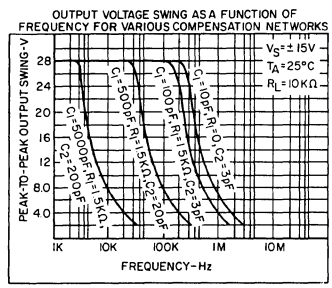


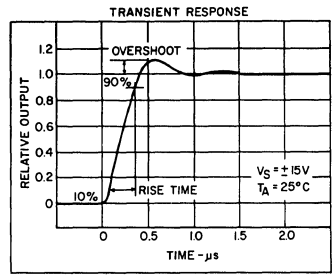


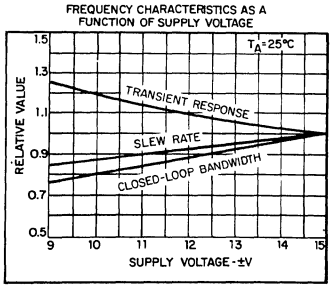


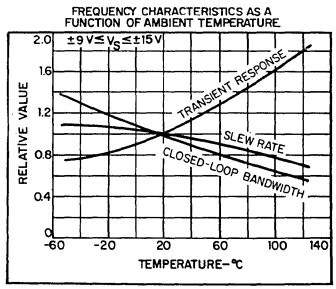
TYPICAL PERFORMANCE CURVES, continued

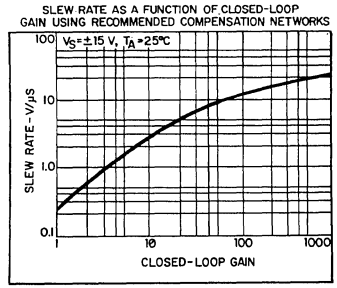


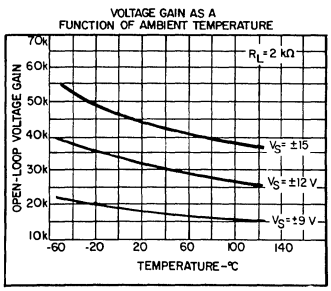


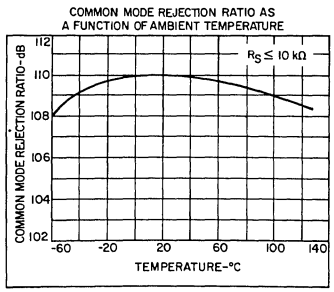












DEFINITION OF TERMS:

INPUT OFFSET VOLTAGE—That voltage which must be applied between the input terminals to obtain zero output voltage. The input offset voltage may also be defined for the case where two equal resistances are inserted in series with the input leads.

INPUT OFFSET CURRENT—The difference in the currents into the two input terminals with the output at zero volts.

INPUT RESISTANCE—The resistance looking into either input terminal with the other grounded.

INPUT BIAS CURRENT—The average of the two input currents.

INPUT VOLTAGE RANGE—A range of voltage which, if exceeded on either input terminal, could cause the amplifier to cease functioning properly.

INPUT COMMON MODE REJECTION RATIO—The ratio of the input voltage range to the maximum change in input offset voltage over this range.

LARGE-SIGNAL VOLTAGE GAIN—The ratio of the maximum output voltage swing with load to the change in input voltage required to drive the output from zero to this voltage.

OUTPUT VOLTAGE SWING—The peak output swing, referred to zero, that can be obtained without clipping.

OUTPUT RESISTANCE—The resistance seen looking into the output terminal with the output at null. This parameter is defined only under small signal conditions at frequencies above a few hundred cycles to eliminate the influence of drift and thermal feedback.

POWER CONSUMPTION—The DC power required to operate the amplifier with the output at zero and with no load current.

SUPPLY VOLTAGE REJECTION RATIO—The ratio of the change in input offset voltage to the change in supply voltage producing it.

TRANSIENT RESPONSE—The closed-loop step function response of the amplifier under small-signal conditions.

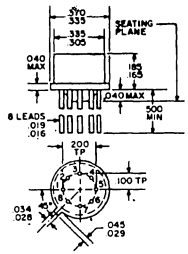
HIGH PERFORMANCE OPERATIONAL AMPLIFIER

- **Tight Transient Response Specs**
- **Low Input Offset Voltage**
- **Large Input Common Mode Range**
- **High Output Voltage Swing**

The MIC709-1 and MIC709-5 are high-gain operational amplifiers constructed on a single silicon chip using the ITT Planar epitaxial process. They feature low offset, high input impedance, large input common mode range, high output swing under load and low power consumption. The devices display exceptional temperature stability and will operate over a wide voltage range with little degradation of performance. These amplifiers are intended for use in DC servo systems, high impedance analog computers, in low-level instrumentation applications and for the generation of special linear and nonlinear transfer functions. The devices utilize the same pin configuration.

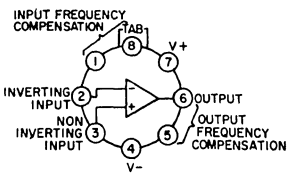
DIMENSIONS

SIMILAR TO TO-5



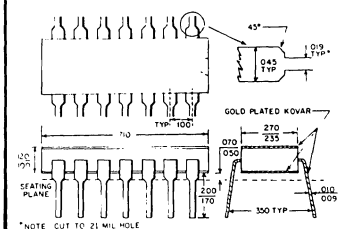
NOTE: DIMENSIONS AS PER LATEST JS-10 COMMITTEE.
ALL DIMENSIONS IN INCHES
LEADS ARE GOLD-PLATED KOVAR.
PACKAGE WEIGHT IS .863 GRAMS

CONNECTION DIAGRAM
(Top View)



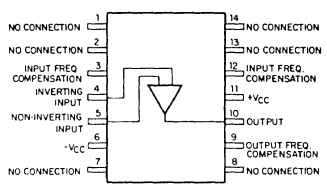
NOTE: PIN 4 CONNECTED TO CASE.

DUAL IN-LINE PACKAGE



*NOTE CUT TO 21 MIL HOLE

CONNECTION DIAGRAM



ABSOLUTE MAXIMUM RATINGS

CHARACTERISTICS		UNITS
Supply Voltage	±18	Volts
Internal Power Dissipation (Note 1)	300	mW
Differential Input Voltage	±5.0	Volts
Input Voltage	±10	Volts
Output Short-Circuit Duration ($T_A = 25°C$)	5	sec.
Storage Temperature Range	−65 to +150	°C
Operating Temperature Range (Note 2)	−55 to +125	°C
Lead Temperature (Soldering, 60 sec)	300	°C

NOTE 1: Rating applies to the MIC709-1 at case temperatures to +125°C; derate linearly at 5.6 mW/°C for ambient temperatures above +95°C. The rating for the MIC709-5 is 250mW and applies for case temperatures to +70°C.

NOTE 2: Rating for the MIC709-5 is 0° to +70°C.

ELECTRICAL CHARACTERISTICS ($T_A = +25°C$, $\pm 9V \leq V_S \leq \pm 15V$ unless otherwise noted)

PARAMETER (see definitions)	MIN.	TYP.	MAX.	UNITS	CONDITIONS
Input Offset Voltage		1.0	5.0	mV	$R_S \leq 10K\Omega$
Input Offset Current		50	200	nA	
Input Bias Current		200	500	nA	
Input Resistance	150	400		KΩ	
Output Resistance		150		Ω	
Power Consumption		80	165	mW	$V_S = \pm 15V$
Transient Response Risetime Overshoot		 0.3 10	 1.0 30	 μs %	$V_{in} = 20mV$, $R_L = 2K\Omega$, $C_1 = 5000$ pF, $R_1 = 1.5$ KΩ, $C_2 = 200pF$, $R_2 = 50\Omega$ $C_L \leq 100pF$
The following specifications apply for $-55°C \leq T_A \leq +125°C$:					
Input Offset Voltage			6.0	mV	$R_S \leq 10K\Omega$
Average Temperature Coefficient of Input Offset Voltage		 3.0 6.0		 μV/°C μV/°C	 $R_S = 50\Omega$ $R_S \leq 10K\Omega$
Large-Signal Voltage Gain	 25,000	 45,000	 70,000		$V_S = \pm 15V$, $R_L \geq 2K\Omega$, $V_{out} = \pm 10V$
Output Voltage Swing	±12 ±10	±14 ±13		V V	$V_S = \pm 15V$, $R_L \geq 10K\Omega$ $V_S = \pm 15V$, $R_L \geq 2K\Omega$
Input Voltage Range	±8.0	±10		V	$V_S = \pm 15V$
Common Mode Rejection Ratio	70	90		db	$R_S \leq 10K\Omega$
Supply Voltage Rejection Ratio		25	150	μV/V	$R_S \leq 10K\Omega$
Input Offset Current		20 100	200 500	nA nA	$T_A = +125°C$ $T_A = -55°C$
Input Bias Current		0.5	1.5	μA	$T_A = -55°C$
Input Resistance	40	100		kΩ	

DEFINITION OF TERMS:

INPUT OFFSET VOLTAGE—That voltage which must be applied between the input terminals to obtain zero output voltage. The input offset voltage may also be defined for the case where two equal resistances are inserted in series with the input leads.

INPUT OFFSET CURRENT—The difference in the currents into the two input terminals with the output at zero volts.

INPUT RESISTANCE—The resistance looking into either input terminal with the other grounded.

INPUT BIAS CURRENT—The average of the two input currents.

INPUT VOLTAGE RANGE—A range of voltage which, if exceeded on either input terminal, could cause the amplifier to cease functioning properly.

INPUT COMMON MODE REJECTION RATIO—The ratio of the input voltage range to the maximum change in input offset voltage over this range.

LARGE-SIGNAL VOLTAGE GAIN—The ratio of the maximum output voltage swing with load to the change in input voltage required to drive the output from zero to this voltage.

OUTPUT VOLTAGE SWING—The peak output swing, referred to zero, that can be obtained without clipping.

OUTPUT RESISTANCE—The resistance seen looking into the output terminal with the output at null. This parameter is defined only under small signal conditions at frequencies above a few hundred cycles to eliminate the influence of drift and thermal feedback.

POWER CONSUMPTION—The DC power required to operate the amplifier with the output at zero and with no load current.

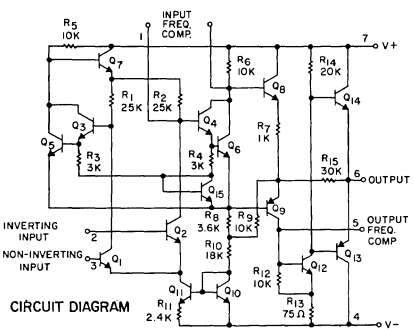
SUPPLY VOLTAGE REJECTION RATIO—The ratio of the change in input offset voltage to the change in supply voltage producing it.

ELECTRICAL CHARACTERISTICS (V_S = ±15V, T_A = 25°C unless otherwise specified)

PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
Input Offset Voltage		2.0	7.5	mV	$R_S \leq 10K$, $\pm 9V \leq V_S \leq \pm 15V$
Input Offset Current		100	500	nA	
Input Bias Current		0.3	1.5	μA	
Input Resistance	50	250		KΩ	
Output Resistance		150		Ω	
Large-Signal Voltage Gain	15,000	45,000			$R_L \geq 2K$, $V_{OUT} = \pm 10V$
Output Voltage Swing	±12 ±10	±14 ±13		V V	$R_L \geq 10K$ $R_L \geq 2K$
Input Voltage Range	±8.0	±10		V	
Common Mode Rejection Ratio	65	90		db	$R_S \leq 10K$
Supply Voltage Rejection Ratio		25	200	μV/V	$R_S \leq 10K$
Power Consumption		80	200	mW	
Transient Response Risetime Overshoot		 0.3 10	 1.0 30	 μs %	$V_{in} = 20mV$, $R_L = 2K\Omega$, $C_1 = 5000$ pF, $R_1 = 1.5$ KΩ, $C_2 = 200$pF, $R_2 = 50\Omega$ $C_L \leq 100$pF

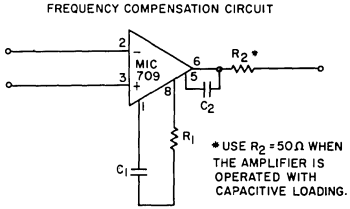
The following specifications apply for $0°C \leq T_A \leq +70°C$

Input Offset Voltage			10	mV	$R_S \leq 10K$, $\pm 9V \leq V_S \leq \pm 15V$
Input Offset Current			750	nA	
Input Bias Current			2.0	μA	
Large-Signal Voltage Gain	12,000				$R_L \geq 2K$, $V_{OUT} = \pm 10V$
Input Resistance	35			kΩ	



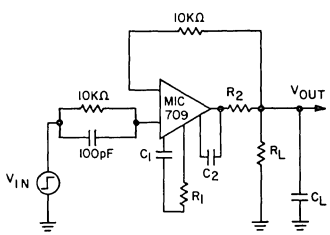
CIRCUIT DIAGRAM

FREQUENCY COMPENSATION CIRCUIT

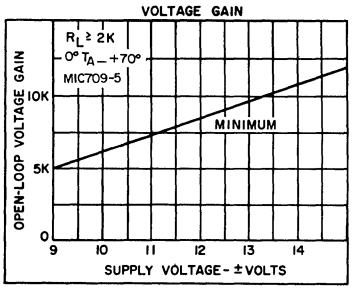


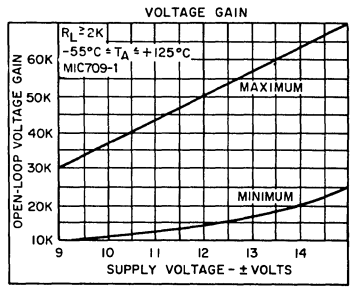
*USE $R_2 = 50\Omega$ WHEN THE AMPLIFIER IS OPERATED WITH CAPACITIVE LOADING.

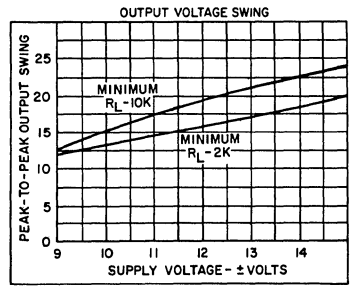
TRANSIENT RESPONSE TEST CIRCUIT



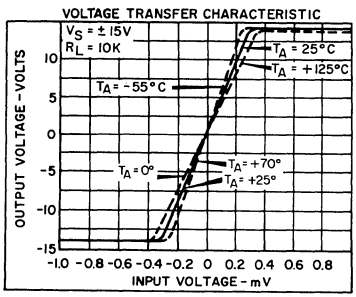
GUARANTEED ELECTRICAL CHARACTERISTICS

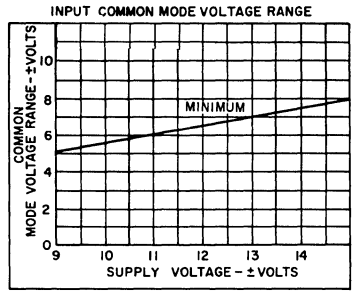


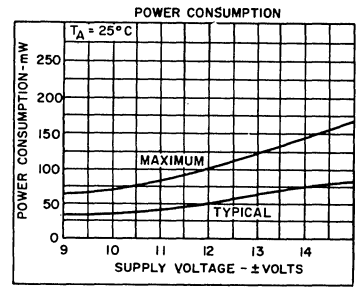


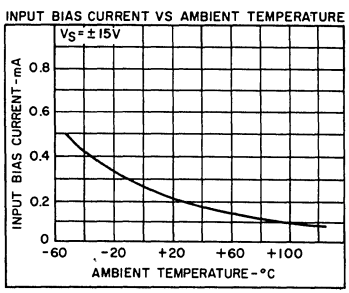


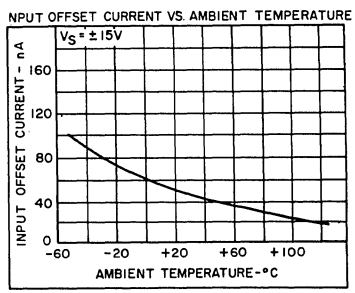
TYPICAL PERFORMANCE CURVES

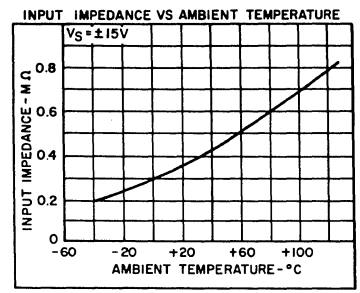






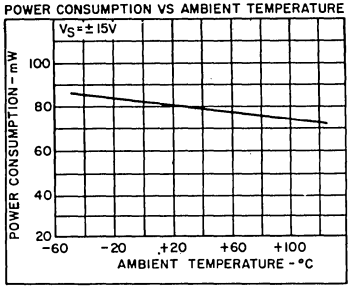




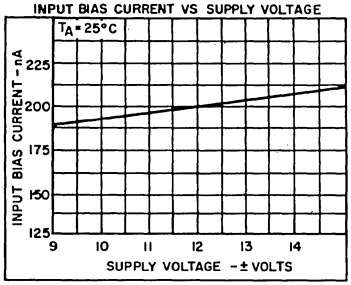


TYPICAL PERFORMANCE CURVES, continued

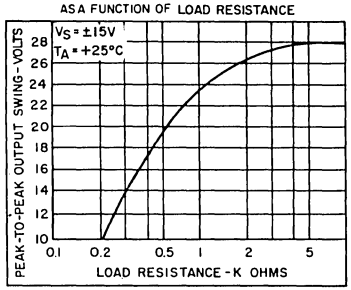
POWER CONSUMPTION VS AMBIENT TEMPERATURE



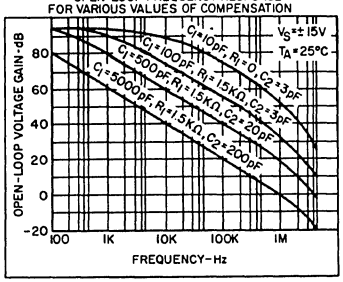
INPUT BIAS CURRENT VS SUPPLY VOLTAGE



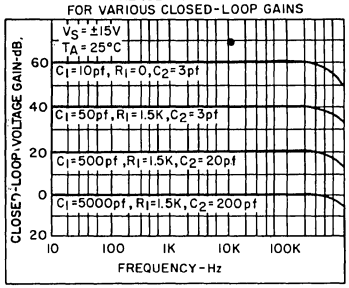
OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE



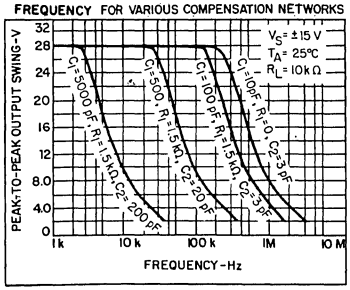
OPEN-LOOP FREQUENCY RESPONSE FOR VARIOUS VALUES OF COMPENSATION



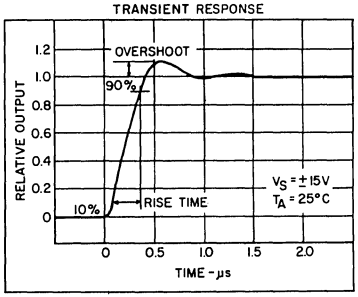
FREQUENCY RESPONSE FOR VARIOUS CLOSED-LOOP GAINS



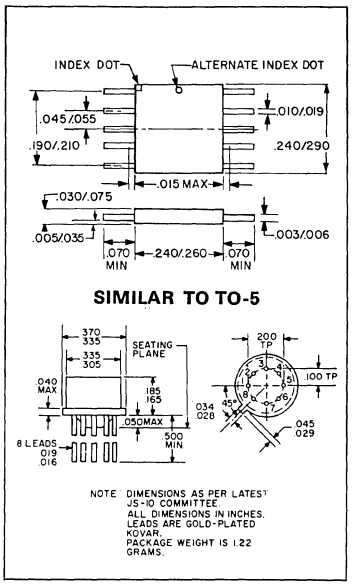
OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY FOR VARIOUS COMPENSATION NETWORKS



TRANSIENT RESPONSE



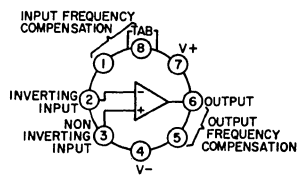
HIGH SPEED DIFFERENTIAL COMPARATOR



- **Low Offset Voltage**
- **Low Offset Current**
- **High Voltage Gain**
- **Fast Response Time**

The ITT MIC 710 is a differential voltage comparator which offers high accuracy and fast response times. The entire circuit is contained on one silicon chip and is manufactured using the ITT Planar Epitaxial process. The output of the MIC 710 is compatible with all integrated logic forms. The MIC 710 can also be used as a variable threshold Schmidt trigger, a pulse height discriminator, a memory sense amplifier, a high noise immunity line receiver, or in high speed A-D conversion and multivibrator functions.

CONNECTION DIAGRAM
(Top View)

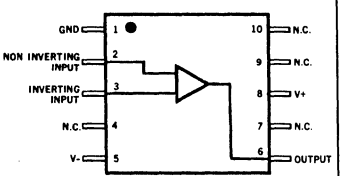


NOTE: PIN 4 CONNECTED TO CASE.

ABSOLUTE MAXIMUM RATINGS

CHARACTERISTICS	UNITS
Positive Supply Voltage	+14.0 V
Negative Supply Voltage	−7.0 V
Peak Output Current	10 mA
Differential Input Voltage	±5.0 V
Input Voltage	±7.0 V
Internal Power Dissipation (MIC710-1 Note 1, MIC710-5 Note 2)	300 mW
Operating Temperature Range MIC710-1	−55° to +125°C
MIC710-5	0° to +70°C
Storage Temperature Range	−65° to +150°C
Lead Temperature (Soldering, 60 sec.)	300°C

CONNECTION DIAGRAM
(Top View)



FLAT PACK

ELECTRICAL CHARACTERISTICS for 710-5 (TA = 25°C, V = 12.0V, V = −6.0V unless otherwise specified)

PARAMETER (see definitions)	MIN.	TYP.	MAX.	UNITS	CONDITIONS (Note 5)
Input Offset Voltage		1.6	5.0	mV	$R_S \leqslant 200\Omega$
Input Offset Current		1.8	5.0	uA	
Input Bias Current		16	25	uA	
Voltage Gain	1000	1500			
Output Resistance		200		Ω	
Output Sink Current	1.6	2.5		mA	$\Delta V_{in} \geqslant 5mV$, $V_{out} = 0$
Response Time (Note 3)		40		ns	
The following specifications apply for 0°C ≤TA ≤+70°C:					
Input Offset Voltage			6.5	mV	$R_S \leqslant 200\Omega$
Average Temperature Coefficient of Input Offset Voltage		5.0	20	uV/°C	$R_S = 50\Omega$, TA = 0°C to TA = +70°C
Input Offset Current			7.5	uA	
Average Temperature Coefficient of Input Offset Current		15	50	nA/°C	TA = 25°C to TA = +70°C
		24	100	nA/°C	TA = 25°C to TA = 0°C
Input Bias Current		25	40	uA	TA = 0°C
Input Voltage Range	±5.0			V	V = −7.0V
Common Mode Rejection Ratio	70	98		dB	$R_S \leqslant 200$
Differential Input Voltage Range	±5.0			V	
Voltage Gain	800				
Positive Output Level	2.5	3.2	4.0	V	$\Delta V_{in} \geqslant 5mV$, $0 \leqslant I_{out} \leqslant 5.0mA$
Negative Output Level	−1.0	−0.5	0	V	$\Delta V_{in} \geqslant 5mV$
Output Sink Current	0.5			mA	$\Delta V_{in} \geqslant 5mV$, $V_{out} = 0$
Positive Supply Current		5.2	9.0	mA	$V_{out} \leqslant 0$
Negative Supply Current		4.6	7.0	mA	
Power Consumption		90	150	mW	

DEFINITION OF TERMS:

LOGIC THRESHOLD VOLTAGE — The approximate voltage at the output of the comparator at which the loading logic circuitry changes its digital state.

INPUT OFFSET VOLTAGE* — The voltage between the input terminals when the output is at the logic threshold voltage. The input offset voltage may also be defined for the case where two equal resistances are inserted in series with the input leads.

INPUT OFFSET CURRENT* — The difference in the currents into the two input terminals with the output at the logic threshold voltage.

INPUT BIAS CURRENT* — The average of the two input currents.

INPUT VOLTAGE RANGE* — The range of voltage on the input terminals for which the comparator will operate within specifications.

DIFFERENTIAL INPUT VOLTAGE RANGE* — The range of voltage between the input terminals for which operation within specifications is assured.

VOLTAGE GAIN* — The ratio of the change in output voltage to the change in voltage between the input terminals producing it with the DC output level in the vicinity of the logic threshold voltage.

RESPONSE TIME* — The interval between the application of an input step function and the time when the output crosses the logic threshold voltage. The input step drives the comparator from some initial, saturated input voltage to an input level just barely in excess of that required to bring the output from saturation to the logic threshold voltage. This excess is referred to as the voltage overdrive.

STROBE RELEASE TIME* — The time required for the output to rise to the logic threshold voltage after the strobe terminal has been driven from the zero to the one logic level. Appropriate input conditions are assumed.

POSITIVE OUTPUT LEVEL* — The DC output voltage in the positive direction with the input voltage equal to or greater than a minimum specified amount.

NEGATIVE OUTPUT LEVEL* — The DC output voltage in the negative direction with the input voltage equal to or greater than a minimum specified amount.

OUTPUT SINK CURRENT — The maximum negative current that can be delivered by the comparator.

PEAK OUTPUT CURRENT — The maximum current that may flow into the output load without causing damage to the comparator.

OUTPUT RESISTANCE* — The resistance seen looking into the output terminal with the DC output level at the logic threshold voltage.

STROBED OUTPUT LEVEL* — The DC output voltage, independent of input voltage with the voltage on the strobe terminal equal to or less than a minimum specified amount.

STROBE CURRENT — The maximum current drawn by the strobe terminal when it is at the zero logic level.

POWER CONSUMPTION — The DC power into the amplifier with no output load. The DC power will vary with signal level, but is specified as a maximum for the entire range of input-signal conditions.

*These definitions apply for either side with the other disabled with the strobe.

ELECTRICAL CHARACTERISTICS for 710-1 ($T_A = +25°C$, $V = 12.0V$, $V = -6.0V$ unless otherwise specified)

PARAMETER (see definitions)	MIN.	TYP.	MAX.	UNITS	CONDITIONS (Note 4)
Input Offset Voltage		0.6	2.0	mV	$R_S \leq 200\Omega$
Input Offset Current		0.75	3.0	uA	
Input Bias Current		13	20	uA	
Voltage Gain	1250	1700			
Output Resistance		200		Ω	
Output Sink Current	2.0	2.5		mA	$\Delta V_{in} \geq 5mV$, $V_{out} = 0$
Response Time (Note 3)		40		ns	
The following specifications apply for $-55°C \leq T_A \leq +125°C$:					
Input Offset Voltage			3.0	mV	$R_S \leq 200\Omega$
Average Temperature Coefficient of Input Offset Voltage		3.5	10	uV/°C	$R_S = 50\Omega$, $T_A = 25°C$ to $T_A = +125°C$
		2.7	10	uV/°C	$R_S 50\Omega$, $T_A = 25°C$ to $T_A = -55°C$
Input Offset Current		0.25	3.0	uA	$T_A = +125°C$
		1.8	7.0	uA	$T_A = -55°C$
Average Temperature Coefficient of Input Offset Current		5.0	25	nA/°C	$T_A = 25°C$ to $T_A = +125°C$
		15	75	nA/°C	$T_A = 25°C$ to $T_A = -55°C$
Input Bias Current		27	45	uA	$T_A = -55°C$
Input Voltage Range	±5.0			V	$V = -7.0V$
Common Mode Rejection Ratio	80	100		dB	$R_S \leq 200\Omega$
Differential Input Voltage Range	±5.0			V	
Voltage Gain	1000				
Positive Output Level	2.5	3.2	4.0	V	$V_{in} \geq 5mV$, $0 \leq I_{out} \leq 5.0mA$
Negative Output Level	−1.0	−0.5	0	V	$\Delta V_{in} \geq 5mV$
Output Sink Current	0.5	1.7		mA	$T_A = +125°C$, $\Delta V_{in} \geq 5mV$, $V_{out} = 0$
	1.0	2.3		mA	$T_A = -55°C$, $\Delta V_{in} \geq 5mV$, $V_{out} = 0$
Positive Supply Current		5.2	9.0	mA	$V_{out} \leq 0$
Negative Supply Current		4.6	7.0	mA	
Power Consumption		90	150	mW	

NOTES:

(1) Rating applies for case temperatures to +125°C; derate linearly at 5.6mW/°C for ambient temperatures above +105°C.

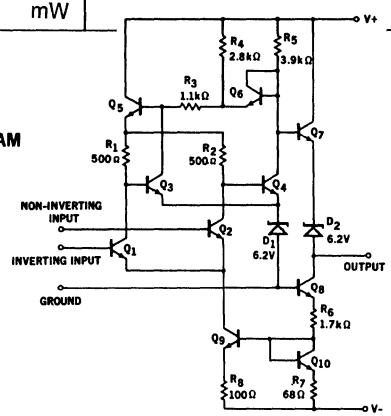
(2) Ratings apply for ambient temperatures to +70°C.

(3) The response time specified (see definitions) is for a 100-mV input step with 5-mV overdrive.

(4) The input offset voltage and input offset current (see definitions) are specified for a logic threshold voltage of 1.8V at −55°C, 1.4V at +25°C and 1.0V at +125°C.

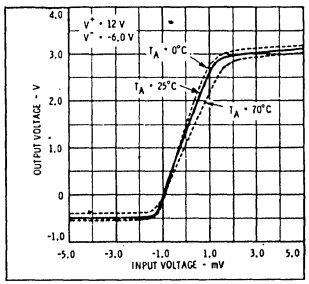
(5) The input offset voltage and input offset current (see definitions) are specified for a logic threshold voltage of 1.5V at 0°C, 1.4V at +25°C and 1.2V at +70°C.

SCHEMATIC DIAGRAM

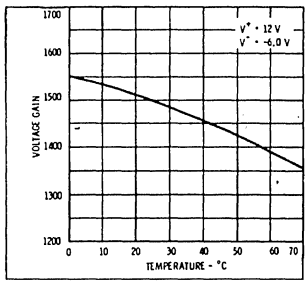


TYPICAL CHARACTERISTICS MIC 710-5 (TA = 25°C, V = 12.0V, V = −6.0V unless otherwise specified)

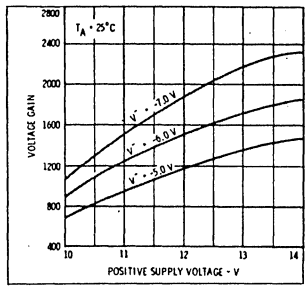
VOLTAGE TRANSFER CHARACTERISTIC



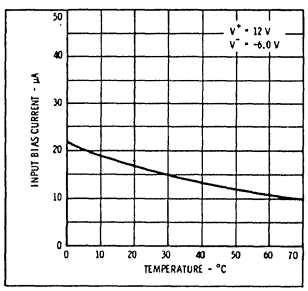
VOLTAGE GAIN AS A FUNCTION OF AMBIENT TEMPERATURE



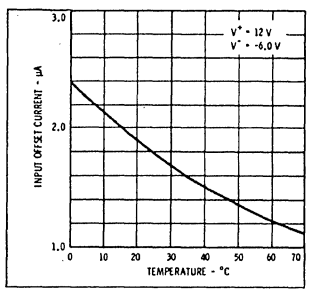
VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGES



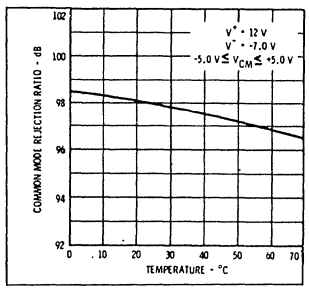
INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



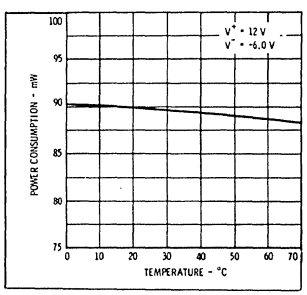
INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



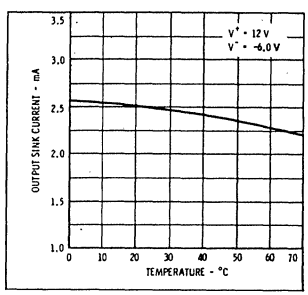
COMMON MODE REJECTION RATIO AS A FUNCTION OF AMBIENT TEMPERATURE



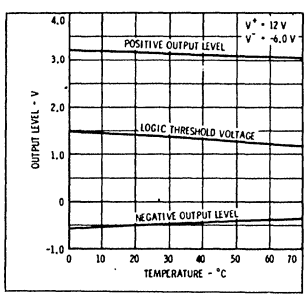
POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE



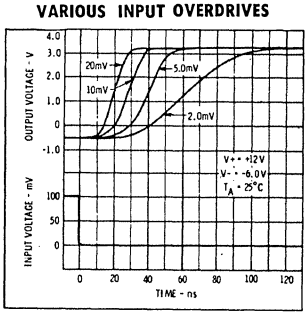
OUTPUT SINK CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



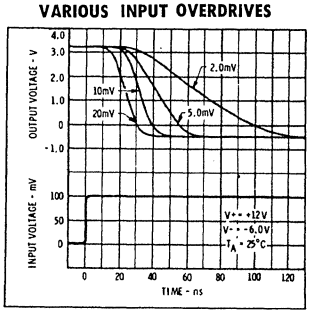
OUTPUT VOLTAGE LEVELS AS A FUNCTION OF AMBIENT TEMPERATURE



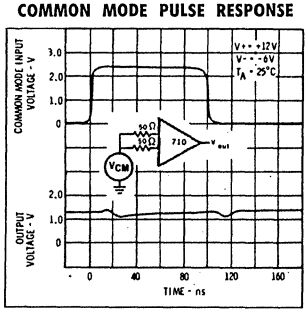
RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



COMMON MODE PULSE RESPONSE

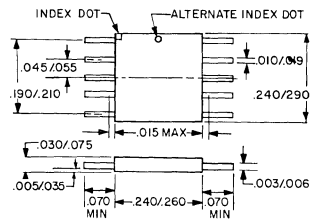


DUAL COMPARATOR

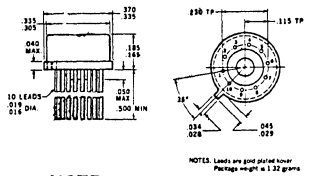
- **High Accuracy**
- **Fast Response Time**
- **Large Input Voltage Range**
- **Low Power Consumption**

The MIC 711 is a dual differential voltage comparator. It was primarily designed for core-memory sense amplifiers which require high accuracy, fast response times, large input voltage range, and low power consumption. The output voltage is compatible with most integrated logic forms. When used as a sense amplifier, the threshold voltage can be adjusted over a wide range, almost independent of the integrated circuit characteristics. Each comparator channel is provided with independent strobing. Pulse stretching on the output is easily accomplished. Double-ended detection for automatic GO/NO-GO test equipment and pulse height detection (window discriminator) are additional applications of the dual comparator. The entire circuit is contained on a silicon chip and is manufactured using ITT Planar Epitaxial process.

PHYSICAL DIMENSIONS
FLAT PACKAGE (TOP VIEW)

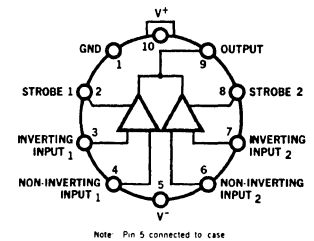


SIMILAR TO TO-5



NOTE:
All dimensions in inches

TO-5 CONNECTION DIAGRAM
(Top View)



Note: Pin 5 connected to case

ABSOLUTE MAXIMUM RATINGS

CHARACTERISTICS	UNITS
Positive Supply Voltage	+14.0 V
Negative Supply Voltage	−7.0 V
Peak Output Current	50 mA
Differential Input Voltage	±5.0 V
Input Voltage	±7.0 V
Strobe Voltage	0 to +6.0 V
Internal Power Dissipation (MIC711-1 Note 1, MIC711-5 Note 2)	300 mW
Operating Temperature Range MIC711-1	−55° to +125°C
MIC711-5	0° to +50°C
Storage Temperature Range	−65° to +150°C
Lead Temperature (Soldering, 60 sec.)	300°C

NOTES: (1) Rating applies for case temperatures to +125°C; derate linearly at 5.6mW/°C for ambient temperatures above +95°C.
(2) Rating applies for ambient temperatures to +70°C.

ELECTRICAL CHARACTERISTICS FOR 711-1 ($T_A = 25°C$, $V^+ = 12.0V$, $V^- = -6.0V$ unless otherwise specified)

PARAMETER (see definitions)	MIN.	TYP.	MAX.	UNITS	CONDITIONS
Input Offset Voltage		1.0 1.0	3.5 5.0	mV mV	$V_{out} = +1.4V, R_S \leq 200\Omega, V_{CM} = 0$ $V_{out} = +1.4V$, $R_S \leq 200\Omega$,
Input Offset Current		0.5	10.0	uA	$V_{out} = +1.4V$
Input Bias Current		25	75	uA	
Voltage Gain	750	1500			
Response Time (Note 3)		40		ns	
Strobe Release Time		12		ns	
Input Voltage Range	±5.0			V	$V^- = -7.0V$
Differential Input Voltage Range	±5.0			V	
Output Resistance		200		Ω	
Positive Output Level		4.5	5.0	V	$V_{in} \geq 10mV$
Loaded Positive Output Level	2.5	3.5		V	$V_{in} \geq 10mV$, $I_O = 5mA$
Negative Output Level	−1.0	−0.5	0	V	$V_{in} \geq 10mV$
Strobed Output Level	−1.0		0	V	$V_{strobe} \leq 0.3V$
Output Sink Current	0.5	0.8		mA	$V_{in} \geq 10mV$, $V_{out} \geq O$
Strobe Current		1.2	2.5	mA	$V_{strobe} = 100mV$
Positive Supply Current		8.6		mA	$V_{out} \leq 0$
Negative Supply Current		3.9		mA	
Power Consumption		130	200	mW	
The following specifications apply for $-55°C \leq T \leq 125°C$:					
Input Offset Voltage (Note 4)			4.5 6.0	mV mV	$R_S \leq 200\Omega$, $V_{CM} = 0$ $R_S \leq 200\Omega$
Input Offset Current (Note 4)			20	uA	
Input Bias Current			150	uA	
Temperature Coefficient of Input Offset Voltage		5.0		uV/°C	
Voltage Gain	500				

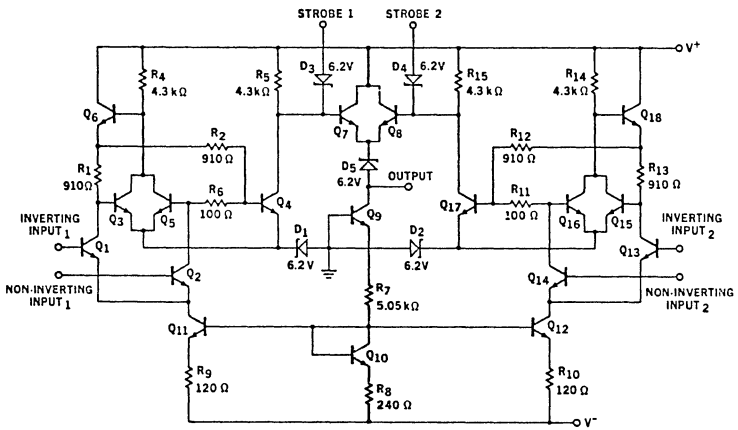
NOTES:

(3) The response time specified (see definitions) is for a 100-mV input step with 5-mV overdrive.

(4) The input offset voltage (see definitions) is specified for a logic threshold voltage of 1.8V at −55°C, 1.4V at +25°C and 1.0V at +125°C.

(5) The input offset voltage is specified for a logic threshold voltage of 1.5V at 0°C, 1.4V at +25°C and 1.2V at +70°C.

SCHEMATIC DIAGRAM



ELECTRICAL CHARACTERISTICS FOR 711-5 ($T_A = 25°C$, $V^+ = 12.0V$, $V^- = -6.0V$ unless otherwise specified)

PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
Input Offset Voltage		1.0 1.0	5.0 7.5	mV mV	$V_{out} = +1.4V, R_S \leq 200\Omega, V_{CM} = 0$ $V_{out} = +1.4V$, $R_S \leq 200\Omega$,
Input Offset Current		0.5	15	uA	$V_{out} = +1.4V$
Input Bias Current		25	100	uA	
Voltage Gain	700	1500			
Response Time (Note 3)		40		ns	
Strobe Release Time		12		ns	
Input Voltage Range	±5.0			V	$V^- = -7.0V$
Differential Input Voltage Range	±5.0			V	
Output Resistance		200		Ω	
Positive Output Level		4.5	5.0	V	$V_{in} \geq 10mV$
Loaded Positive Output Level	2.5	3.5		V	$V_{in} \geq 10mV$, $I_O = 5mA$
Negative Output Level	−1.0	−0.5	0	V	$V_{in} \geq 10mV$
Strobed Output Level	−1.0		0	V	$V_{strobe} \leq 0.3V$
Output Sink Current	0.5	0.8		mA	$V_{in} \geq 10mV$, $V_{out} \geq 0$
Strobe Current		1.2	2.5	mA	$V_{strobe} = 100mV$
Positive Supply Current		8.6		mA	$V_{out} \leq 0$
Negative Supply Current		3.9		mA	
Power Consumption		130	230	mW	
The following specifications apply for $0°C \leq T \leq +70°C$:					
Input Offset Voltage (Note 5)			6.0 10	mV mV	$R_S \leq 200\Omega$, $V_{CM} = 0$ $R_S \leq 200\Omega$
Input Offset Current (Note 5)			25	uA	
Input Bias Current			150	uA	
Temperature Coefficient of Input Offset Voltage		5.0		uV/°C	
Voltage Gain	500				

DEFINITION OF TERMS:

LOGIC THRESHOLD VOLTAGE — The approximate voltage at the output of the comparator at which the loading logic circuitry changes its digital state.

INPUT OFFSET VOLTAGE* — The voltage between the input terminals when the output is at the logic threshold voltage. The input offset voltage may also be defined for the case where two equal resistances are inserted in series with the input leads.

INPUT OFFSET CURRENT* — The difference in the currents into the two input terminals with the output at the logic threshold voltage.

INPUT BIAS CURRENT* — The average of the two input currents.

INPUT VOLTAGE RANGE* — The range of voltage on the input terminals for which the comparator will operate within specifications.

DIFFERENTIAL INPUT VOLTAGE RANGE* — The range of voltage between the input terminals for which operation within specifications is assured.

VOLTAGE GAIN* — The ratio of the change in output voltage to the change in voltage between the input terminals producing it with the DC output level in the vicinity of the logic threshold voltage.

RESPONSE TIME* — The interval between the application of an input step function and the time when the output crosses the logic threshold voltage. The input step drives the comparator from some initial, saturated input voltage to an input level just barely in excess of that required to bring the output from saturation to the logic threshold voltage. This excess is referred to as the voltage overdrive.

STROBE RELEASE TIME* — The time required for the output to rise to the logic threshold voltage after the strobe terminal has been driven from the zero to the one logic level. Appropriate input conditions are assumed.

POSITIVE OUTPUT LEVEL* — The DC output voltage in the positive direction with the input voltage equal to or greater than a minimum specified amount.

NEGATIVE OUTPUT LEVEL* — The DC output voltage in the negative direction with the input voltage equal to or greater than a minimum specified amount.

OUTPUT SINK CURRENT — The maximum negative current that can be delivered by the comparator.

PEAK OUTPUT CURRENT — The maximum current that may flow into the output load without causing damage to the comparator.

OUTPUT RESISTANCE* — The resistance seen looking into the output terminal with the DC output level at the logic threshold voltage.

STROBED OUTPUT LEVEL* — The DC output voltage, independent of input voltage, with the voltage on the strobe terminal equal to or less than a minimum specified amount.

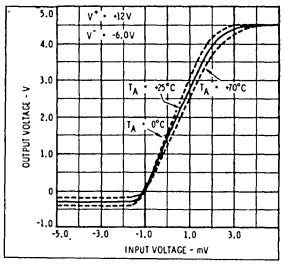
STROBE CURRENT — The maximum current drawn by the strobe terminal when it is at the zero logic level.

POWER CONSUMPTION — The DC power into the amplifier with no output load. The DC power will vary with signal level, but is specified as a maximum for the entire range of input-signal conditions.

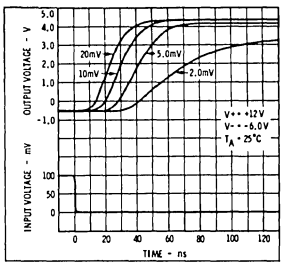
*These definitions apply for either side with the other disabled with the strobe.

TYPICAL PERFORMANCE CURVES MIC 711-5

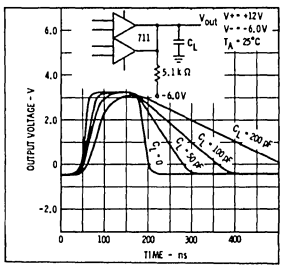
VOLTAGE TRANSFER CHARACTERISTIC



RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES

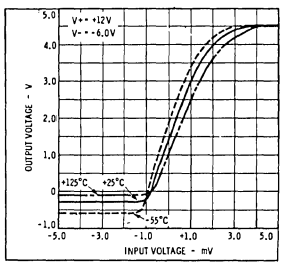


OUTPUT PULSE STRETCHING WITH CAPACITIVE LOADING

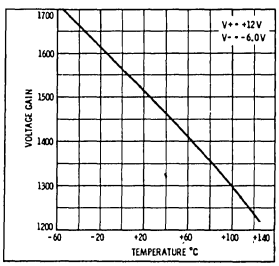


TYPICAL PERFORMANCE CURVES MIC 711-1

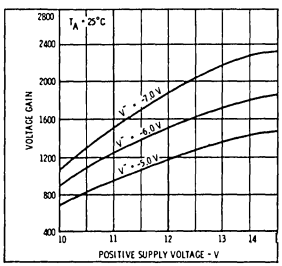
VOLTAGE TRANSFER CHARACTERISTIC



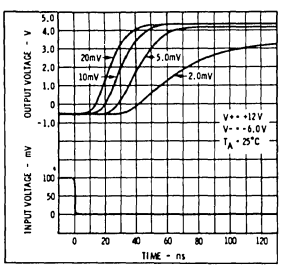
VOLTAGE GAIN AS A FUNCTION OF AMBIENT TEMPERATURE



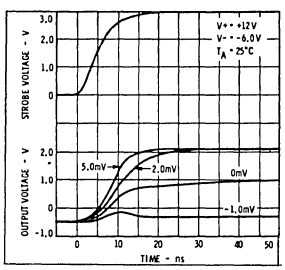
VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGES



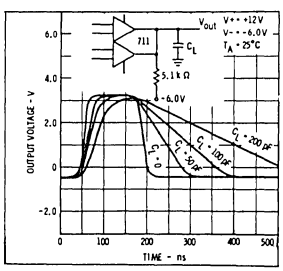
RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



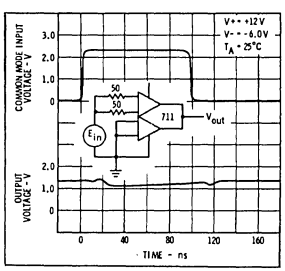
STROBE RELEASE TIME FOR VARIOUS INPUT OVERDRIVES



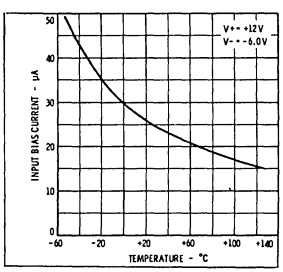
OUTPUT PULSE STRETCHING WITH CAPACITANCE LOADING



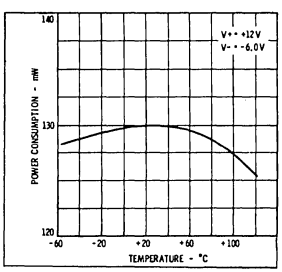
COMMON MODE PULSE RESPONSE



INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



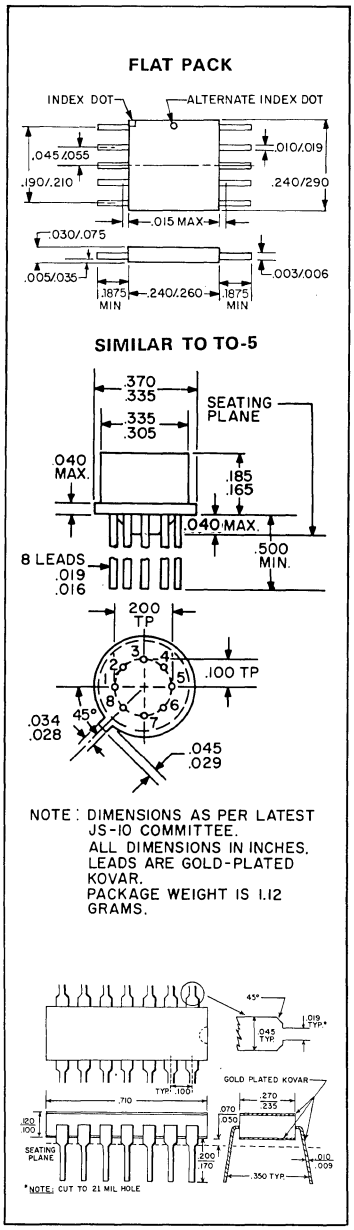
POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE



HIGH-GAIN WIDEBAND DC AMPLIFIER

- **Low Offset Voltage**
- **High Voltage Gain**
- **Low Offset Voltage Drift**

The MIC 712 is a general purpose amplifier for use as an operational amplifier in high speed analog computers, a precision instrumentation amplifier or in other applications requiring a feedback amplifier capable of operating within the frequency ranges of DC to as high as 30MHz. The MIC 712 amplifier achieves low DC offset and low thermal drift, wideband operation and low power consumption as a result of ITT Planar epitaxial manufacturing process.



ABSOLUTE MAXIMUM RATINGS

CHARACTERISTICS		UNITS
Voltage between V^+ and V^- terminals	±21	Volts
Internal Power Dissipation (TO-5) (MIC 712-1 note 1, MIC 712-5 note 2)	300	mW
Differential Input Voltage	±5.0	Volts
Input Voltage	+1.5 to −6.0	Volts
Peak Output Voltage	50	mA
Storage Temperature Range	−65 to +150	°C
Operating Temperature Range		
MIC 712-1	−55 to +125	°C
MIC 712-5	0 to +70	°C
Lead Temperature (Soldering, 60 sec.)	300	°C

NOTES: (1) Rating applies for case temperatures to +125°C; derate linearly at 5.6mW/°C for ambient temperatures above +95°C.
(2) Rating applies for ambient temperatures to +70°C.

ELECTRICAL CHARACTERISTICS for MIC 712-1

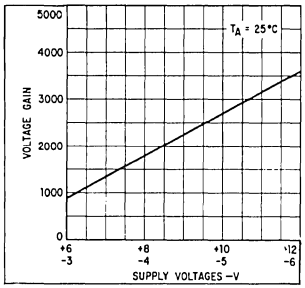
PARAMETER (See definitions)	MIN.	TYPE	MAX.	MIN.	TYPE	MAX	UNITS	CONDITIONS
	V+ = 12.0V, V− = 6.0V			V+ = 6.0V, V− = −3.0V				
Input Offset Voltage		0.5	2.0		0.7	3.0	mV	$R_s \leq 2k\Omega$
Input Offset Current		180	500		120	500	nA	
Input Bias Current		2.0	5.0		1.2	3.5	uA	
Input Resistance	16	40		22	67		kΩ	
Input Voltage Range	−4.0		+0.5	−1.5		+0.5	V	
Common Mode Rejection Ratio	80	100		80	100		dB	$R_s \leq 2k\Omega$, $f \leq 1kHz$
Large Signal Voltage Gain	2500	3600	6000					$R_L \geq 100k\Omega$, $V_{out} = \pm 5.0V$
				600	900	1500		R_L 100kΩ, $V_{out} = \pm 2.5V$
Output Resistance		200	500		300	700	Ω	
Supply Current		5.0	6.7		2.1	3.3	mA	$V_{out} = 0$
Power Consumption		90	120		19	30	mW	$V_{out} = 0$
Transient Response (Unity-Gain)								$C_l = 0.01$ uF, $R_l = 20\Omega$
								$R_L \geq 100k\Omega$, $V_{in} = 10mW$
Rise Time		25	120				ns	
Overshoot		10	50				%	$C_L \leq 100pF$
Transient Response (x100 gain)								$C_3 = 50pF$, $R_L \geq 100k\Omega$
								$V_{in} = 1$ mV
Risetime		10	30				ns	
Overshoot		20	40				%	
The following specifications apply for $-55°C \leq T_A \leq +125°C$:								
Input Offset Voltage			3.0			4.0	mV	$R_s \leq 2k\Omega$
Average Temperature Coefficient of Input		2.5	10		3.5	15	uV/°C	$R_s = 50\Omega$ $T_A = 25°C$ to $T_A = +125°C$
Offset Voltage								$R_s = 50\Omega$
		2.0	10		3.0	15	uV/°C	$T_A = 25°C$ to $T_A = -55°C$
Input Offset Current		80	500		50	500	nA	$T_A = +125°C$
		400	1500		280	1500	nA	$T_A = -55°C$
Average Temperature Coefficient of Input Offset Current		1.0	5.0		0.7	4.0	nA/°C	$T_A = 25°C$ to $T_A = +125°C$
		3.0	16		2.0	13	nA/°C	$T_A = 25°C$ to $T_A = -55°C$
Input Bias Current		4.3	10		2.6	7.5	uA	$T_A = -55°C$
Input Resistance	6.0			8.0			kΩ	
Common Mode Rejection Ratio	70	95		70	95		dB	$R_s \leq 2k\Omega$, $f \leq 1kHz$
Supply Voltage Rejection Ratio		75	200		75	200	uV/V	V+ = 12V, V− = −6Vto V+ = 6V, V− = −3V $R_s \leq 2k\Omega$
Large Signal Voltage Gain	2000		7000					$R_L \geq 100K\Omega$, $V_{out} = \pm 5.0V$
				500		1750		$R_L \geq 100k\Omega$, $V_{out} = \pm 2.5V$
Output Voltage Swing	±5.0	±5.3		±2.5	±2.7		V	$R_L \geq 100k\Omega$
	±3.5	±4.0		±1.5	±2.0		V	$R_L \geq 10k\Omega$
Supply Current		4.4	6.7		1.7	3.3	mA	$T_A = +125°C$, $V_{out} = 0$
		5.0	7.5		2.1	3.9	mA	$T_A = -55°C$, $V_{out} = 0$
Power Consumption		80	120		15	30	mW	$T_A = +125°C$, $V_{out} = 0$
		90	135		19	35	mW	$T_A = -55°C$, $V_{out} = 0$

ELECTRICAL CHARACTERISTICS for MIC 712-5

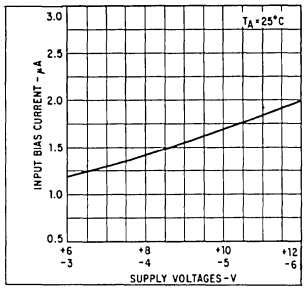
PARAMETER (see definitions)	V+ = 12.0V, V− = −6.0V MIN.	TYP.	MAX.	V+ = 6.0V, V− = −3.0V MIN.	TYP.	MAX.	UNITS	CONDITIONS
The following specifications apply for T_A = 25°C								
Input Offset Voltage		1.5	5.0		1.7	6.0	mV	$R_S \lesssim 2$ KΩ
Input Offset Current		0.5	2.0		0.3	2.0	μA	
Input Bias Current		2.5	7.5		1.5	5.0	μA	
Input Resistance	10	32		16	55		KΩ	
Input Voltage Range	−4.0		+0.5	−1.5		+0.5	V	
Common Mode Rejection Ratio	70	92		70	92		dB	$R_S \lesssim 2$KΩ, $f \lesssim 1$ KHz
Large Signal Voltage Gain	2000	3400	6000					$R_L \gtrsim 100$ KΩ $V_{out} = \pm 5.0$ V
				500	800	1500		$R_L \gtrsim 100$ KΩ $V_{out} = \pm 2.5$ V
Output Resistance		200	600		300	800	Ω	
Supply Current		5.0	6.7		2.1	3.3	mA	$V_{out} = 0$
Power Consumption		90	120		19	30	mW	$V_{out} = 0$
Transient Response (unity gain) Risetime		25	120				ns	$C_l = 0.01\mu F$, $R_l = 20\Omega$ $R_L \gtrsim 100$ KΩ $V_{in} = 10$ mV
Overshoot		10	50				%	$C_L \lesssim 100$ pF
Transient Response (X100 gain) Risetime		10	30				ns	$C_3 = 50$ pF $R_L \gtrsim 100$ KΩ $V_{in} = 1$ mV
Overshoot		20	40				%	
The following specifications apply for 0°C T_A +70°C								
Input Offset Voltage			6.5			7.5	mV	$R_S \lesssim 2$ KΩ
Average Temperature Coefficient of Input Offset Voltage		5.0	20		7.5	25	μV/°C	$R_S = 50\Omega$ $T_A = +70$°C to $T_A = 0$°C
Input Offset Current			2.5			2.5	μA	
Average Temperature Coefficient of Input Offset Current		4.0 6.0	10 20		3.0 5.5	8.0 18	nA/°C nA/°C	$T_A = 25$°C to $T_A = +70$°C $T_A = 25$°C to $T_A = 0$°C
Input Bias Current		4.0	12		2.7	8	μA	$T_A = 0$°C
Input Resistance	6.0	18		9.0	27		KΩ	
Common Mode Rejection Ratio	65	86		65	86		dB	$R_S \lesssim 2$ KΩ, $f \lesssim 1$ KHz
Supply Voltage Rejection Ratio		90	300		90	300	μV/V	V+ = 12V, V− = −6V to V+ = 6V, V− = −3V $R_S \lesssim 2$ KΩ
Large Signal Voltage Gain	1500		7000					$R_L \gtrsim 100$ KΩ $V_{out} = \pm 5.0$V
				400		1750		$R_L \gtrsim 100$KΩ $V_{out} = \pm 2.5$V
Output Voltage Swing	±5.0 ±3.5	±5.3 ±4.0		±2.5 ±1.5	±2.7 ±2.0		V V	$R_L \gtrsim 100$ KΩ $R_L \gtrsim 10$ KΩ
Supply Current		5.0	7.0		2.1	3.9	mA	$V_{out} = 0$
Power Consumption		90	125		19	35	mW	

TYPICAL PERFORMANCE CURVES MIC 712-1, 712-5

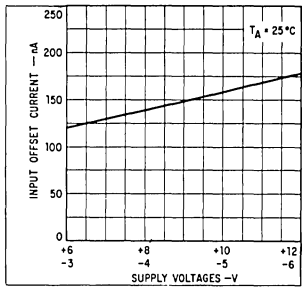
VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGES



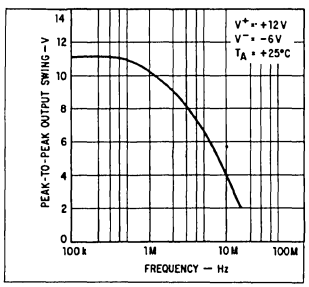
INPUT BIAS CURRENT AS A FUNCTION OF SUPPLY VOLTAGES



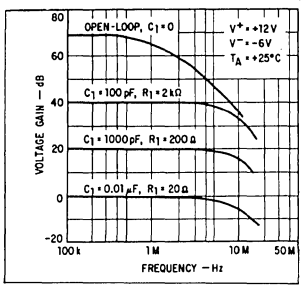
INPUT OFFSET CURRENT AS A FUNCTION OF SUPPLY VOLTAGES



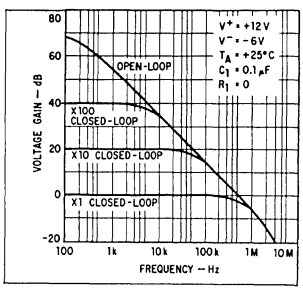
OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY WITH LEAD-LAG COMPENSATION



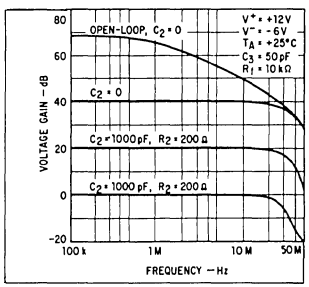
FREQUENCY RESPONSE FOR VARIOUS CLOSED-LOOP GAINS (LAG COMPENSATION)



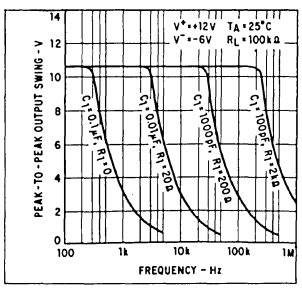
FREQUENCY RESPONSE WITH CONSERVATIVE COMPENSATION NETWORK



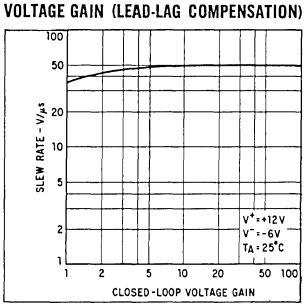
FREQUENCY RESPONSE FOR VARIOUS CLOSED-LOOP GAINS (LEAD-LAG COMPENSATION)



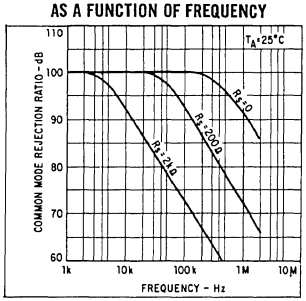
OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY FOR VARIOUS LAG COMPENSATION NETWORKS



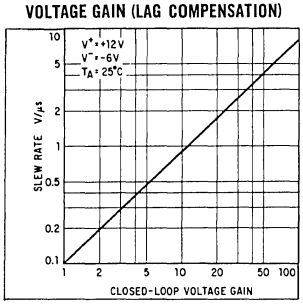
SLEW RATE AS A FUNCTION OF CLOSED-LOOP VOLTAGE GAIN (LEAD-LAG COMPENSATION)



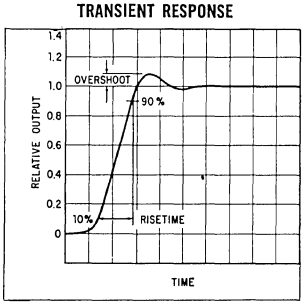
COMMON MODE REJECTION RATIO AS A FUNCTION OF FREQUENCY



SLEW RATE AS A FUNCTION OF CLOSED-LOOP VOLTAGE GAIN (LAG COMPENSATION)

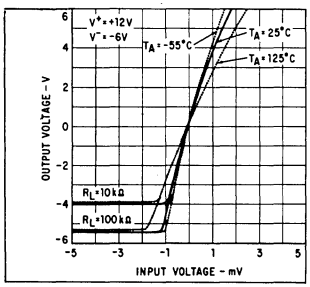


TRANSIENT RESPONSE

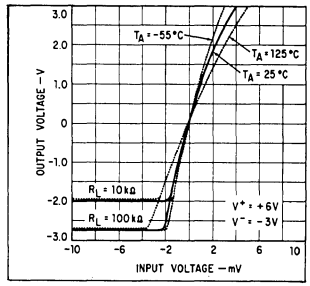


TYPICAL PERFORMANCE CURVES MIC 712-1

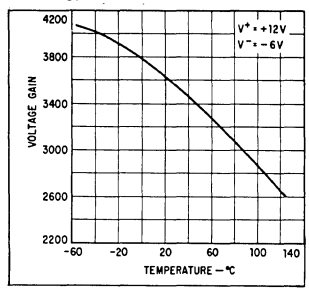
VOLTAGE TRANSFER CHARACTERISTIC



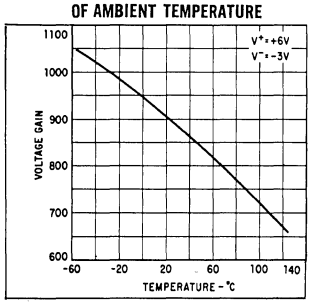
VOLTAGE TRANSFER CHARACTERISTIC



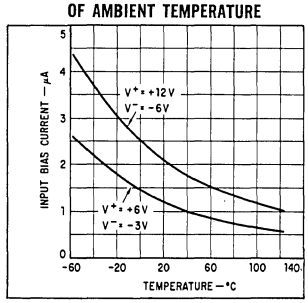
VOLTAGE GAIN AS A FUNCTION OF AMBIENT TEMPERATURE



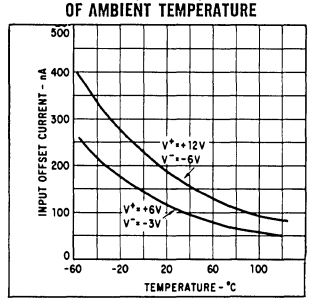
VOLTAGE GAIN AS A FUNCTION OF AMBIENT TEMPERATURE



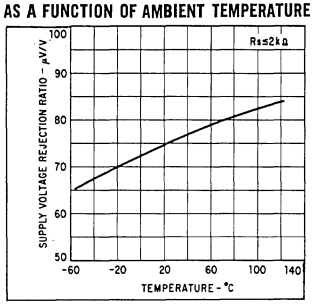
INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



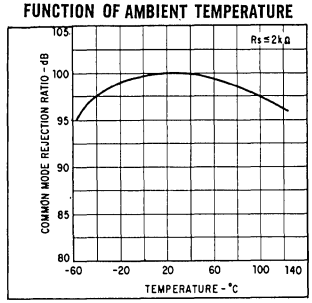
INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



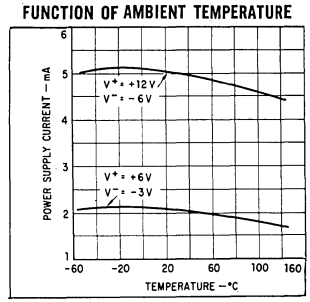
SUPPLY VOLTAGE REJECTION RATIO AS A FUNCTION OF AMBIENT TEMPERATURE



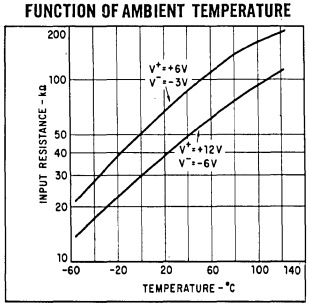
COMMON MODE REJECTION RATIO AS A FUNCTION OF AMBIENT TEMPERATURE



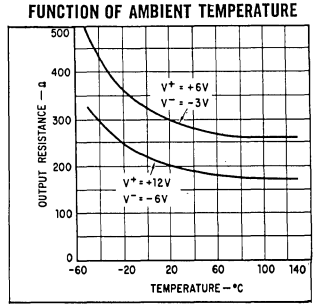
POWER SUPPLY CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



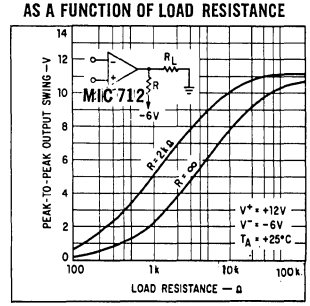
INPUT RESISTANCE AS A FUNCTION OF AMBIENT TEMPERATURE



OUTPUT RESISTANCE AS A FUNCTION OF AMBIENT TEMPERATURE

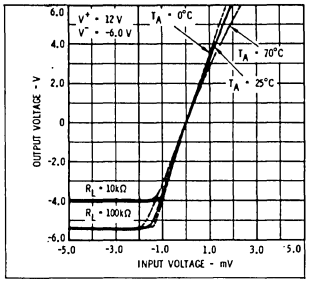


OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE

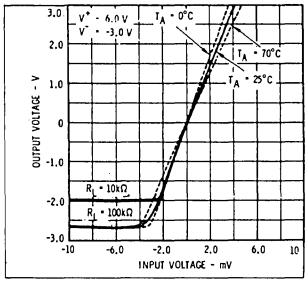


TYPICAL PERFORMANCE CURVES MIC 712-5

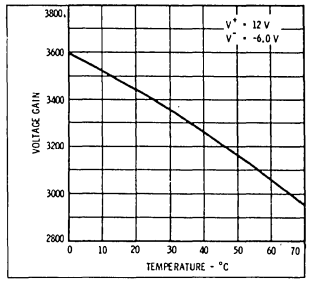
VOLTAGE TRANSFER CHARACTERISTIC



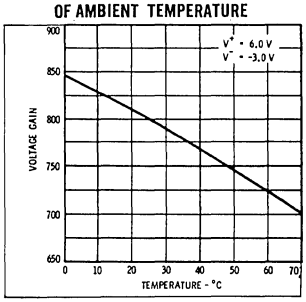
VOLTAGE TRANSFER CHARACTERISTIC



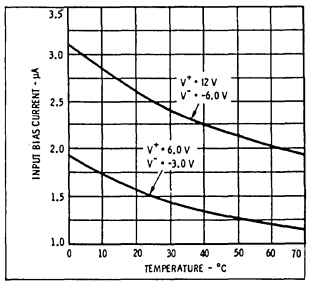
VOLTAGE GAIN AS A FUNCTION OF AMBIENT TEMPERATURE



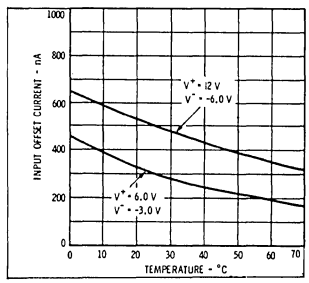
VOLTAGE GAIN AS A FUNCTION OF AMBIENT TEMPERATURE



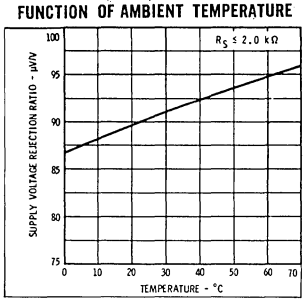
INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



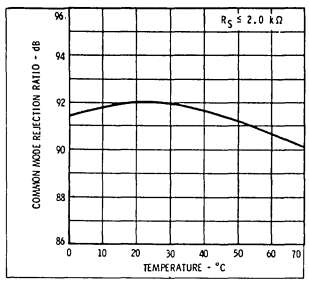
INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



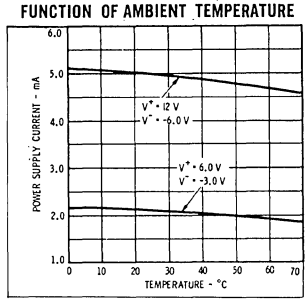
SUPPLY VOLTAGE REJECTION RATIO AS A FUNCTION OF AMBIENT TEMPERATURE



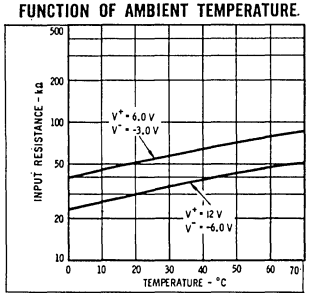
COMMON MODE REJECTION RATIO AS A FUNCTION OF AMBIENT TEMPERATURE



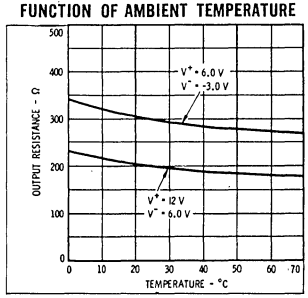
POWER SUPPLY CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



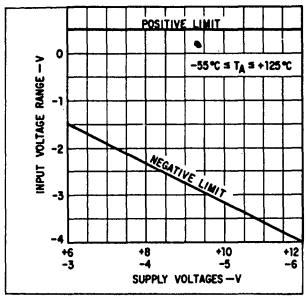
INPUT RESISTANCE AS A FUNCTION OF AMBIENT TEMPERATURE



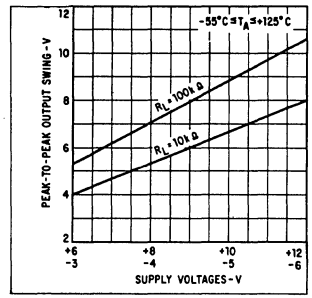
OUTPUT RESISTANCE AS A FUNCTION OF AMBIENT TEMPERATURE



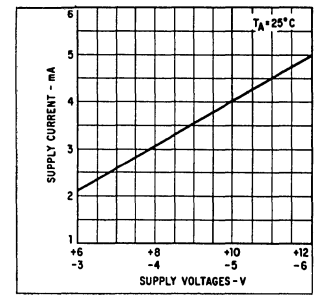
INPUT VOLTAGE RANGE AS A FUNCTION OF SUPPLY VOLTAGES



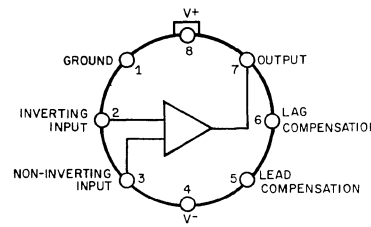
OUTPUT VOLTAGE SWING AS A FUNCTION OF SUPPLY VOLTAGES



SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGES

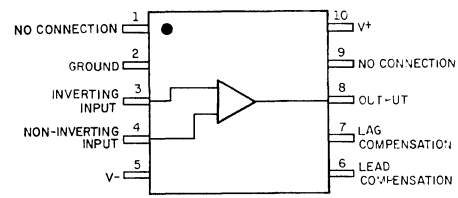


CONNECTION DIAGRAMS TO-5 (Top View)

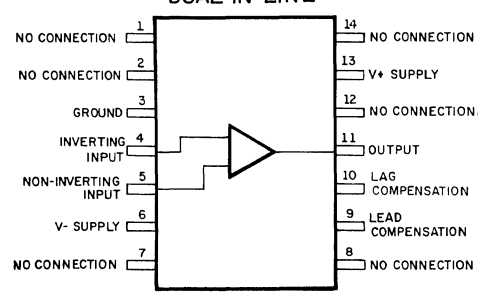


NOTE: PIN 4 CONNECTED TO CASE

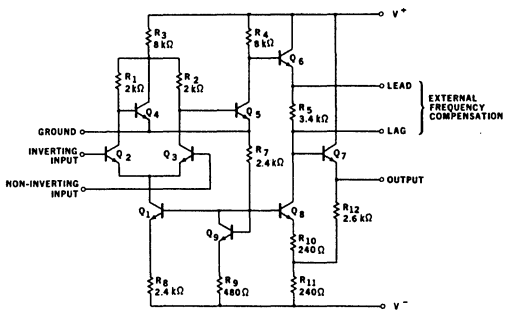
FLAT PACK (Top View)



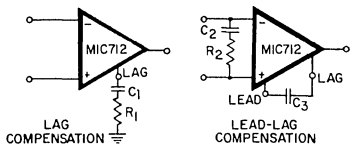
DUAL IN-LINE



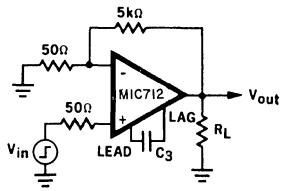
SCHEMATIC DIAGRAM



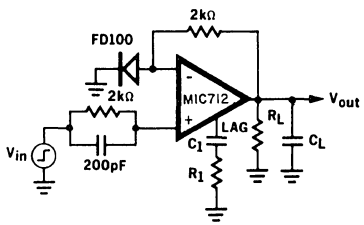
FREQUENCY COMPENSATION CIRCUITS



TRANSIENT RESPONSE TEST CIRCUITS



X100 AMPLIFIER (LEAD COMPENSATION)



UNITY-GAIN AMPLIFIER (LAG COMPENSATION)

SPECIAL ORDERING CODE

Temperature Range:
1 = −55° +125°C
5 = 0° to +70C

Package:
B = .250" X .250" Flat Pack
C = 8-lead TO-5
D = 14-Lead Dual-In-Line

Example:
MIC712-1C means operating temperature range of −55° to +125°C, supplied in a TO-5 package.

DEFINITION OF TERMS

INPUT OFFSET VOLTAGE — That voltage which must be applied between the input terminals to obtain zero output voltage. The input offset voltage may also be defined for the case where two equal resistances are inserted in series with the input leads.

INPUT OFFSET CURRENT — The difference in the currents into the two input terminals with the output at zero volts.

INPUT RESISTANCE — The resistance looking into either input terminal with the other grounded.

INPUT BIAS CURRENT — The average of the two input currents.

INPUT VOLTAGE RANGE — The range of voltage which, if exceeded on either input terminal, could cause the amplifier to cease functioning properly.

INPUT COMMON MODE REJECTION RATIO — The ratio of the input voltage range to the maximum change in input offset voltage over this range.

SUPPLY VOLTAGE REJECTION RATIO — The ratio of the change in input offset voltage to the change in supply voltage producing it.

LARGE-SIGNAL VOLTAGE GAIN — The ratio of the maximum output voltage swing with load to the change in input voltage required to drive the output from zero to this voltage.

OUTPUT VOLTAGE SWING — The peak output swing, referred to zero, that can be obtained without clipping.

OUTPUT RESISTANCE — The resistance seen looking into the output terminal with the output at null. This parameter is defined only under small signal conditions at frequencies above a few hundred cycles to eliminate the influence of drift and thermal feedback.

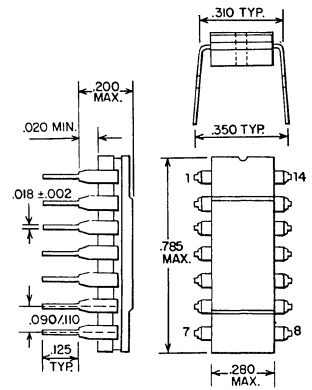
POWER CONSUMPTION — The DC power required to operate the amplifier with the output at zero and with no load current.

TRANSIENT RESPONSE — The closed-loop step-function response of the amplifier under small-signal conditions.

PEAK OUTPUT CURRENT — The maximum current that may flow in the output load without causing damage to the unit.

DUAL HIGH SPEED DIFFERENTIAL COMPARATOR

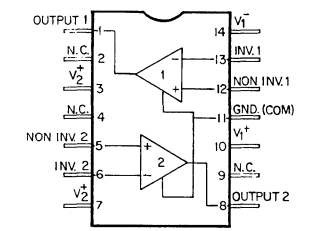
DUAL IN-LINE PACKAGE



- **Better Temperature Tracking**
- **Low Offset Voltage**
- **Low Offset Current**
- **High Voltage Gain**
- **Fast Response Time**

The ITT MIC720 differential voltage dual comparator, offering high accuracy and fast response times, consists of two separate MIC710 high speed differential comparators. The entire circuit is contained on one silicon chip and is manufactured using the ITT Planar Epitaxial process. The output of the MIC720 is compatible with all integrated logic forms. The MIC720 can also be used as a variable threshold Schmidt trigger, a pulse height discriminator, a memory sense amplifier, a high noise immunity line receiver, or in high speed A-D conversion and multivibrator functions.

CONNECTION DIAGRAM



ABSOLUTE MAXIMUM RATINGS

CHARACTERISTICS		UNITS
Positive Supply Voltage		+14.0 V
Negative Supply Voltage		−7.0 V
Peak Output Current		10 mA
Differential Input Voltage		±5.0 V
Input Voltage		±7.0 V
Internal Power Dissipation		300 mW
(MIC720-1 Note 1, MIC720-5 Note 2)		200 mW
Operating Temperature Range	MIC720-1	−55° to +125°C
	MIC720-5	0° to +70°C
Storage Temperature Range		−65° to +150°C
Lead Temperature (Soldering, 60 sec.)		300°C

ELECTRICAL CHARACTERISTICS for MIC 720-1 (T = +25°C, V = 12.0V, V = −6.0V unless otherwise specified)

PARAMETER (see definitions)	MIN.	TYP.	MAX.	UNITS	CONDITIONS (Note 4)
Input Offset Voltage		0.6	2.0	mV	Rs≦200Ω
Input Offset Current		0.75	3.0	uA	
Input Bias Current		13	20	uA	
Voltage Gain	1250	1700			
Output Resistance		200		Ω	
Output Sink Current	2.0	2.5		mA	$\Delta V_{in} \geqq 5mV$, $V_{out} = 0$
Response Time (Note 3)		40		ns	
The following specifications apply for −55°C ≦ T_A ≦ +125°C:					
Input Offset Voltage			3.0	mV	Rs≦200Ω
Average Temperature Coefficient of Input Offset Voltage		3.5	10	uV/°C	Rs = 50Ω, TA = 25°C to TA = +125°C
		2.7	10	uV/°C	Rs50Ω, TA = 25°C to TA = −55°C
Input Offset Current		0.25	3.0	uA	TA = +125°C
		1.8	7.0	uA	T_A = −55°C
Average Temperature Coefficient of Input Offset Current		5.0	25	nA/°C	T_A = 25°C to T_A = +125°C
		15	75	nA/°C	T_A = 25°C to T_A = −55°C
Input Bias Current		27	45	uA	T_A = −55°C
Input Voltage Range	±5.0			V	V = −7.0V
Common Mode Rejection Ratio	80	100		dB	Rs≦200Ω
Differential Input Voltage Range	±5.0			V	
Voltage Gain	1000				
Positive Output Level	2.5	3.2	4.0	V	$V_{in} \geqq 5mV$, $0 \leqq I_{out} \leqq 5.0mA$
Negative Output Level	−1.0	−0.5	0	V	$\Delta V_{in} \geqq 5mV$
Output Sink Current	0.5	1.7		mA	T_A = +125°C, $\Delta V_{in} \geqq 5mV$, $V_{out} = 0$
	1.0	2.3		mA	T_A = −55°C, $\Delta V_{in} \geqq 5mV$, $V_{out} = 0$
Positive Supply Current		5.2	9.0	mA	$V_{out} \leqq 0$
Negative Supply Current		4.6	7.0	mA	
Power Consumption		90	150	mW	

NOTES:

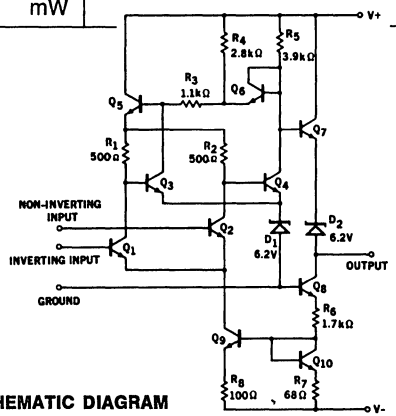
(1) For DIP pack derate at 4.4mW/°C for case temperatures above +115°C; derate linearly at 3.3mW/°C for ambient temperatures above +100°C.

(2) Ratings apply for ambient temperatures to +70°C.

(3) The response time specified (see definitions) is for a 100-mV input step with 5-mV overdrive.

(4) The input offset voltage and input offset current (see definitions) are specified for a logic threshold voltage of 1.8V at −55°C, 1.4V at +25°C and 1.0V at +125°C.

(5) The input offset voltage and input offset current (see definitions) are specified for a logic threshold voltage of 1.5V at 0°C, 1.4V at +25°C and 1.2V at +70°C.



½ CIRCUIT — SCHEMATIC DIAGRAM

ELECTRICAL CHARACTERISTICS for MIC 720-5 (TA = 25°C, V = 12.0V, V = −6.0V unless otherwise specified)

PARAMETER (see definitions)	MIN.	TYP.	MAX.	UNITS	CONDITIONS (Note 5)
Input Offset Voltage		1.6	5.0	mV	$R_S \lessapprox 200\Omega$
Input Offset Current		1.8	5.0	uA	
Input Bias Current		16	25	uA	
Voltage Gain	1000	1500			
Output Resistance		200		Ω	
Output Sink Current	1.6	2.5		mA	$\Delta V_{in} \gtrapprox 5mV$, $V_{out} = 0$
Response Time (Note 3)		40		ns	
The following specifications apply for $0°C \lessapprox TA \lessapprox +70°C$:					
Input Offset Voltage			6.5	mV	$R_S \lessapprox 200\Omega$
Average Temperature Coefficient of Input Offset Voltage		5.0	20	uV/°C	$R_S = 50\Omega$, TA = 0°C to TA = +70°C
Input Offset Current			7.5	uA	
Average Temperature Coefficient of Input Offset Current		15	50	nA/°C	TA = 25°C to TA = +70°C
		24	100	nA/°C	TA = 25°C to TA = 0°C
Input Bias Current		25	40	uA	TA = 0°C
Input Voltage Range	±5.0			V	$V^{\pm} = -7.0V$
Common Mode Rejection Ratio	70	98		dB	$R_S \lessapprox 200$
Differential Input Voltage Range	±5.0			V	
Voltage Gain	800				
Positive Output Level	2.5	3.2	4.0	V	$\Delta V_{in} \gtrapprox 5mV$, $0 \lessapprox I_{out} \lessapprox 5.0mA$
Negative Output Level	−1.0	−0.5	0	V	$\Delta V_{in} \gtrapprox 5mV$
Output Sink Current	0.5			mA	$\Delta V_{in} \gtrapprox 5mV$, $V_{out} = 0$
Positive Supply Current		5.2	9.0	mA	$V_{out} \lessapprox 0$
Negative Supply Current		4.6	7.0	mA	
Power Consumption		90	150	mW	

DEFINITION OF TERMS:

LOGIC THRESHOLD VOLTAGE — The approximate voltage at the output of the comparator at which the loading logic circuitry changes its digital state.

INPUT OFFSET VOLTAGE* — The voltage between the input terminals when the output is at the logic threshold voltage. The input offset voltage may also be defined for the case where two equal resistances are inserted in series with the input leads.

INPUT OFFSET CURRENT* — The difference in the currents into the two input terminals with the output at the logic threshold voltage.

INPUT BIAS CURRENT* — The average of the two input currents.

INPUT VOLTAGE RANGE* — The range of voltage on the input terminals for which the comparator will operate within specifications.

DIFFERENTIAL INPUT VOLTAGE RANGE* — The range of voltage between the input terminals for which operation within specifications is assured.

VOLTAGE GAIN* — The ratio of the change in output voltage to the change in voltage between the input terminals producing it with the DC output level in the vicinity of the logic threshold voltage.

RESPONSE TIME* — The interval between the application of an input step function and the time when the output crosses the logic threshold voltage. The input step drives the comparator from some initial, saturated input voltage to an input level just barely in excess of that required to bring the output from saturation to the logic threshold voltage. This excess is referred to as the voltage overdrive.

STROBE RELEASE TIME* — The time required for the output to rise to the logic threshold voltage after the strobe terminal has been driven from the zero to the one logic level. Appropriate input conditions are assumed.

POSITIVE OUTPUT LEVEL* — The DC output voltage in the positive direction with the input voltage equal to or greater than a minimum specified amount.

NEGATIVE OUTPUT LEVEL* — The DC output voltage in the negative direction with the input voltage equal to or greater than a minimum specified amount.

OUTPUT SINK CURRENT — The maximum negative current that can be delivered by the comparator.

PEAK OUTPUT CURRENT — The maximum current that may flow into the output load without causing damage to the comparator.

OUTPUT RESISTANCE* — The resistance seen looking into the output terminal with the DC output level at the logic threshold voltage.

STROBED OUTPUT LEVEL* — The DC output voltage, independent of input voltage, with the voltage on the strobe terminal equal to or less than a minimum specified amount.

STROBE CURRENT — The maximum current drawn by the strobe terminal when it is at the zero logic level.

POWER CONSUMPTION — The DC power into the amplifier with no output load. The DC power will vary with signal level, but is specified as a maximum for the entire range of input-signal conditions.

*These definitions apply for either side with the other disabled with the strobe.

SPECIAL ORDERING CODE

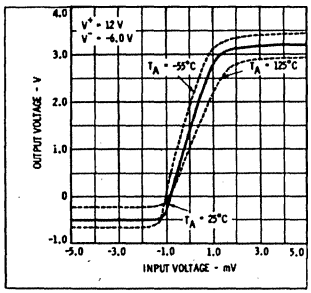
Temperature Range:
1 = −55° +125°C
5 = 0° to +70°C

Case Style:
D = Ceramic Dual In-Line, 16 leads, add "D" following last digit.

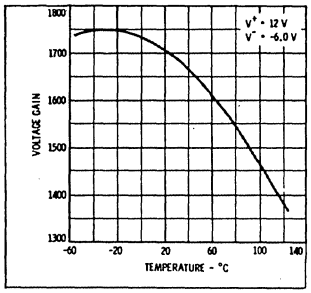
Example:
MIC720-1D is −55°C to +125°C temperature range in Ceramic Dual In-Line package.

TYPICAL CHARACTERISTICS MIC 720-1 ($T_A = +25°C$, $V^+ = 12.0V$, $V^- = -6.0V$ unless otherwise specified)

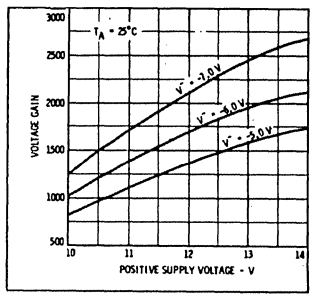
VOLTAGE TRANSFER CHARACTERISTIC



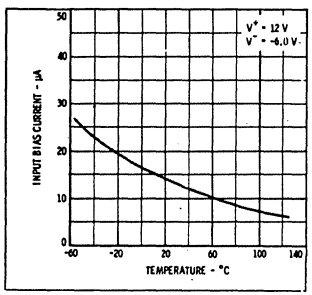
VOLTAGE GAIN AS A FUNCTION OF AMBIENT TEMPERATURE



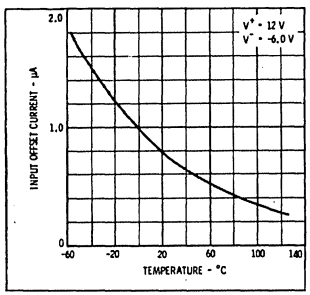
VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGES



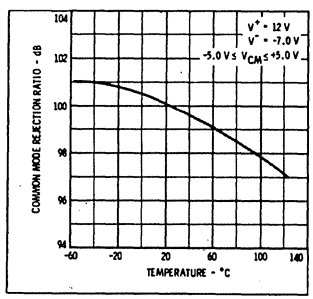
INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



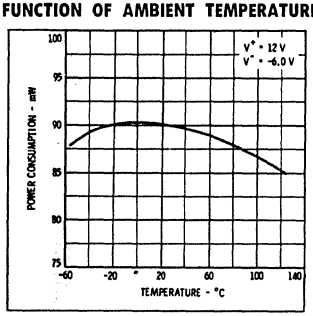
INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



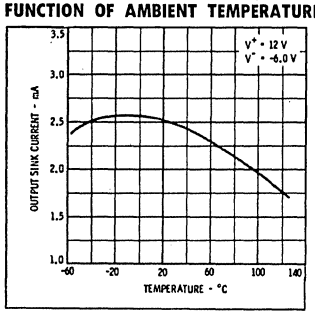
COMMON MODE REJECTION RATIO AS A FUNCTION OF AMBIENT TEMPERATURE



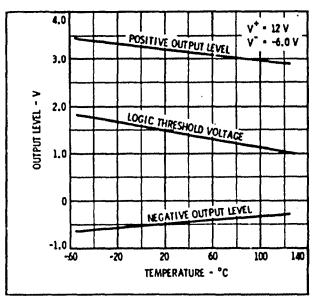
POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE



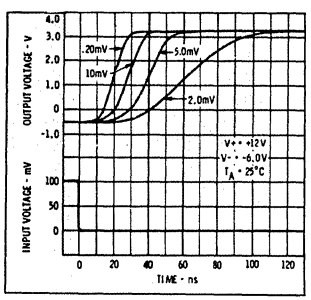
OUTPUT SINK CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



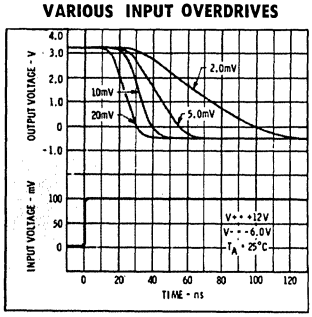
OUTPUT VOLTAGE LEVELS AS A FUNCTION OF AMBIENT TEMPERATURE



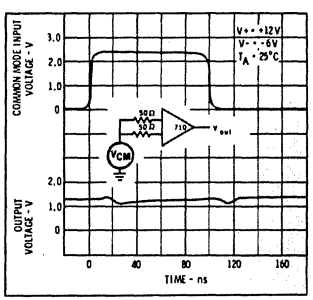
RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES

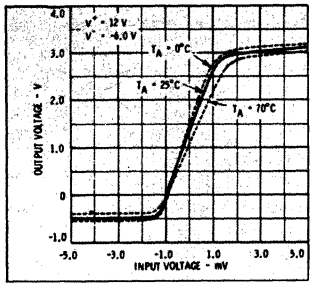


COMMON MODE PULSE RESPONSE

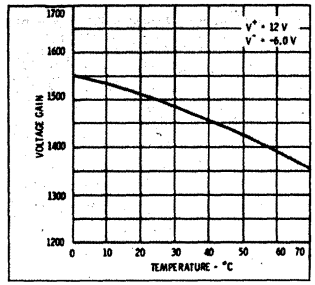


TYPICAL CHARACTERISTICS MIC 720-5 (TA = 25°C, V = 12.0V. V = −6.0V unless otherwise specified)

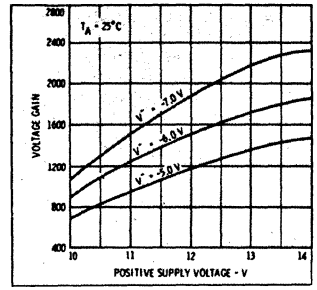
VOLTAGE TRANSFER CHARACTERISTIC



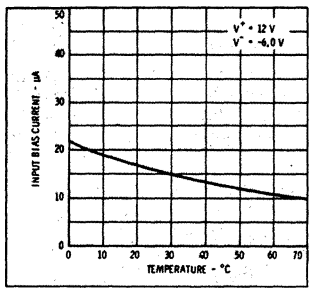
VOLTAGE GAIN AS A FUNCTION OF AMBIENT TEMPERATURE



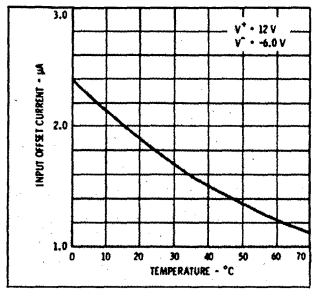
VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGES



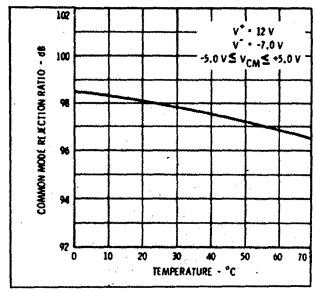
INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



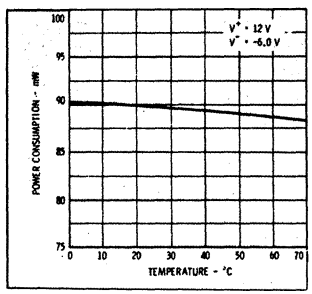
INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



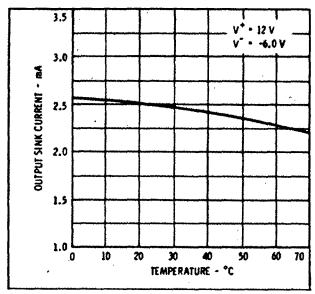
COMMON MODE REJECTION RATIO AS A FUNCTION OF AMBIENT TEMPERATURE



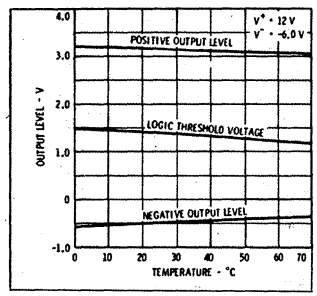
POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE



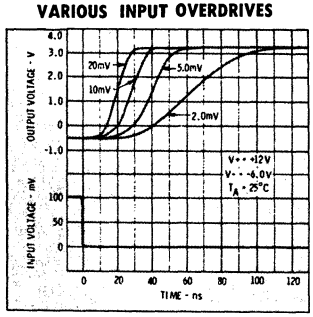
OUTPUT SINK CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



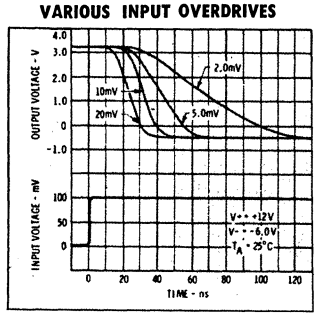
OUTPUT VOLTAGE LEVELS AS A FUNCTION OF AMBIENT TEMPERATURE



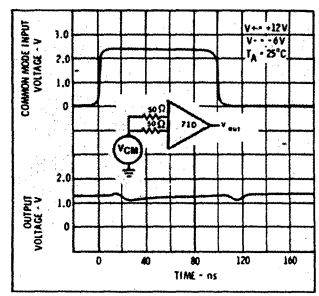
RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



COMMON MODE PULSE RESPONSE

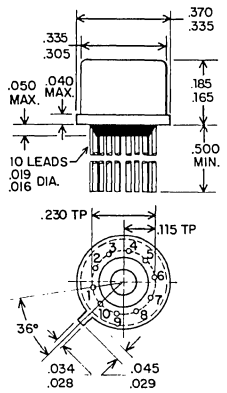


PRECISION VOLTAGE REGULATOR

- **Positive or Negative Supply Operation**
- **Series, Shunt, Switching or Floating Operation**
- **.01% Line and Load Regulation**
- **Output Voltage Adjustable From 2 to 37 Volts**
- **Output Current to 150 mA Without External Pass Transistor**

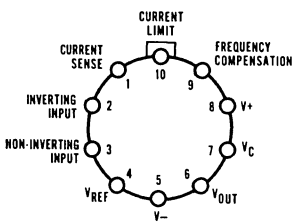
The MIC723 is a monolithic voltage regulator constructed on a single silicon chip using the epitaxial process. The device consists of a temperature compensated reference amplifier, error amplifier, power series pass transistor and current limit circuitry. Additional NPN or PNP pass elements may be used when output currents exceeding 150 mA are required. Provisions are made for adjustable current limiting and remote shutdown. In addition to the above, the device features low standby current drain, low temperature drift and high ripple rejection. The MIC723 is intended for use with positive or negative supplies as a series, shunt, switching or floating regulator. Applications include laboratory power supplies, isolation regulators for low level data amplifiers, logic card regulators, small instrument power supplies, airborne systems and other power supplies for digital and linear circuits.

DIMENSIONS



NOTES: LEADS ARE GOLD-PLATED KOVAR
PACKAGE WEIGHT IS 1.32 GRAMS

CONNECTION DIAGRAMS
TOP VIEWS



Note: On metal can, pin 5 is connected to case

ABSOLUTE MAXIMUM RATINGS

CHARACTERISTICS	MIC723-1	MIC723-5	UNITS
Pulse Voltage from V^+ to V^- (50 msec)	50		V
Voltage from V^+ to V^-		40	V
Continuous Voltage from V^+ to V^-	40		V
Maximum Output Current		150	mA
Input-Output Voltage Differential	40	40	V
Current from V_Z	25	25	mA
Current from V_{REF}	15	15	mA
Internal Power Dissipation — Metal Can (Note 1)	800	800	mW
Internal Power Dissipation — DIP (Note 1)	900	900	mW
Operating Temperature Range	−55 to +125	0 to +70	°C
Storage Temperature Range	−65 to +150	−65 to +150	°C
Lead Temperature (Soldering, 60 sec.)	300	300	°C

ELECTRICAL CHARACTERISTICS for MIC723-1 (Note 2)

PARAMETER (see definitions)	MIN.	TYP.	MAX.	UNITS	CONDITIONS
Line Regulation		.01	0.1	$\%V_{OUT}$	$V_{IN}=12$ V to $V_{IN}=15$ V
		.02	0.2	$\%V_{OUT}$	$V_{IN}=12$ V to $V_{IN}=40$ V
			0.3	$\%V_{OUT}$	$-55°C \leq T_A \leq +125°C$, $V_{IN}=12$ V to $V_{IN}=15$ V
Load Regulation		.03	0.15	$\%V_{OUT}$	$I_L=1$ mA to $I_L=50$ mA
			0.6	$\%V_{OUT}$	$-55°C \leq T_A \leq +125°C$, $I_L=1$ mA to $I_L=50$ mA
Ripple Rejection		74		dB	f=50 Hz to 10 kHz, $C_{REF}=0$
		86		dB	f=50 Hz to 10 kHz, $C_{REF}=5\ \mu F$
Average Temperature Coefficient of Output Voltage		.002	.015	%/°C	$-55°C \leq T_A \leq +125°C$
Short Circuit Current Limit		65		mA	$R_{SC}=10\ \Omega$, $V_{OUT}=0$
Reference Voltage	6.95	7.15	7.35	V	
Output Noise Voltage		20		μV_{rms}	BW=100 Hz to 10 kHz, $C_{REF}=0$
		2.5		μV_{rms}	BW=100 Hz to 10 kHz, $C_{REF}=5\ \mu F$
Long Term Stability		0.1		%/1000 hrs	
Standby Current Drain		2.3	3.5	mA	$I_L=0$, $V_{IN}=30$ V
Input Voltage Range	9.5		40	V	
Output Voltage Range	2.0		37	V	
Input-Output Voltage Differential	3.0		38	V	

DEFINITION OF TERMS

LINE REGULATION — The percentage change in output voltage for a specified change in input voltage.

LOAD REGULATION — The percentage change in output voltage for a specified change in load current.

RIPPLE REJECTION — The ratio of the peak to peak input ripple voltage to the peak to peak output ripple voltage.

AVERAGE TEMPERATURE COEFFICIENT OF OUTPUT VOLTAGE — The percentage change in output voltage for a specified change in ambient temperature.

SHORT CIRCUIT CURRENT LIMIT — The output current of the regulator with the output shorted to the negative supply.

REFERENCE VOLTAGE — The output of the reference amplifier measured with respect to the negative supply.

OUTPUT NOISE VOLTAGE — The rms output noise voltage with constant load and no input ripple.

STANDBY CURRENT DRAIN — The supply current drawn by the regulator with no output load and no reference voltage load.

INPUT VOLTAGE RANGE — The range of supply voltage over which the regulator will operate.

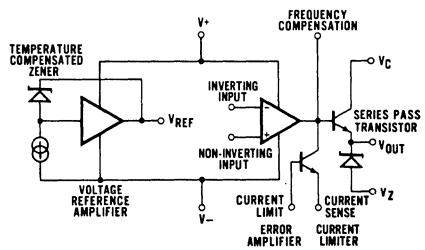
OUTPUT VOLTAGE RANGE — The range of output voltage over which the regulator will operate.

INPUT-OUTPUT VOLTAGE DIFFERENTIAL — The range of voltage difference between the supply voltage and the regulated output voltage over which the regulator will operate.

SENSE VOLTAGE — The voltage between current sense and current limit terminals necessary to cause current limiting.

TRANSIENT RESPONSE — The closed-loop step function response of the regulator under small-signal conditions.

EQUIVALENT CIRCUIT



NOTES:

(1) Derate metal can package at 6.8 mW/°C and dual-in-line package at 9 mW/°C for operation at ambient temperatures above 25°C.

(2) Unless otherwise specified, $T_A=25°C$, $V_{IN}=V^+=V_C=12$ V, $V^-=0$, $V_{ref}=5$ V, $I_L=1$ mA, $R_{SC}=0$, $C_I=100$ pF, $C_{REF}=0$ and divider impedance as seen by error amplifier ≤ 10 KΩ connected as shown in Fig. 1.

(3) L_1 is 40 turns of #20 enameled copper wire wound on Ferroxcube P36/22-3B7 pot core or equivalent with 0.009" air gap.

(4) Figures in parentheses may be used if R_1/R_2 divider is placed on opposite of error amp.

(5) Replace R_1/R_2 in figures with divider shown in figure 13.

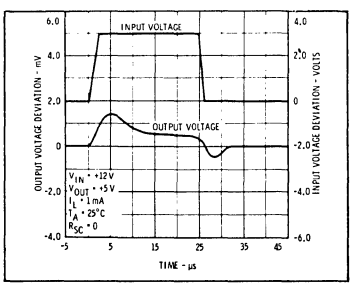
(6) V^+ must be connected to a +3 V or greater supply.

ELECTRICAL CHARACTERISTICS for MIC723-5 (Note 2)

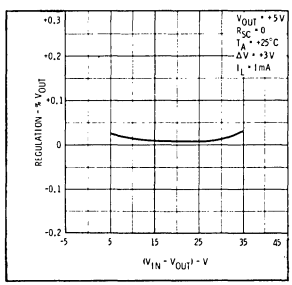
PARAMETER (see definitions)	MIN.	TYP.	MAX.	UNITS	CONDITIONS
Line Regulation		.01	0.1	% V_{OUT}	V_{IN} = 12 V to V_{IN} = 15 V
		0.1	0.5	% V_{OUT}	V_{IN} = 12 V to V_{IN} = 40 V
			0.3	% V_{OUT}	0°C ≤ T_A ≤ 70°C, V_{IN} = 12 V to V_{IN} = 15 V
Load Regulation		.03	0.2	% V_{OUT}	I_L = 1 mA to I_L = 50 mA
			0.6	% V_{OUT}	0°C ≤ T_A ≤ 70°C, I_L = 1 mA to I_L = 50 mA
Ripple Rejection		74		dB	f = 50 Hz to 10 kHz, C_{REF} = 0
		86		dB	f = 50 Hz to 10 kHz, C_{REF} = 5 μF
Average Temperature Coefficient of Output Voltage		.003	.015	%/°C	0°C ≤ T_A ≤ 70°C
Short Circuit Current Limit		65		mA	R_{SC} = 10 Ω, V_{OUT} = 0
Reference Voltage	6.80	7.15	7.50	V	
Output Noise Voltage		20		μV_{rms}	BW = 100 Hz to 10 kHz, C_{REF} = 0
		2.5		μV_{rms}	BW = 100 Hz to 10 kHz, C_{REF} = 5 μF
Long Term Stability		0.1		%/1000 hrs	
Standby Current Drain		2.3	4.0	mA	I_L = 0, V_{IN} = 30 V
Input Voltage Range	9.5		40	V	
Output Voltage Range	2.0		37	V	
Input-Output Voltage Differential	3.0		38	V	

TYPICAL PERFORMANCE CURVES MIC723-1, 723-5

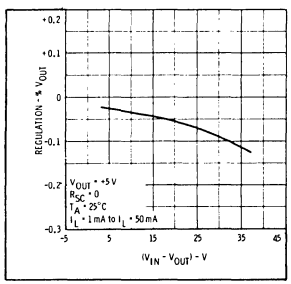
LINE TRANSIENT RESPONSE



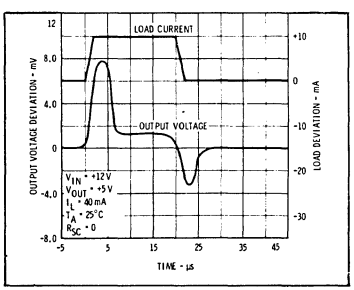
LINE REGULATION AS A FUNCTION OF INPUT-OUTPUT VOLTAGE DIFFERENTIAL



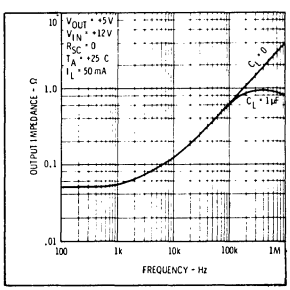
LOAD REGULATION AS A FUNCTION OF INPUT-OUTPUT VOLTAGE DIFFERENTIAL



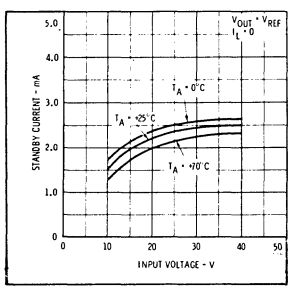
LOAD TRANSIENT RESPONSE



OUTPUT IMPEDANCE AS A FUNCTION OF FREQUENCY

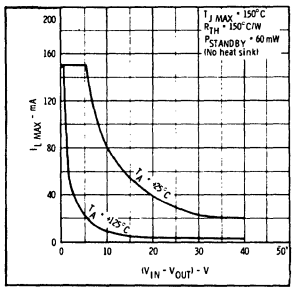


STANDBY CURRENT DRAIN AS A FUNCTION OF INPUT VOLTAGE

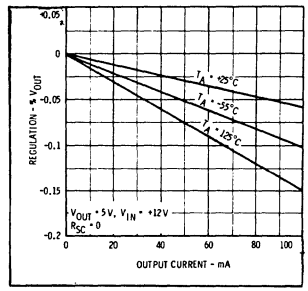


TYPICAL PERFORMANCE CURVES MIC723-1

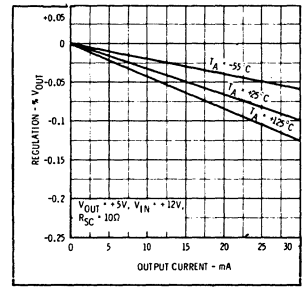
MAXIMUM LOAD CURRENT AS A FUNCTION OF INPUT-OUTPUT VOLTAGE DIFFERENTIAL



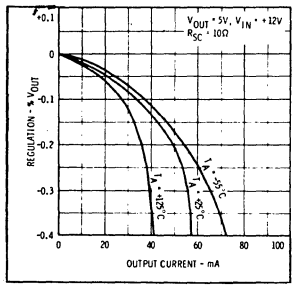
LOAD REGULATION CHARACTERISTICS WITHOUT CURRENT LIMITING



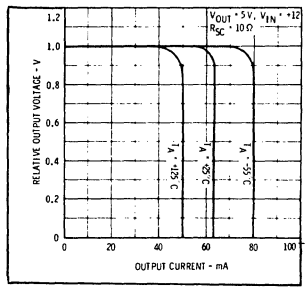
LOAD REGULATION CHARACTERISTICS WITH CURRENT LIMITING



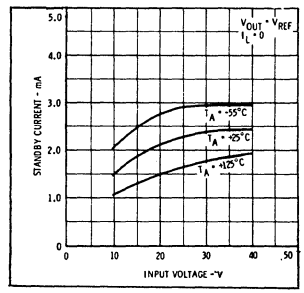
LOAD REGULATION CHARACTERISTICS WITH CURRENT LIMITING



CURRENT LIMITING CHARACTERISTICS

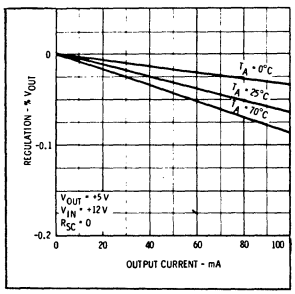


AS A STANDBY CURRENT DRAIN FUNCTION OF INPUT VOLTAGE

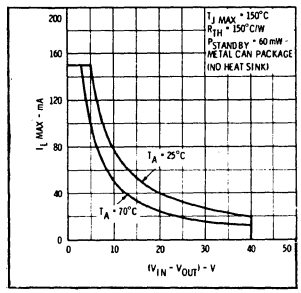


TYPICAL PERFORMANCE CURVES MIC723-5

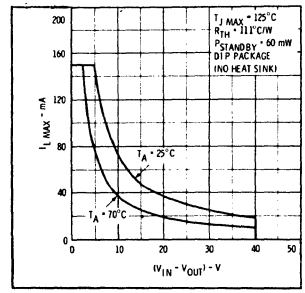
LOAD REGULATION CHARACTERISTICS WITHOUT CURRENT LIMITING



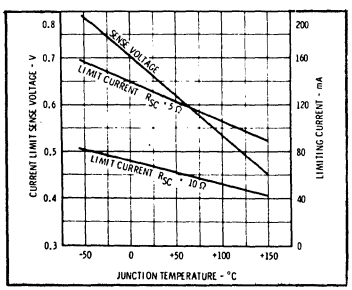
MAXIMUM LOAD CURRENT AS A FUNCTION OF INPUT-OUTPUT VOLTAGE DIFFERENTIAL



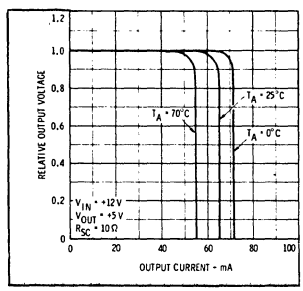
MAXIMUM LOAD CURRENT AS A FUNCTION OF INPUT-OUTPUT VOLTAGE DIFFERENTIAL



CURRENT LIMITING CHARACTERISTICS AS A FUNCTION OF JUNCTION TEMPERATURE



CURRENT LIMITING CHARACTERISTICS



LOAD REGULATION CHARACTERISTICS WITH CURRENT LIMITING

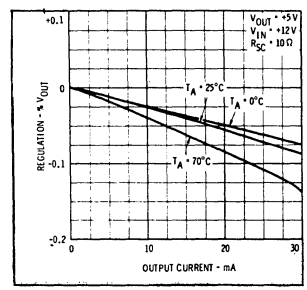


TABLE I — RESISTOR VALUES (kΩ) FOR STANDARD OUTPUT VOLTAGES

Positive Output Voltage	Applicable Figures	Fixed Output ±5%		Output Adjustable ±10% (Note 5)			Negative Output Voltage	Applicable Figures	Fixed Output ±5%		5% Output Adjustable ±10%		
	(Note 4)	R_1	R_2	R_1	P_1	R_2			R_1	R_2	R_1	P_1	R_2
+3.0	1, 5, 6, 9, 12 (4)	4.12	3.01	1.8	0.5	1.2	+100	7	3.57	102	2.2	10	91
+3.6	1, 5, 6, 9, 12 (4)	3.57	3.65	1.5	0.5	1.5	+250	7	3.57	255	2.2	10	240
+5.0	1, 5, 6, 9, 12 (4)	2.15	4.99	.75	0.5	2.2	−6 (note 6)	3, (10)	3.57	2.43	1.2	0.5	.75
+6.0	1, 5, 6, 9, 12 (4)	1.15	6.04	0.5	0.5	2.7	−9	3, 10	3.48	5.36	1.2	0.5	2.0
+9.0	2, 4, (5, 6, 12, 9)	1.87	7.15	.75	1.0	2.7	−12	3, 10	3.57	8.45	1.2	0.5	3.3
+12	2, 4, (5, 6, 9, 12)	4.87	7.15	2.0	1.0	3.0	−15	3, 10	3.65	11.5	1.2	0.5	4.3
+15	2, 4, (5, 6, 9, 12)	7.87	7.15	3.3	1.0	3.0	−28	3, 10	3.57	24.3	1.2	0.5	10
+28	2, 4, (5, 6, 9, 12)	21.0	7.15	5.6	1.0	2.0	−45	8	3.57	41.2	2.2	10	33
+45	7	3.57	48.7	2.2	10	39	−100	8	3.57	97.6	2.2	10	91
+75	7	3.57	78.7	2.2	10	68	−250	8	3.57	249	2.2	10	240

TABLE II — FORMULAE FOR INTERMEDIATE OUTPUT VOLTAGES

Outputs from +2 to +7 volts
[Figures 1, 5, 6, 9, 12, (4)]

$$V_{OUT} = [V_{REF} \times \frac{R_2}{R_1 + R_2}]$$

Outputs from +4 to +250 volts
[Figure 7]

$$V_{OUT} = [\frac{V_{REF}}{2} \times \frac{R_2 - R_1}{R_1}]\ ;\ R_3 = R_4$$

Current Limiting

$$I_{LIMIT} = \frac{V_{SENSE}}{R_{sc}}$$

Outputs from +7 to +37 volts
[Figures 2, 4, (5, 6, 9, 12)]

$$V_{OUT} = [V_{REF} \times \frac{R_1 + R_2}{R_2}]$$

Outputs from −6 to −250 volts
[Figures 3, 8, 10]

$$V_{OUT} = [\frac{V_{REF}}{2} \times \frac{R_1 + R_2}{R_1}]\ ;\ R_3 = R_4$$

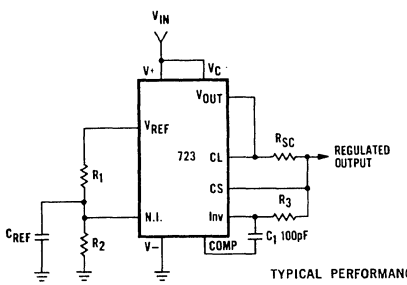
Foldback Current Limiting

$$I_{KNEE} = [\frac{V_{OUT}\ R_3}{R_{sc}\ R_4} + \frac{V_{SENSE}\ (R_3 + R_4)}{R_{sc}\ R_4}]$$

$$I_{SHORT\ CKT} = [\frac{V_{SENSE}}{R_{sc}} \times \frac{R_3 + R_4}{R_4}]$$

Figure 1

BASIC LOW VOLTAGE REGULATOR
(V_{out} = 2 to 7 Volts)



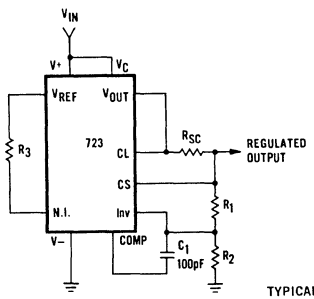
TYPICAL PERFORMANCE

Regulated Output Voltage	5 V
Line Regulation (ΔV_{IN} = 3 V)	0.5 mV
Load Regulation (ΔI_L=50 mA)	1.5 mV

Note: $R_3 = \frac{R_1\ R_2}{R_1 + R_2}$ for minimum temperature drift.

Figure 2

BASIC HIGH VOLTAGE REGULATOR
(V_{out} = 7 to 37 Volts)



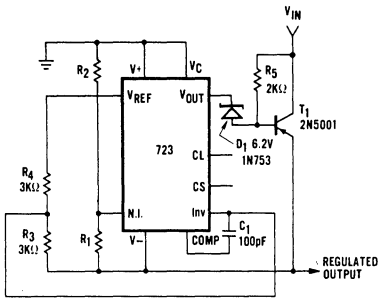
TYPICAL PERFORMANCE

Regulated Output Voltage	15 V
Line Regulation (ΔV_{IN} = 3 V)	1.5 mV
Load Regulation (ΔI_L=50 mA)	4.5 mV

Note: $R_3 = \frac{R_1\ R_2}{R_1 + R_2}$ for minimum temperature drift.

R_3 may be eliminated for minimum component count.

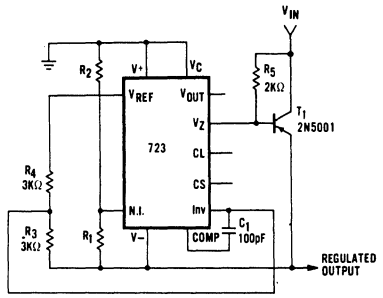
Figure 3
NEGATIVE VOLTAGE REGULATOR



TYPICAL PERFORMANCE

Regulated Output Voltage	−15 V
Line Regulation ($\Delta V_{IN} = 3$ V)	1 mV
Load Regulation ($\Delta I_L = 100$ mA)	2 mV

Figure 3A*
NEGATIVE VOLTAGE REGULATOR

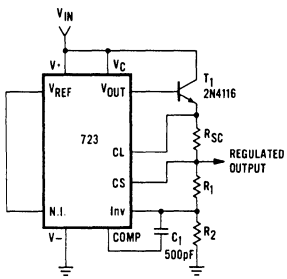


TYPICAL PERFORMANCE

Regulated Output Voltage	−15 V
Line Regulation ($\Delta V_{IN} = 3$ V)	1 mV
Load Regulation ($\Delta I_L = 100$ mA)	2 mV

Note 3

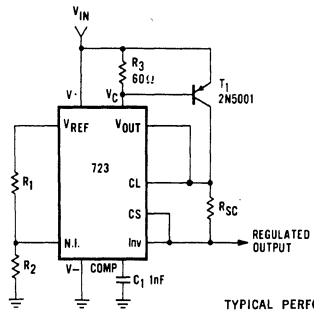
Figure 4
POSITIVE VOLTAGE REGULATOR (External NPN Pass Transistor)



TYPICAL PERFORMANCE

Regulated Output Voltage	+15 V
Line Regulation ($\Delta V_{IN} = 3$ V)	1.5 mV
Load Regulation ($\Delta I_L = 1$ A)	15 mV

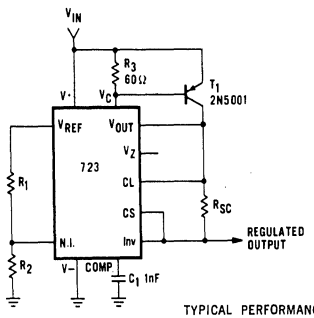
Figure 5
POSITIVE VOLTAGE REGULATOR (External PNP Pass Transistor)



TYPICAL PERFORMANCE

Regulated Output Voltage	+5 V
Line Regulation ($\Delta V_{IN} = 3$ V)	0.5 mV
Load Regulation ($\Delta I_L = 1$ A)	5 mV

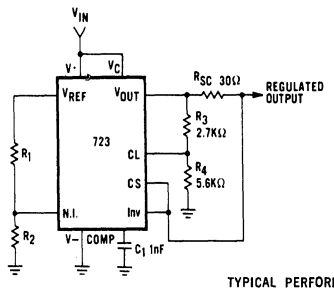
Figure 5A*
POSITIVE VOLTAGE REGULATOR (External PNP Pass Transistor)



TYPICAL PERFORMANCE

Regulated Output Voltage	+5 V
Line Regulation ($\Delta V_{IN} = 3$ V)	0.5 mV
Load Regulation ($\Delta I_L = 1$ A)	5 mV

Figure 6
FOLDBACK CURRENT LIMITING

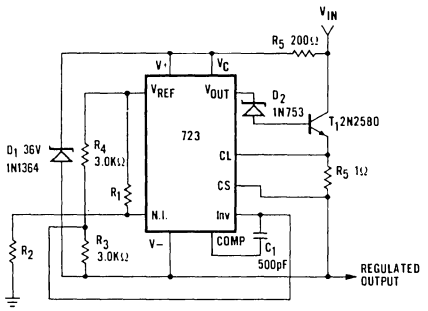


TYPICAL PERFORMANCE

Regulated Output Voltage	+5 V
Line Regulation ($\Delta V_{IN} = 3$ V)	0.5 mV
Load Regulation ($\Delta I_L = 10$ mA)	1 mV
Current Limit Knee	20 mA

* Figure numbers followed by "A" indicate low temperature range

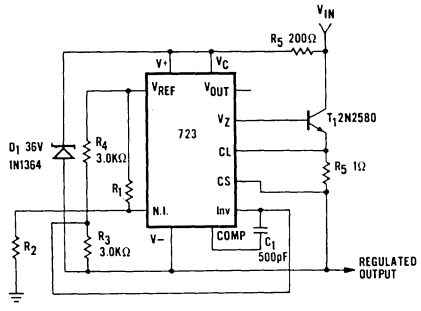
Figure 7
POSITIVE FLOATING REGULATOR



TYPICAL PERFORMANCE

Regulated Output Voltage	+50 V
Line Regulation ($\Delta V_{IN} = 20$ V)	15 mV
Load Regulation ($\Delta I_L = 50$ mA)	20 mV

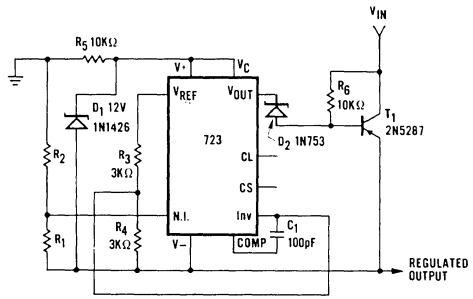
Figure 7A*
POSITIVE FLOATING REGULATOR



TYPICAL PERFORMANCE

Regulated Output Voltage	+50 V
Line Regulation ($\Delta V_{IN} = 20$ V)	15 mV
Load Regulation ($\Delta I_L = 50$ mA)	20 mV

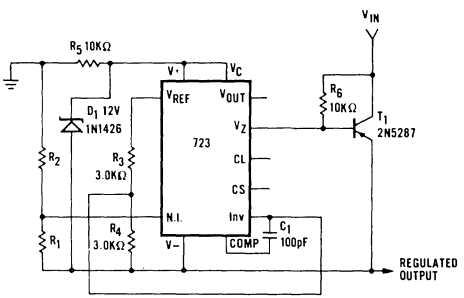
Figure 8
NEGATIVE FLOATING REGULATOR



TYPICAL PERFORMANCE

Regulated Output Voltage	−100 V
Line Regulation ($\Delta V_{IN} = 20$ V)	30 mV
Load Regulation (ΔI_L=100 mA)	20 mV

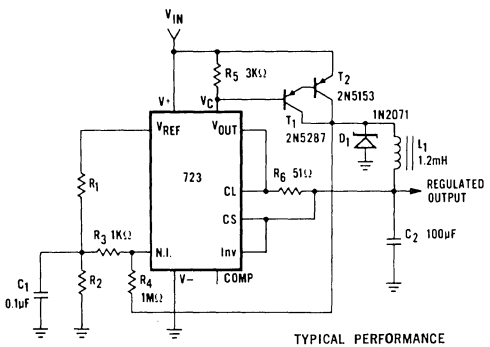
Figure 8A*
NEGATIVE FLOATING REGULATOR



TYPICAL PERFORMANCE

Regulated Output Voltage	−100 V
Line Regulation ($\Delta V_{IN} = 20$ V)	30 mV
Load Regulation (ΔI_L=100 mA)	20 mV

Figure 9
POSITIVE SWITCHING REGULATOR

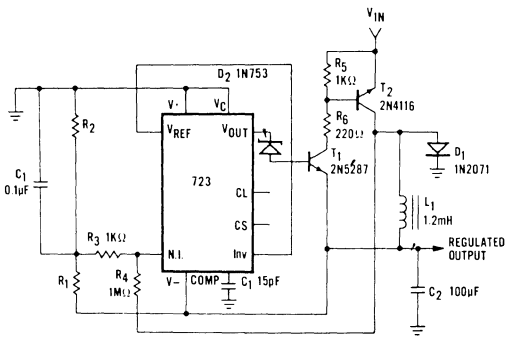


TYPICAL PERFORMANCE

Regulated Output Voltage	+5 V
Line Regulation ($\Delta V_{IN} = 30$ V)	10 mV
Load Regulation ($\Delta I_L = 2$ A)	80 mV

Note 3

Figure 10
NEGATIVE SWITCHING REGULATOR



TYPICAL PERFORMANCE

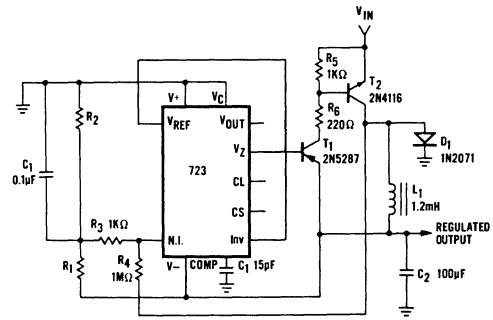
Regulated Output Voltage	−15 V
Line Regulation ($\Delta V_{IN} = 20$ V)	8 mV
Load Regulation ($\Delta I_L = 2$ A)	6 mV

Note 3

* Figure numbers followed by "A" indicate low temperature range

Figure 10A*

NEGATIVE SWITCHING REGULATOR



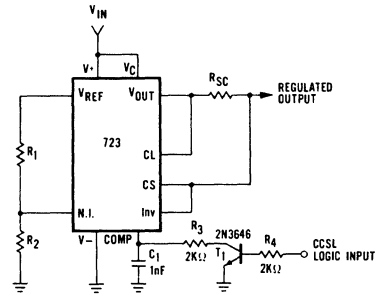
TYPICAL PERFORMANCE

Regulated Output Voltage	−15 V
Line Regulation (ΔV_{IN} = 20 V)	8 mV
Load Regulation (ΔI_L = 2 A)	6 mV

Note 3
Note 7

Figure 11

REMOTE SHUTDOWN REGULATOR WITH CURRENT LIMITING



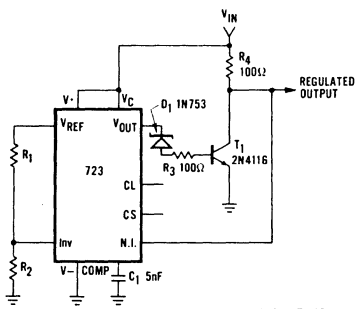
Note: Current limit transistor may be used for shutdown if current limiting is not required.

TYPICAL PERFORMANCE

Regulated Output Voltage	+5 V
Line Regulation (ΔV_{IN} = 3 V)	0.5 mV
Load Regulation (ΔI_L=50 mA)	1.5 mV

Figure 12

SHUNT REGULATOR

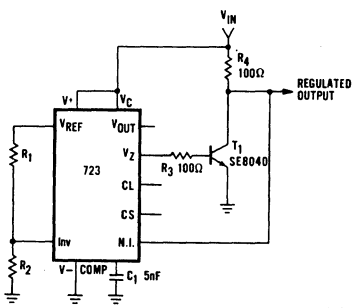


TYPICAL PERFORMANCE

Regulated Output Voltage	+5 V
Line Regulation (ΔV_{IN} = 10 V)	0.5 mV
Load Regulation (ΔI_L = 100 mA)	1.5 mV

Figure 12 *

SHUNT REGULATOR



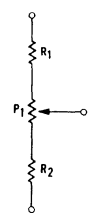
Note 3

TYPICAL PERFORMANCE

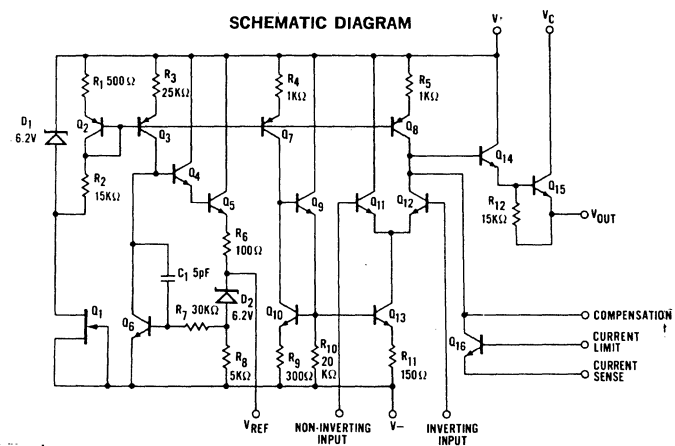
Regulated Output Voltage	+5 V
Line Regulation (ΔV_{IN} = 10 V)	0.5 mV
Load Regulation (ΔI_L = 100 mA)	1.5 mV

Figure 13

OUTPUT VOLTAGE ADJUST



SCHEMATIC DIAGRAM



* Figure numbers followed by "A" indicate low temperature range.

TEMPERATURE-CONTROLLED DIFFERENTIAL PAIR

- **Excellent Transistor Matching**
- **Close Thermal Coupling**
- **Fast Thermal Response**
- **Tight Temperature Control**

MIC726 is a monolithic transistor pair in a high thermal-resistance package, held at a constant temperature by active temperature regulator circuitry. The transistor pair displays the excellent matching, close thermal coupling and fast thermal response inherent in monolithic construction. The high gain and low standby dissipation of the regulator circuit permits tight temperature control over a wide range of ambient temperatures. It is intended for use as an input stage in very-low drift dc amplifiers, replacing complex chopper-stabilized amplifiers; it is also useful as the nonlinear element in logarithmic amplifiers and multipliers where the highly predictable exponential relation between emitter-base voltage and collector current is employed. The device is constructed on a single silicon chip using the ITT Planar process.

ABSOLUTE MAXIMUM RATINGS

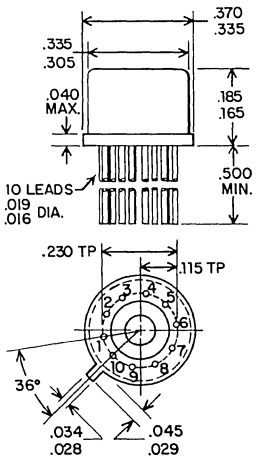
CHARACTERISTICS	UNITS
Operating Temperature Range	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering 60 seconds)	300°C
Supply Voltage	±18 V

MAXIMUM RATINGS FOR EACH TRANSISTOR

CHARACTERISTICS	UNITS
Maximum collector-to-substrate voltage	40 V
BV_{CBO}	40 V
LV_{CEO} [Note 1]	30 V
BV_{EBO}	5 V
Collector Current	5 mA

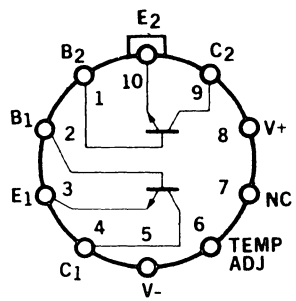
Note 1: Measured at 1 mA collector current.

PHYSICAL DIMENSIONS



NOTES: LEADS ARE GOLD-PLATED KOVAR
PACKAGE WEIGHT IS 1.32 GRAMS

CONNECTION DIAGRAM



SPECIAL ORDERING CODE

Temperature Range:
1 = −55°C to 125°C
5 = 0°C to 70°C

Package:
C = 10-lead TO-5
D = 14-lead DIP

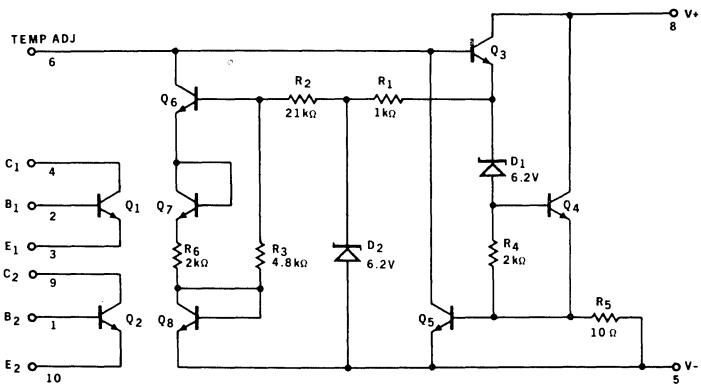
Example:
MIC726-1C means operating temperature range of −55°C to +125°C, supplied in a TO-5 package.

ELECTRICAL CHARACTERISTICS for MIC 726-1

($-55°C \leq T_A \leq +125°C$, $V_S = \pm 15$ V, $R_{adj} = 62k\Omega$ unless otherwise specified)

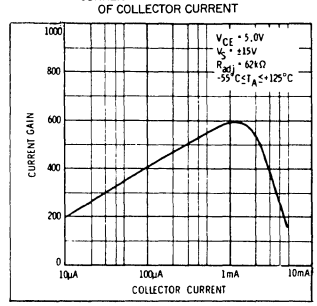
PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
Input Offset Voltage		1.0	2.5	mV	$10\ \mu A \leq I_C \leq 100\mu A$ $V_{CE} = 5$ V, $R_S \leq 50\Omega$
Input Offset Current		10	50	nA	$I_C = 10\ \mu A$, $V_{CE} = 5$ V
Input Offset Current		50	200	nA	$I_C = 100\ \mu A$, $V_{CE} = 5$ V
Average Input Bias Current		50	150	nA	$I_C = 10\ \mu A$, $V_{CE} = 5$ V
Average Input Bias Current		250	500	nA	$I_C = 100\ \mu A$, $V_{CE} = 5$ V
Offset Voltage Change		0.3	6.0	mV	$I_C = 10\ \mu A$, $5\text{ V} \leq V_{CE} \leq 25$ V, $R_S \leq 100$ kΩ
Offset Voltage Change		0.3	6.0	mV	$I_C = 100\ \mu A$, $5\text{ V} \leq V_{CE} \leq 25$ V, $R_S \leq 10$ kΩ
Input Offset Voltage Drift		0.2	1.0	μV/°C	$10\ \mu A \leq I_C \leq 100\ \mu A$, $V_{CE} = 5$ V, $R_S \leq 50\Omega$, $+25°C \leq T_A \leq +125°C$
Input Offset Voltage Drift		0.2	1.0	μV/°C	$10\ \mu A \leq I_C \leq 100\ \mu A$, $V_{CE} = 5$ V, $R_S \leq 50\Omega$, $-55°C \leq T_A \leq +25°C$
Input Offset Current Drift		10		pA/°C	$I_C = 10\ \mu A$, $V_{CE} = 5$ V
Input Offset Current Drift		30		pA/°C	$I_C = 100\ \mu A$, $V_{CE} = 5$ V
Supply Voltage Rejection Ratio		25		μV/V	$10\ \mu A \leq I_C \leq 100\ \mu A$, $R_S \leq 50\Omega$,
Low-Frequency Noise		4.0		μV pp	$I_C = 10\ \mu A$, $V_{CE} = 5$ V, $R_S \leq 50\Omega$, BW = .001 Hz to 0.1 Hz
Broadband Noise		10		μV pp	$I_C = 10\ \mu A$, $V_{CE} = 5$ V, $R_S \leq 50\Omega$, BW = 0.1 Hz to 10 kHz
Long-Term Drift		5.0		μV/week	$10\ \mu A \leq I_C \leq 100\ \mu A$, $V_{CE} = 5$ V, $R_S \leq 50\Omega$, $T_A = 25°C$
High-Frequency Current Gain	1.5	3.5			$f = 20$ MHz, $I_C = 100\ \mu A$, $V_{CE} = 5$ V
Output Capacitance		1.0		pF	$I_E = 0$, $V_{CB} = 5$ V
Emitter Transition Capacitance		1.0		pF	$I_E = 100\ \mu A$
Collector Saturation Voltage		0.5	1.0	V	$I_B = 100\ \mu A$, $I_C = 1$ mA

TYPICAL CHARACTERISTICS FOR MIC726-1

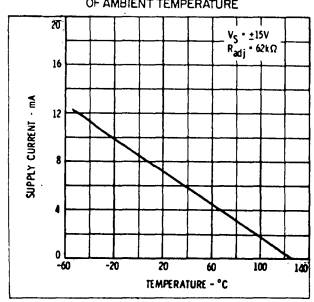


SCHEMATIC DIAGRAM-1-5

CURRENT GAIN AS A FUNCTION OF COLLECTOR CURRENT



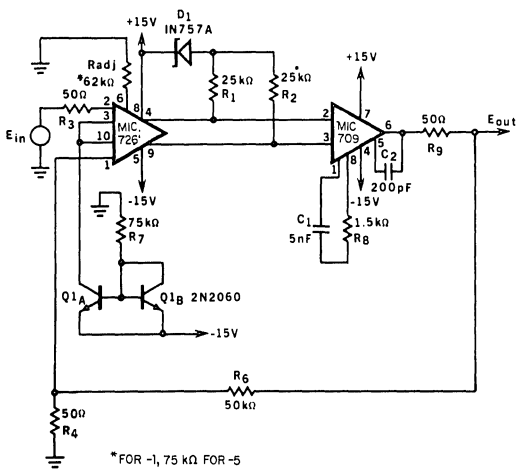
SUPPLY CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



ELECTRICAL CHARACTERISTICS for MIC726-5

($0°C \leq T_A \leq +85°C$, $V_S = \pm 15$ V, $R_{adj} = 75$ kΩ unless otherwise specified)

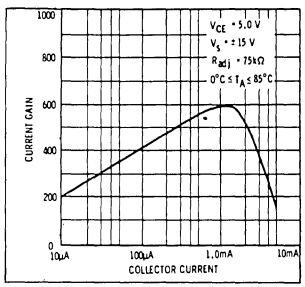
PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
Input Offset Voltage		1.0	3.0	mV	10 μA ≤ I_C ≤ 100μA V_{CE} = 5 V, $R_S \leq$ 50Ω
Input Offset Current		10	100	nA	I_C = 10 μA, V_{CE} = 5 V
Input Offset Current		50	400	nA	I_C = 100 μA, V_{CE} = 5 V
Average Input Bias Current		50	300	nA	I_C = 10 μA, V_{CE} = 5 V
Average Input Bias Current		250	1000	nA	I_C = 100 μA, V_{CE} = 5 V
Offset Voltage Change		0.3	6.0	mV	I_C = 10 μA, 5 V ≤ V_{CE} ≤ 25 V, $R_S \leq$ 100 kΩ
Offset Voltage Change		0.3	6.0	mV	I_C = 100 μA, 5 V ≤ V_{CE} ≤ 25 V, $R_S \leq$ 10 kΩ
Input Offset Voltage Drift		0.2	2.0	μV/°C	I_C = 100 μA, V_{CE} = 5 V, $R_S \leq$ 50Ω
Input Offset Current Drift		10		pA/°C	I_C = 10 μA, V_{CE} = 5 V
Input Offset Current Drift		30		pA/°C	I_C = 100 μA, V_{CE} = 5 V
Supply Voltage Rejection Ratio		25		μV/V	I_C = 100 μA, R_S = 50Ω
Low-Frequency Noise		4.0		μV pp	I_C = 10 μA, V_{CE} = 5 V, $R_S \leq$ 50Ω, BW = 0.001 Hz to 0.1 Hz
Broadband Noise		10		μV pp	I_C = 10 μA, V_{CE} = 5 V, $R_S \leq$ 50Ω, BW = O.1 Hz to 10 kHz
Long-Term Drift		5.0		μV/week	I_C = 100 μA, V_{CE} = 5 V, $R_S \leq$ 50Ω, T_A = 25°C
High-Frequency Current Gain	1.5	3.5			f = 20 MHz, I_C = 100 μA, V_{CE} = 5 V
Output Capacitance		1.0		pF	I_E = 0, V_{CB} = 5 V
Emitter Transition Capacitance		1.0		pF	I_E = 100 μA
Collector Saturation Voltage		0.5	1.0	V	I_B = 100 μA, I_C = 1 mA



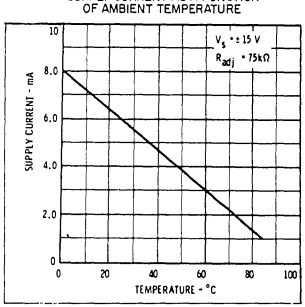
TYPICAL X1000 CIRCUIT

TYPICAL CHARACTERISTICS FOR MIC726-5

CURRENT GAIN AS A FUNCTION OF COLLECTOR CURRENT



SUPPLY CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE

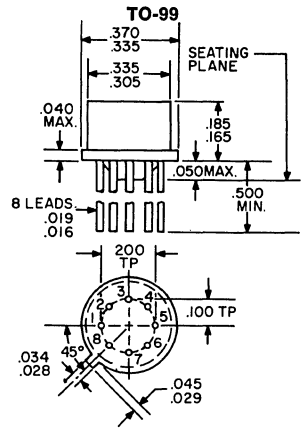


DIFFERENTIAL AMPLIFIER

- **Low Input Offset Voltage**
- **High and Low Impedance Differential Outputs**
- **1.0 MHz Bandwidth**

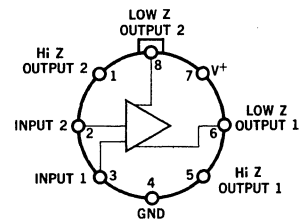
The MIC730 is a differential amplifier constructed on a single silicon-chip using the ITT Planar epitaxial process. This device has a wide range of applications since it has both a differential input and output; any combination of single-ended or differential configurations can be employed at its input and output. The emitter follower output stage gives this device a low output impedance making it useful as a preamplifier.

PHYSICAL DIMENSIONS
TO-99



NOTE: DIMENSIONS AS PER LATEST JS-10 COMMITTEE.
ALL DIMENSIONS IN INCHES.
LEADS ARE GOLD-PLATED KOVAR.
PACKAGE WEIGHT IS 1.22 GRAMS.

CONNECTION DIAGRAM



Note: Pin 4 connected to case

ABSOLUTE MAXIMUM RATINGS

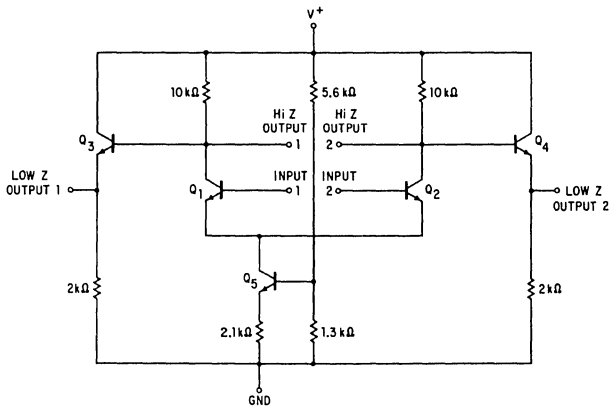
CHARACTERISTICS		UNITS
Supply Voltage	15	V
Differential Input Voltage	±5	V
Common Mode Input Voltage	2.5 to 5.5	V
Internal Power Dissipation (Note 1 and 2)	300	mW
Operating Temperature Range (Note 3)	−55 to +125	°C
Storage Temperature Range	−65 to +150	°C
Lead Temperature (Soldering, 60 seconds)	+300	°C

NOTES: (1) Rating applies for case temperature to +125°C; derate linearly at 5.6 mW/°C for ambient temperature above +105°C.

(2) Rating applies for ambient temperatures to +70°C.

(3) Also limited temperature range from 0°C to +70°C.

SCHEMATIC DIAGRAM



SPECIAL ORDERING CODE

Temperature Range:
1 = −55°C to +125°C
5 = 0°C to +70°C

Package:
C = TO-99

Example:
MIC730-1C means operating temperature range of −55°C to +125°C, supplied in a TO-99 package.

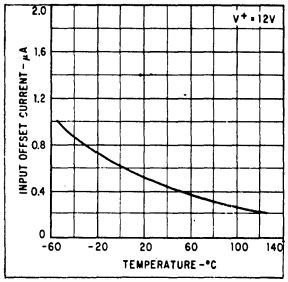
For Package Options:
Contact local ITT Franchised Distributor or Field Sales Office.

ELECTRICAL CHARACTERISTICS ($T_A = 25°C$, $V+ = 12.0$ V, and $V_{CM} = 3.5$ V unless otherwise specified)

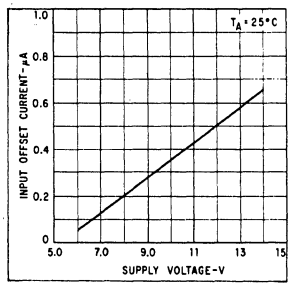
PARAMETER (See Definitions)	−55°C to +125°C			CONDITIONS	0°C to +70°C			UNITS	CONDITIONS
	MIN.	TYP.	MAX.		MIN.	TYP.	MAX.		
Input Offset Voltage		1.0	2.5	$R_S \leq 50\Omega$		2.0	5.0	mV	$R_S \leq 50\Omega$
Input Offset Current		0.5	1.5			0.7	3.0	μA	
Input Bias Current		3.5	7.5			4.5	16.0	μA	
Input Resistance	5.0	20			2.5	15		kΩ	
Differential Voltage Gain	100	145	160	$R_L \geq 100$ kΩ	100	135	160		$R_L \geq 100$ kΩ
Differential Distortion		80	300	$R_L \geq 100$ kΩ		85	300	mVpp	$R_L \geq 100$ kΩ
Bandwidth	1.0	1.5			1.0	1.5		MHz	
Single-Ended Output Resistance		70	500			70	500	Ω	
Output Voltage Swing	5.0	8.0		$R_L \geq 100$ kΩ	5.0	8.0		Vpp	$R_L \geq 100$ kΩ
Supply Current		9.5	13	$R_L \geq 100$ kΩ		9.5	13	mA	$R_L \geq 100$ kΩ
Power Consumption		114	156	$R_L \geq 100$ kΩ		114	156	mW	$R_L \geq 100$ kΩ
The following specifications apply for $-55°C \leq T_A \leq 125°C$:					The following specifications apply for $0°C \leq T_A \leq +70°C$:				
Input Offset Voltage			3.5	$R_S \leq 50\Omega$			7.5	mV	$R_S \leq 50\Omega$
Input Offset Current		0.2	1.5	$T_A = +125°C$		0.5	3.0	μA	$T_A = +70°C$
		1.0	3.0	$T_A = -55°C$		0.8	5.0	μA	$T_A = 0°C$
Input Bias Current		6.5	15	$T_A = -55°C$		5.0	20	μA	$T_A = 0°C$
Input Resistance	0.9				1.8			kΩ	
Input Voltage Range	3.5		5.2		+3.5		+5.2		
Common Mode Rejection Ratio	70	85		$R_S \leq 50\Omega$, $f \leq 1.0$ kHz, $+3.5\text{ V} \leq V_{CM} \leq +5.2\text{ V}$	60	80		dB	$R_S \leq 50\Omega$, $f \leq 1.0$ kHz, $+3.5\text{ V} \leq V_{CM} \leq +5.2\text{ V}$
Differential Voltage Gain	90		175	$R_L \geq 100$ kΩ	80		190		$R_L \geq 100$ kΩ
Common Mode Output Voltage	5.5	7.0	7.75		5.0	7.0	8.0	V	
Output Resistance			600				600	Ω	
Output Voltage Swing	4.5	6.8			4.5	7.5		Vpp	
Supply Current		10	15	$T_A = -55°C$		10	15	mA	$T_A = 0°C$
		8.0	11	$T_A = 125°C$		8.8	13	mA	$T_A = +70°C$
Power Consumption		120	180	$T_A = -55°C$		120	180	mW	$T_A = 0°C$
		96	121	$T_A = 125°C$		100	158	mW	$T_A = +70°C$

TYPICAL PERFORMANCE CURVES FOR −55°C TO +125°C

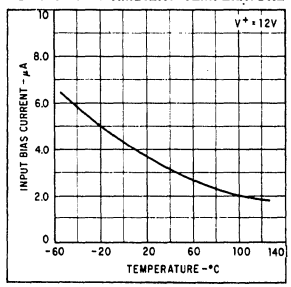
INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



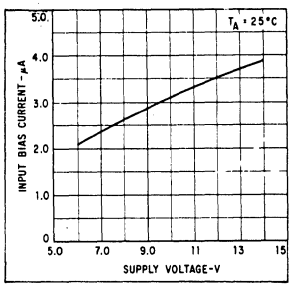
INPUT OFFSET CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



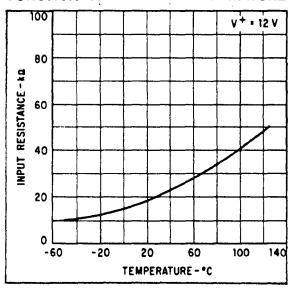
INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



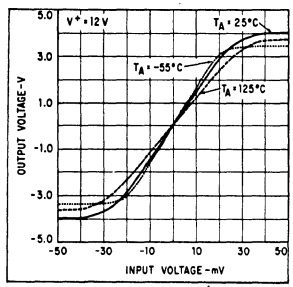
INPUT BIAS CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



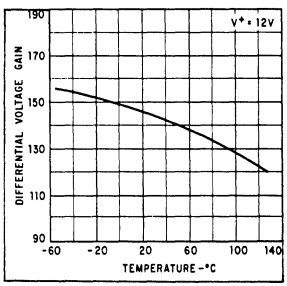
INPUT RESISTANCE AS A FUNCTION OF AMBIENT TEMPERATURE



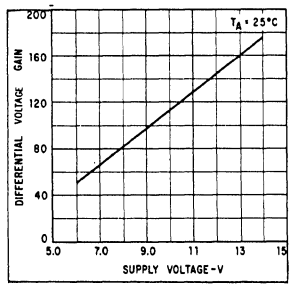
VOLTAGE TRANSFER CHARACTERISTICS



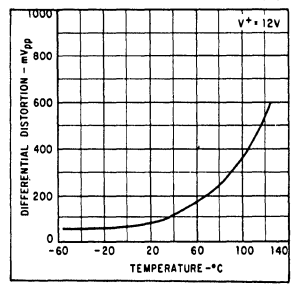
DIFFERENTIAL VOLTAGE GAIN AS A FUNCTION OF AMBIENT TEMPERATURE



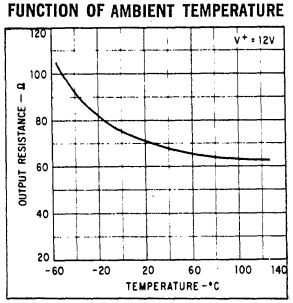
DIFFERENTIAL VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE



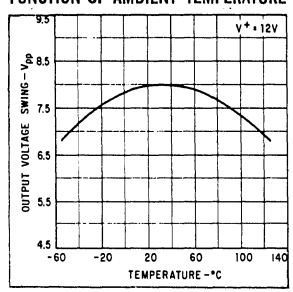
DIFFERENTIAL DISTORTION AS A FUNCTION OF AMBIENT TEMPERATURE



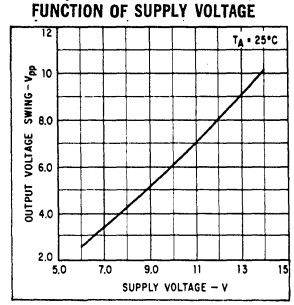
OUTPUT RESISTANCE AS A FUNCTION OF AMBIENT TEMPERATURE



OUTPUT VOLTAGE SWING AS A FUNCTION OF AMBIENT TEMPERATURE

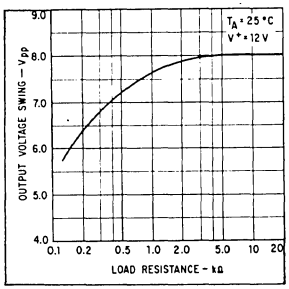


OUTPUT VOLTAGE SWING AS A FUNCTION OF SUPPLY VOLTAGE

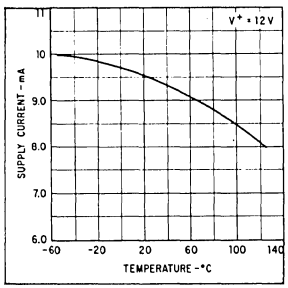


TYPICAL PERFORMANCE CURVES FOR −55°C TO +125°C

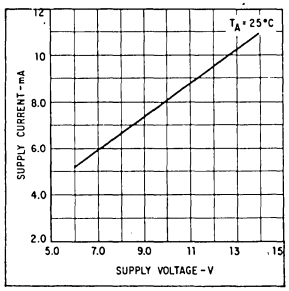
OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE



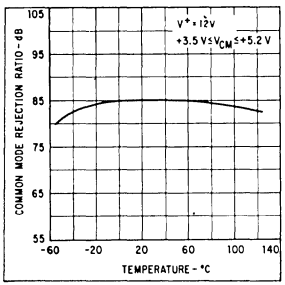
SUPPLY CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



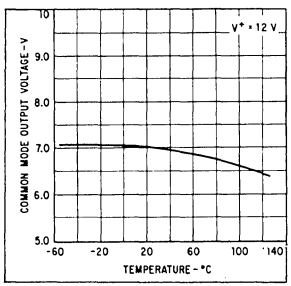
SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



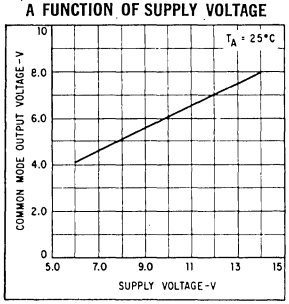
COMMON MODE REJECTION RATIO AS A FUNCTION OF AMBIENT TEMPERATURE



COMMON MODE OUTPUT VOLTAGE AS A FUNCTION OF AMBIENT TEMPERATURE

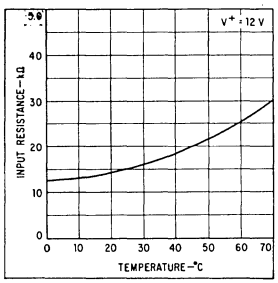


COMMON MODE OUTPUT VOLTAGE AS A FUNCTION OF SUPPLY VOLTAGE

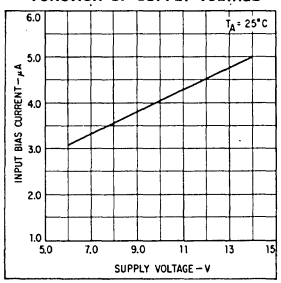


TYPICAL PERFORMANCE CURVES FOR 0°C TO +70°C

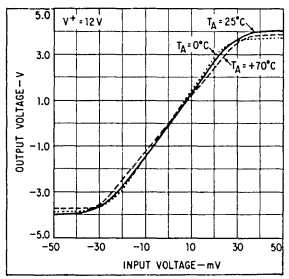
INPUT RESISTANCE AS A FUNCTION OF AMBIENT TEMPERATURE



INPUT BIAS CURRENT AS A FUNCTION OF SUPPLY VOLTAGE

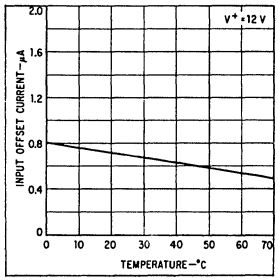


VOLTAGE TRANSFER CHARACTERISTICS

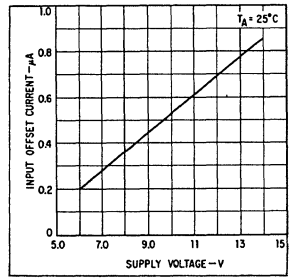


TYPICAL PERFORMANCE CURVES FOR 0°C TO +70°C

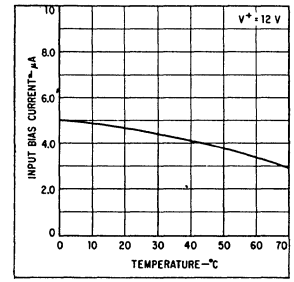
INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



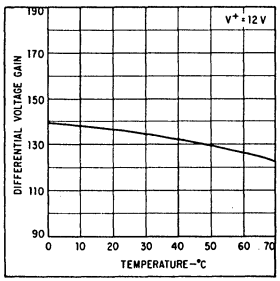
INPUT OFFSET CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



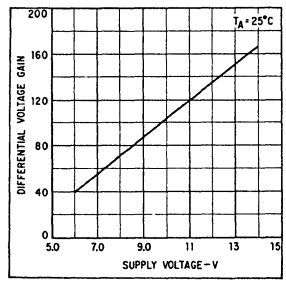
INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



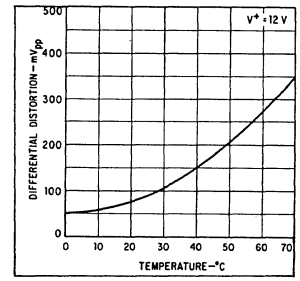
DIFFERENTIAL DISTORTION AS A FUNCTION OF AMBIENT TEMPERATURE



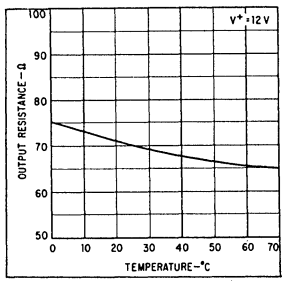
DIFFERENTIAL VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE



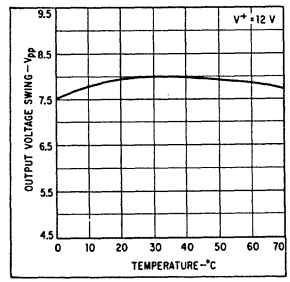
DIFFERENTIAL VOLTAGE GAIN AS A FUNCTION OF AMBIENT TEMPERATURE



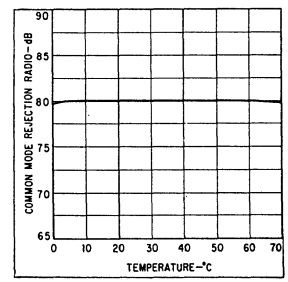
OUTPUT RESISTANCE AS A FUNCTION OF AMBIENT TEMPERATURE



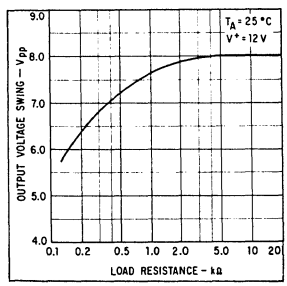
OUTPUT VOLTAGE SWING AS A FUNCTION OF AMBIENT TEMPERATURE



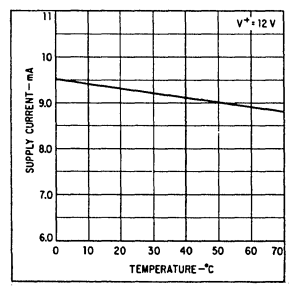
COMMON MODE REJECTION RATIO AS A FUNCTION OF AMBIENT TEMPERATURE



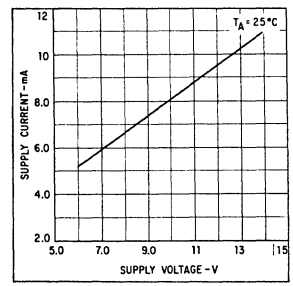
OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE



SUPPLY CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE

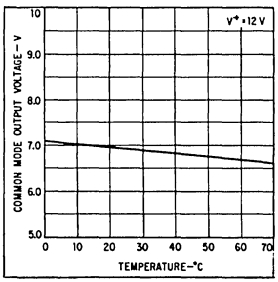


SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE

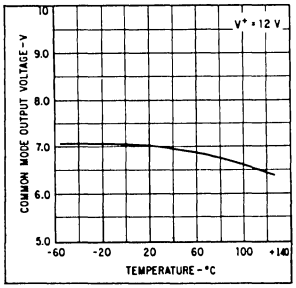


TYPICAL PERFORMANCE CURVES FOR 0°C TO +70°C

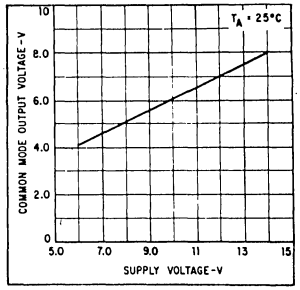
COMMON MODE OUTPUT VOLTAGE AS A FUNCTION OF AMBIENT TEMPERATURE



COMMON MODE OUTPUT VOLTAGE AS A FUNCTION OF AMBIENT TEMPERATURE



COMMON MODE OUTPUT VOLTAGE AS A FUNCTION OF SUPPLY VOLTAGE



DEFINITION OF TERMS

INPUT OFFSET VOLTAGE — That voltage which must be applied between the input terminals to obtain zero differential output voltage.

INPUT OFFSET CURRENT — The difference in the currents into the two input terminals with the output at zero differential volts.

INPUT BIAS CURRENT — The average of the two input currents.

INPUT BIAS RESISTANCE — The resistance looking into either input terminal with the other grounded.

INPUT VOLTAGE RANGE — The range of voltage which, if exceeded on either input terminal, could cause the amplifier to cease functioning properly.

COMMON MODE REJECTION RATIO — The ratio of the input voltage range to the maximum change in input offset voltage over this range.

DIFFERENTIAL VOLTAGE GAIN — The ratio of the change in the differential output voltage to the change in voltage between the input terminals producing it.

DIFFERENTIAL DISTORTION — The A.C. unbalance in the output common mode voltage produced by unsymmetrical output voltage swings.

BANDWIDTH — The frequency at which the differential voltage gain is 3 dB below its low frequency value.

OUTPUT RESISTANCE — The resistance seen looking into either output terminal with the output at differential null.

COMMON MODE OUTPUT VOLTAGE — The average voltage at the two output terminals referred to ground.

OUTPUT VOLTAGE SWING — The peak-to-peak output swing that can be obtained without clipping.

SUPPLY CURRENT — The current required from the power supply to operate the device with no load.

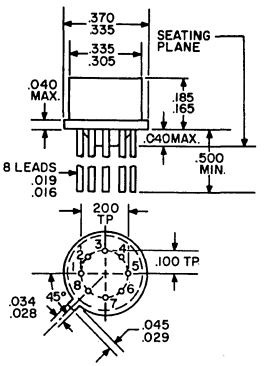
POWER CONSUMPTION — The DC power required to operate the amplifier with no load current.

HIGH PERFORMANCE OPERATIONAL AMPLIFIER

- **No Frequency Compensation Required**
- **Short-Circuit Protection**
- **Offset Voltage Null Capability**
- **Large Common-Mode and Differential Voltage Ranges**
- **Low Power Consumption**
- **No Latch Up**

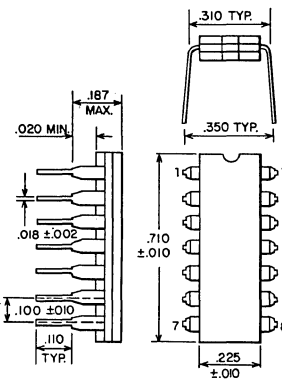
The MICA741 is a high performance monolithic operational amplifier constructed on a single silicon chip, using the ITT Planar epitaxial process. It is intended for a wide range of analog applications. High common mode voltage range and absence of "latch-up" tendencies make the MICA741 ideal for use as a voltage follower. The high gain and wide range of operating voltages provide superior performance in integrator, summing amplifier, and general feedback applications. The MICA741 is short-circuit protected, has the same pin configuration as the popular MICA709 operational amplifier, but requires no external components for frequency compensation. The internal 6dB/ octave roll-off insures stability in closed loop applications.

DIMENSIONS



NOTE: DIMENSIONS AS PER LATEST JS-10 COMMITTEE.
ALL DIMENSIONS IN INCHES.
LEADS ARE GOLD-PLATED KOVAR.
PACKAGE WEIGHT IS 1.22 GRAMS.

DUAL IN-LINE



ABSOLUTE MAXIMUM RATINGS

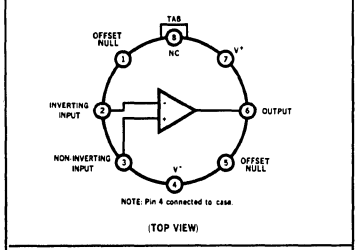
CHARACTERISTICS	MIC741-1	MIC741-5	UNITS
Supply Voltage	±22	±18	V
Internal Power Dissipation	500 (Note 1)	500	mW
Differential Input Voltage	±30	±30	V
Input Voltage (Note 2)	±15	±15	V
Storage Temperature Range	−65 to +150	−65 to +150	°C
Operating Temperature Range	−55 to +125	0 to +70	°C
Lead Temperature (Soldering, 60 sec)	300	300	°C
Output Short-Circuit Duration	Indefinite (Note 3)	Indefinite (Note)	

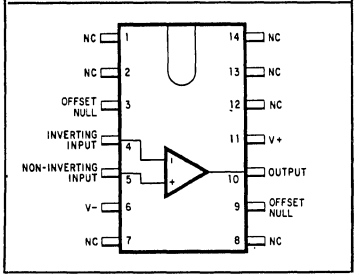
NOTES:
(1) Rating applies for case temperatures to 125°C; derate linearly at 6.5 mW/°C for ambient temperatures above +75°C.
(2) For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
(3) Short circuit may be to ground or either supply. Rating applies to +125°C case temperature or +75°C ambient temperature.
( ) Short circuit may be to ground or either supply.

ELECTRICAL CHARACTERISTICS for MIC 741-1 ($V_S = \pm 15V$, $T_A = 25°C$ unless otherwise specified)

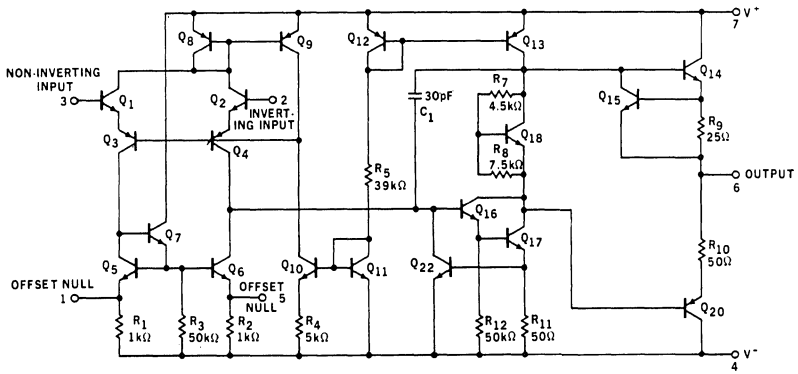
PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
Input Offset Voltage		1.0	5.0	mV	R_S 10kΩ
Input Offset Current		30	200	nA	
Input Bias Current		200	500	nA	
Input Resistance	0.3	1.0		MΩ	
Large-Signal Voltage Gain	50,000	200,000			$R_L \geq 2k\Omega$, $V_{out} = \pm 10V$
Output Voltage Swing	±12 ±10	±14 ±13		V V	$R_L \geq 10k\Omega$ $R_L \geq 2k\Omega$
Input Voltage Range	±12	±13		V	
Common Mode Rejection Ratio	70	90		dB	$R_S \leq 10k\Omega$
Supply Voltage Rejection Ratio		30	150	μV/V	$R_S \leq 10k\Omega$
Power Consumption		50	85	mW	
Transient Response (unity gain)					$V_{in} = 20mV$, $R_L = 2k\Omega$, $C_L \leq 100pF$
Risetime		0.3	1.0	μs	
Overshoot		5.0	10	%	
Slew Rate (unity gain) (Pulsed)		0.5		V/μs	
The following specifications apply for $-55°C \leq T_A \leq +125°C$:					
Input Offset Voltage			6.0	mV	$R_S \leq 10k\Omega$
Input Offset Current			500	nA	
Input Bias Current			1.5	μA	
Large Signal Voltage Gain	25,000				$R_L \geq 2k\Omega$, $V_{out} = \pm 10V$
Output Voltage Swing	±10			V	$R_L \geq 2k\Omega$

CONNECTION DIAGRAMS





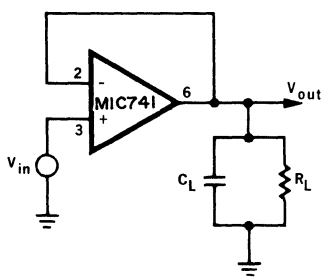
SCHEMATIC DIAGRAM



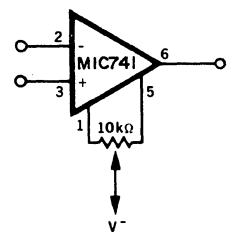
ELECTRICAL CHARACTERISTICS for MIC 741-5 ($V_S = \pm 15V$, $T_A = 25°C$ unless otherwise specified)

PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
Input Offset Voltage		2.0	6.0	mV	$R_S \leq 10k\Omega$
Input Offset Current		30	200	nA	
Input Bias Current		200	500	nA	
Input Resistance	0.3	1.0		MΩ	
Large-Signal Voltage Gain	20,000	100,000			$R_L \geq 2k\Omega$, $V_{out} = \pm 10V$
Output Voltage Swing	± 12 ± 10	± 14 ± 13		V V	$R_L \geq 10k\Omega$ $R_L \geq 2k\Omega$
Input Voltage Range	± 12	± 13		V	
Common Mode Rejection Ratio	70	90		dB	$R_S \leq 10k\Omega$
Supply Voltage Rejection Ratio		30	150	μV/V	$R_S \leq 10k\Omega$
Power Consumption		50	85	mW	
Transient Response (unity gain)					$V_{in} = 20mV$, $R_L = 2k\Omega$, $C_L \leq 100pF$
Risetime		0.3		μs	
Overshoot		5.0		%	
Slew Rate (unity gain)		0.5		V/μs	$R_L \geq 2k\Omega$
The following specifications apply for $0°C \leq 1_A \leq +70°C$:					
Input Offset Voltage			7.5	mV	$R_S \leq 10k\Omega$
Input Offset Current			300	nA	
Input Bias Current			800	nA	
Large-Signal Voltage Gain	15,000				$R_L \geq 2k\Omega$, $V_{out} = \pm 10V$
Output Voltage Swing	± 10			V	$R_L \geq 2k\Omega$

TRANSIENT RESPONSE TEST CIRCUIT

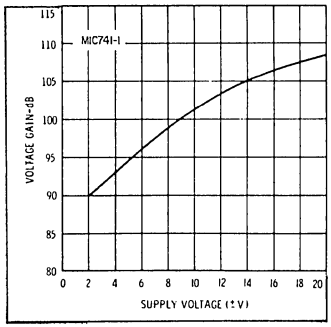


VOLTAGE OFFSET NULL CIRCUIT

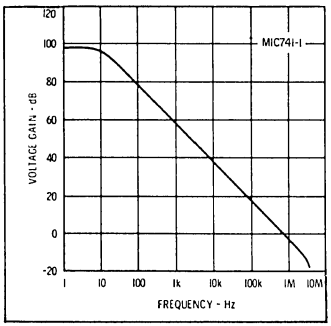


TYPICAL PERFORMANCE CURVES

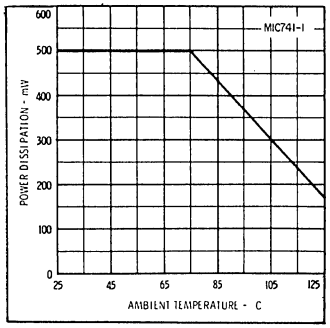
OPEN LOOP
VOLTAGE GAIN



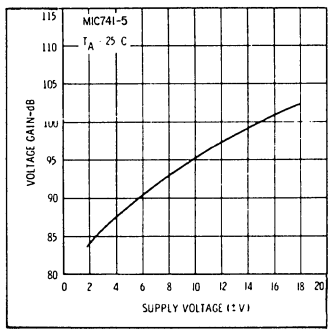
OPEN LOOP
FREQUENCY RESPONSE



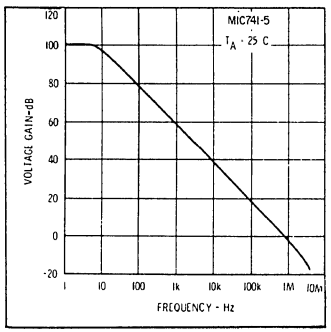
ABSOLUTE MAXIMUM
POWER DISSIPATION



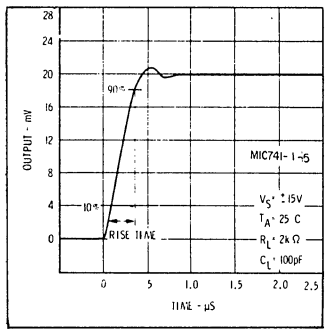
OPEN LOOP
VOLTAGE GAIN



OPEN LOOP
FREQUENCY RESPONSE



TRANSIENT RESPONSE



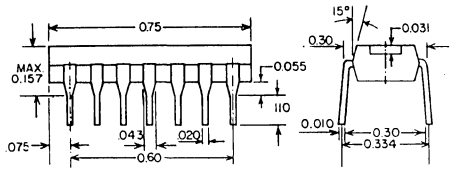
Monolithic integrated circuit in bipolar technique, designed primarily for use in electronic organs. The device incorporates seven flip-flops with externally accessible inputs and outputs.

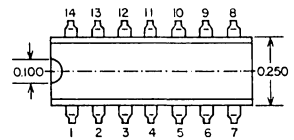
Each flip-flop changes state on application of a positive-going input pulse. The individual flip-flops can be interconnected to form a divider chain. Two flip-flop pairs are already internally series-connected as shown in Fig. 2.

An emitter-follower is interposed between each flip-flop and the associated output terminal to ensure that the output voltage is largely independent of load. Because no internal emitter resistors are provided, the emitter-follower delivers undirectional output currents.

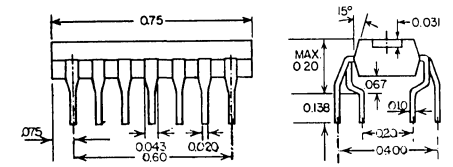
When used in electronic organs the frequency divider SAJ110 may be driven by sine-wave as well as square-wave signals. The shape of the square-wave output signal can be modified by connection of RC filters.

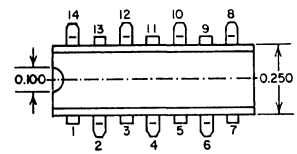
If, by means of an appropriate circuit, all inputs and outputs are brought to a potential below 1.5 volts for a short time, all outputs remain in the low state.





SAJ 110 A

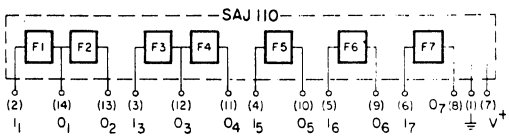




SAJ 110 B

Normally, the SAJ110 is delivered in the dual in-line plastic package TO-116 (Fig. 1a, add suffix "A" to type No.). Upon special request it is also available in the quad in-line package (Fig. 1b, add suffix "B" to type No.).

Block Diagram



The figures in brackets correspond to the pin numbers.

All voltages are referred to terminal 1.

ABSOLUTE MAXIMUM RATINGS

Characteristic			Unit
Supply voltage	V_7	11	V
Input voltage see Fig. 6			
Output current per stage	I_o	5*)	mA
External voltage at output terminals	V_{ext}	±5	V
Ambient temperature range	T_{amb}	−10 . . . +60	°C
Storage temperature range	T_s	−30 . . . +125	°C

Characteristics per Divider Stage

at V_7 = 9 V, R_L = 2.2 kΩ, T_{amb} = 25°C

Characteristic			Unit
Supply current (low state at output)	I	< 3	mA
Input voltage high state (see Fig. 6)	V_i	6 . . . 9	V
Input voltage low state	V_i	< 1	V
Output voltage low state	V_o	< 0.1	V
Output voltage high state	V_o	> 7.0	V
Rise time of output voltage	t_r	< 0.2	μs
Fall time of output voltage	t_f	< 0.2	μs
Input resistance (see Fig. 7)	r_i	6 . . . 9	kΩ

Characteristics per Divider Stage
at V_7 = 9 V, R_L = 2.2 kΩ, T_{amb} = 25°C

Characteristic			Unit
Output resistance low state	r_o	> 1	MΩ
Output resistance high state	r_o	200	Ω

*) During resetting in accordance with Figs. 4 and 6 this value may be exceeded for a time less than 0.1 ms.

Recommended Operating Conditions			
Supply voltage	V_7	9	V
Max. input frequency	f_{imax}	50	kHz
Load resistance	R_L	2 . . . 20	kΩ

If the output voltage shape has to be modified for applications in electronic organs (see Fig. 3), a protective resistor R_S = 180 Ω, connected in series with the capacitor C_L, should be used. In this case the condition $R_L >> R_S$ must be met.

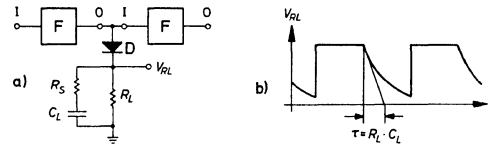


Fig. 3: Modification of the square-wave output voltage using RC networks.
a) Circuit diagram, D = Decoupling diode, e. g. BA 170
b) Shape of output voltage V_{RL}

On application in counter circuits resetting may be required. This can be accomplished by bringing all outputs to a potential less than 3 Volts with the inputs kept on 0 Volt as shown in Fig. 8, or more conveniently by bringing all imputs and outputs to a potential less than 1.5 Volts. The active edge of the reset pulse has to be fast enough to complete the resetting within less than 0.1 ms, otherwise the device may be overloaded. Fig. 4 shows a recommended circuit for resetting.

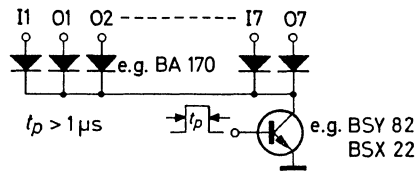


Fig. 4: Recommended reset circuit for counting applications.

Fig. 5:
Output voltage versus supply voltage.

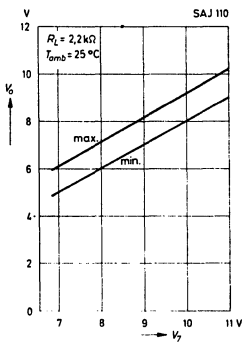


Fig. 6: Max. admissible and min. required value of input pulses (high state) versus supply voltage.

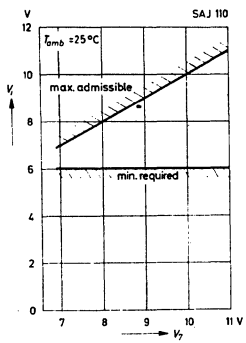


Fig. 7:
Input characteristic

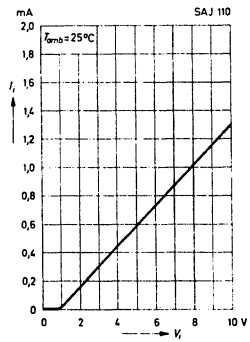
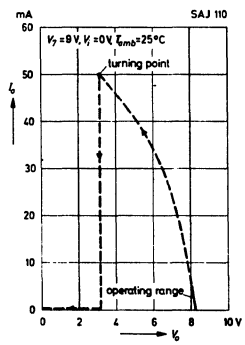


Fig. 8:
Output characteristic



SEVEN STAGE FREQUENCY DIVIDER POWER OSCILLATOR

The monolithic integrated circuit SAJ170 is intended for application in quartz-controlled clocks (wall and table models). The device consists of seven series-connected flip-flop stages, triggered by the positive-going edge of the respective input pulse. The SAJ170 may be driven either by sine-wave or by square-wave signals according to Fig. 3a and 3b.

For divisions by the usual factor 2^{14} (e. g. from 16,384 Hz to 1 Hz) it is necessary to use two SAJ170 connected directly in series.

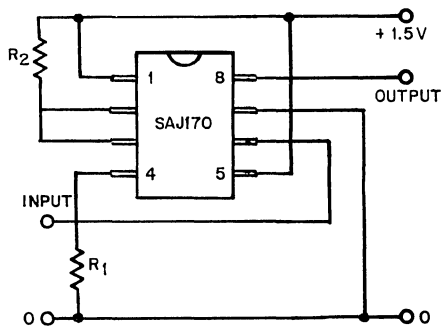


Fig. 1: Operating circuit of SAJ170.

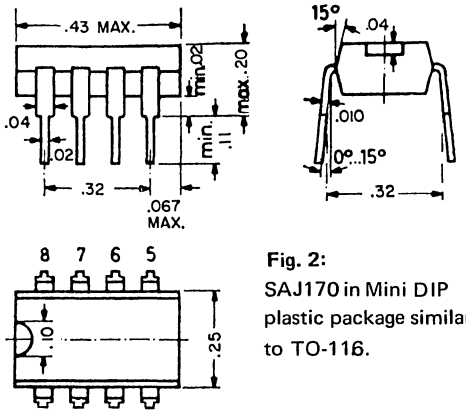


Fig. 2: SAJ170 in Mini DIP plastic package similar to TO-116.

All voltages are referred to terminal 7.

ABSOLUTE MAXIMUM RATINGS

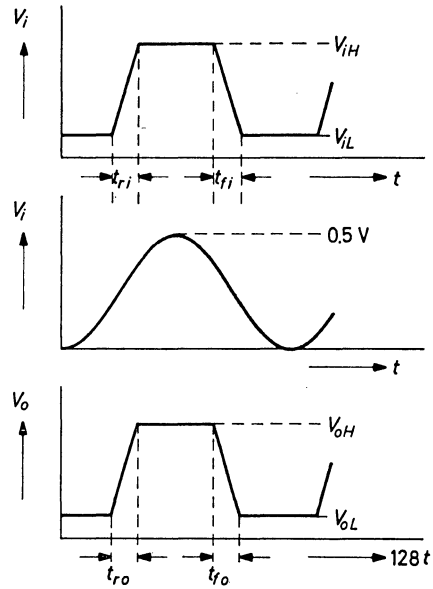
Characteristics	Units
Supply voltage	2 V
Ambient temperature range	-10 . . . +60 °C
Storage temperature range	-30 . . . +125 °C

ELECTRICAL CHARACTERISTICS @ $V_1 = V_5 = 1.5$ V, R1 = 680 kΩ, R2 = 270 kΩ, $T_{amb} = 25°C$

Characteristics			Units
Current consumption	$I_{1+2+3+5}$	17	uA
Divider ratio	f_i/f_o	128	
Output voltage high state	V_{oH}	0.55	V
Output voltage low state	V_{oL}	0.05	V
Rise time of output voltage	t_{ro}	10	us
Fall time of output voltage	t_{fo}	5	us

RECOMMENDED OPERATING CONDITIONS @ $T_{amb} = 25°C$

Characteristics			Units
Supply voltage	V_1, V_5	V1.2	V
Current consumption adjustable by R1	$I_{1+2+3+5}$	10 . . . 25	uA
Resistor for adjusting current consumption	R1	according to Fig. 4	
Input frequency	f_i	V50	kHz
Capacitive load at output	C_8	V30	pF
Input voltage high state	V_{iH}	0.4 . . . 0.6	V
Input voltage low state	V_{iL}	V0.1	V
Rise time of input voltage	t_{ri}	V20	us
Fall time of input voltage	t_{fi}	V10	us



a) Input voltage if driven by square-wave signal

b) Input voltage if driven by sinusoidal signal (only for $f_i > 8$ kHz)

c) Output voltage

Fig. 3: Input and output voltages of SAJ 170

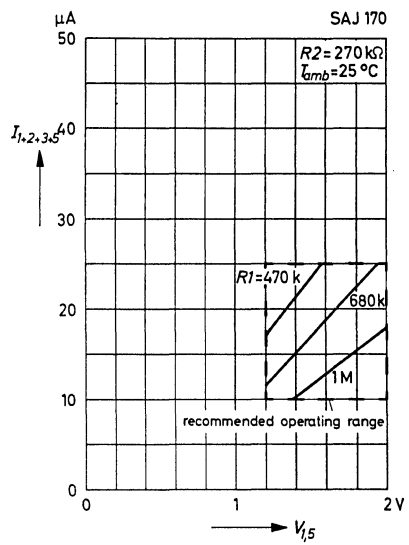


Fig. 4: Current consumption versus supply voltage

The monolithic integrated circuit SAK110 is designed for use in rev-counters of cars.

By use of suitable external circuitry the rev-counter can be adapted to engines with two to eight cylinders. It is designed for a nominal 12 V DC supply.

The heart of the SAK110 is a monostable flip-flop which converts the input signal (which can be derived, for example, directly from the contactbreaker) into square pulses with constant voltage and duration. Using an 8 mA moving-coil instrument it is possible to design a simple frequency meter.

The circuit is so designed that with the use of a suitable instrument the readings will be practically independent of temperature. The push-pull output allows for the use of instruments with high inductance moving coil even at high frequencies. A diode which is parallel to input terminal 2 and 3 prevents triggering by negative pulses.

The SAK110 can be triggered only by pulses exceeding 8 V supplied from a voltage-divider directly connected to contact-baker. Thus good noise immunity is obtained.

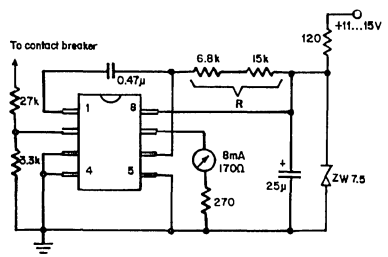


Fig. 1: Circuit diagram of a rev-counter with full scale deflection at 6000 RPM (two control pulses per turn of crank-shaft). Nominal voltage of car battery 12 V.

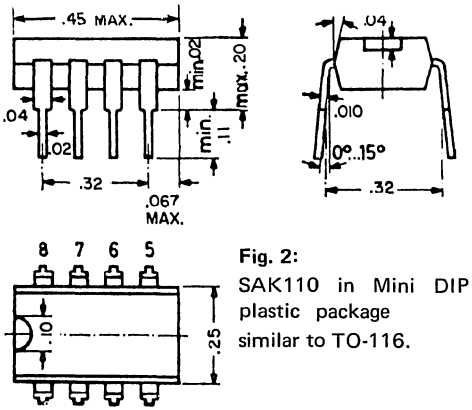


Fig. 2: SAK110 in Mini DIP plastic package similar to TO-116.

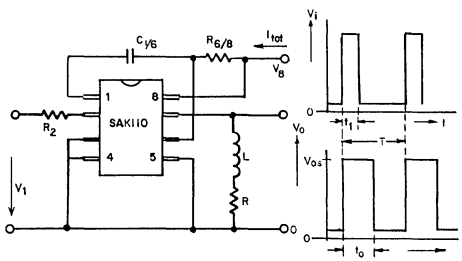


Fig. 3: Test Circuit.

All voltages are referred to terminals 3, 4 and 5.

ABSOLUTE MAXIMUM RATINGS

Characteristics	Units
Supply voltage	9 V
Currents	−20 mA
average value	2 mA
at pulse duration V0.5 ms	20 mA
at pulse duration V0.5 ms	75 mA
at pulse duration V0.5 ms	−75 mA
Ambient temperature range	-25 . . . +65 °C

RECOMMENDED OPERATING CONDITIONS

Characteristics			Units
Supply voltage	V_8	7.5 . . . 8	V
Frequency of input pulses	f_i	<10	kHz
Pulse duty factor of output voltage	t_o/T	<0.85	
Timing resistor	$R_{6/8}$	3 . . . 20	kΩ

TEST CONDITIONS FOR CHARACTERISTICS see test circuit Fig. 3

Characteristics			Units
Supply voltage (± 1 %)	V_8	8	V
Timing resistor (± 0.1 %)	$R_{6/8}$	10	kΩ
Timing capacitor (± 0.1 %)	$C_{1/6}$	0.47	μF
Load resistance (± 0.5 %)	R_L	440	Ω
Load inductance (± 5 %)	L	80	mH
Series resistance at input (± 1 %)	R_2	10	kΩ
Voltage amplitude of input pulses (± 2 %)	V_{is}	10	V
Duration of input pulses (± 5 %)	t_i	0.5	ms
Frequency of input pulses (± 0.1 %)	f_i	250	Hz

CHARACTERISTICS AT T_{amb} = 25°C. See preceding test conditions

Supply current at V_i = 0	I_{tot}	12 . . . 22	mA
Input voltage drop	$V_{2/3}$	6.5 . . . 8	V
Duration of output pulses	t_o	2.7 . . . 3.1	ms
Voltage amplitude of output pulses	V_{os}	5 . . . 5.8	V
Output voltage average vlaue	V_o	3.3 . . . 4.5	V
Change of output voltage for a supply voltage change of ± IV_8 = 0.3 V	$\pm\frac{\Delta V_o}{V_o}$	<2	%
Temperature coefficient of output voltage	a_{V_o}	$< 2 \cdot 10^{-3}$	1/°C
Residual output voltage	$V_{o\ res}$	<30	mV

At input frequencies in the range of f_i = 25 . . . 250 hZ:

Dependence of output voltage on the frequency $V_{o\ lin} = \frac{V_{o\ max} - V_{o\ res}}{f_{i\ max}} \cdot f_i + V_{o\ res}$

Deflection linearity error $\left|\frac{V_o - V_{o\ lin}}{V_{o\ max}}\right| < 0.3\ \%$

Definitions:

V_o = actual value of output voltage (average value)

$V_{o\ lin}$ = nominal value of output voltage

$V_{o\ max}$ = final value of output voltage at $f_i = f_{i\ max}$ = 250 Hz (full scale deflection)

The duration of the input pulses must always be shorter than the duration of the output pulses.

POWER OSCILLATOR

Monolithic integrated circuit in bipolar technique. Particularly suited as electronic pulse generator for direction blinker and emergency blinker in cars with 12V DC supply. Also suited for other applications, e.g. for interval wind-screen wipers.

The TAA 775 G is an oscillator, the frequency of which is determined by an external RC network and which supplies rectangular output pulses. The output terminal 10 is connected to the collector of the output transistor operating in common emitter configuration. An integrated diode between the collector of the output transistor and the supply voltage terminal 1 allows for operation with inductive loads.

As can be seen from the terminal diagram Fig. 1, the TAA 775 G has two oscillator input terminals 5 and 6, for the connection of the frequency-determining RC network. By applying a suitable control voltage to the control input (terminal 7) the following operating modes are possible (see Fig. 5):

a) Operation at nominal frequency f_o

b) Operation at increased frequency f'_o

c) Oscillator not oscillating

When a control voltage for operating mode a) or b) is applied, oscillation starts in the on-state. Since the control voltage is effective only during the off-state, blocking of the oscillator in the on-state is possible only at the end of the normal on-state.

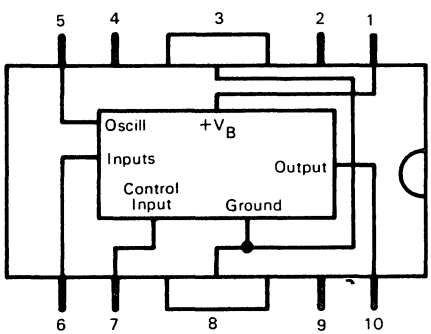
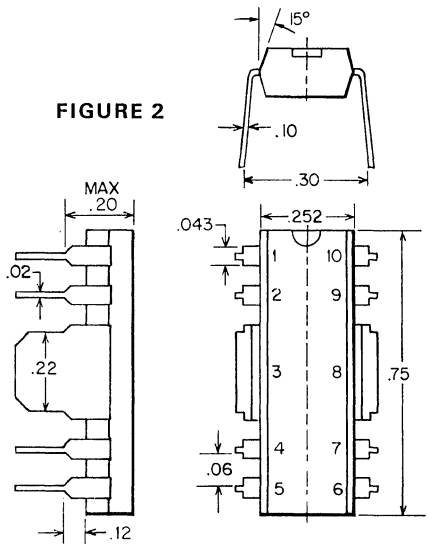


FIGURE 1 – TERMINAL DIAGRAM OF TAA 775 G

The TAA 775 G is supplied in a modified dual in-line plastic package. Instead of the three central connection pins a connection fin of suitable width serving as ground terminal is lead out on both sides (see Fig. 2).

FIGURE 2



ABSOLUTE MAXIMUM RATINGS

Characteristics	Unit
Supply Voltage	15 Volts
Control Voltage	$<V_1$
External Voltage on Terminal 10	$<V_1$
Output Current	150 mA
Ambient Temperature Range	−25...+85°C

STATIC CHARACTERISTICS @ V_1 = 12 Volts: $V_3 = V_8$ = 0 Volt T_{amb} = 25°C (see Fig. 3)

Characteristics	Unit
Average Current Consumption	8 mA
Leakage Current of the Oscillator Input at V_5 = 0 Volt	<1 μA
Required Oscillator Input Current for Turning on the Oscillator Output	>10 μA
Output Saturation Voltage in the On-State at I_{10} = 110 mA	<1 Volt
Output Leakage Current in the Off-State at $V_{10} = V_1$ and V_5 = 0 Volt or $V_7 = V_1$	<1 μA

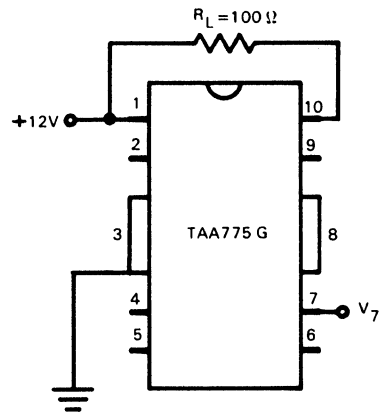


FIGURE 3 — TEST CIRCUIT FOR THE STATIC CHARACTERISTICS

Dynamic Characteristics

at V_1 = 12 Volts, $V_3 = V_8$ = 0 Volt,

T_{amb} = 25°C (see Fig. 4)

Frequency-determining resistor — $R_{5/6}$	1...120	kΩ
Frequency-determining capacitor — C_5	optional, but the leakage current of the capacitor must be taken into consideration.	

Oscillator frequency (see Fig. 5)

at V_7 = 0...0.35 Volt — $f_o = \frac{800}{R_{5/6} \cdot C_5}$ Hz ($R_{5/6}$ in kΩ, C_5 in uF)

at V_7 = 0.45...5 Volts — $f'_o = 2.2\ f_o$

at V_7 = 8 Volts...V_1 — f''_o = 0; output transistor blocked

on/off ratio (see Fig. 5)

at V_7 = 0...0.35 Volt — $t_{on}/t_{off} = 0.8$

at V_7 = 0.45...5 Volts — $t'_{on}/t'_{off} = 1.1$

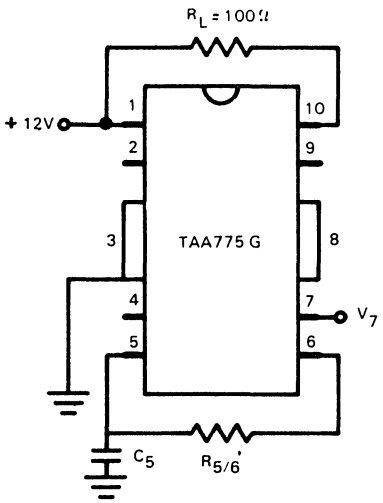
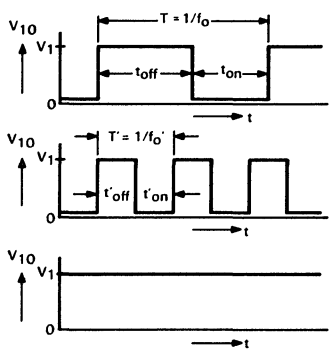


FIGURE 4 – TEST CIRCUIT FOR THE DYNAMIC CHARACTERISTICS



V_7 = 0...0.35 Volt

V_7 = 0.45...5 Volts

V_7 = 8 Volts...V_1

FIGURE 5 – OPERATION OF THE CONTROL INPUT 7 (STEADY STATE)

Application as directional and emergency blinker (see Fig. 6)

In conjunction with a frequency-determining RC network (e.g. $R_{5/6}$ = 5.6 kΩ, C_5 = 100 µF/6 Volts) and a relay (coil resistance min. 100Ω) the TAA 775 G replaces a conventional hot wire interval switch and a current monitoring relay. The previous arrangement of the terminals on the blinker realy package (plus and minus pole of the battery and connection to steering-wheel changeover switch) can be retained. In the case of direction blinking, the bulbs are monitored: the breakdown of a bulb causes a greatly increased blink frequency. The capacitor C_6 prevents battery voltage transients affecting the operation of the TAA 775 G.

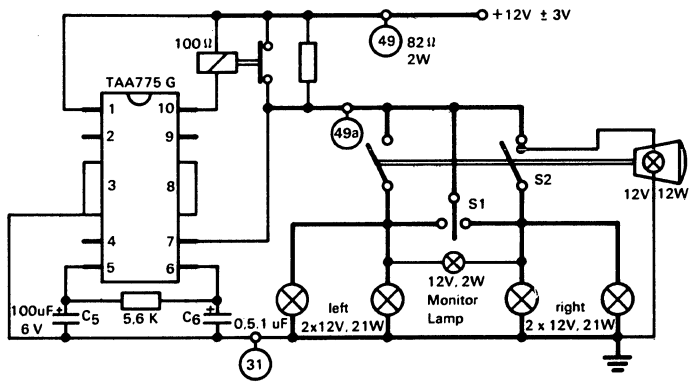


FIGURE 6 – CIRCUITRY OF A DIRECTION AND EMERGENCY BLINKER USING INTEGRATED CIRCUIT TAA 775 G

S 1: Direction blinking
S 2: Emergency blinking

Characteristics of Blinker Circuit

At V_1 = 12 Volts, T_{amb} = 25°C, as in Circuit Fig. 6

Operation starts with a bright interval			
Duration of the first bright interval	t	<1	Sec
Nom. frequency in normal operating with two 21 Watt bulbs	f_o	85	Min^{-1}
Nom. frequency in emergency operation with four 21 Watt bulbs	f_o	85	Min^{-1}
Ratio of on-time to total period at nom. frequency	ν	45	%
Dependence of operating frequency on the supply voltage in the range of 9 to 15 Volts	$\pm\Delta f_o/f_o$	<2	%
Control of the lamps:			
Defect in one of the two direction indicating lamps causes an increase of the blink frequency by the factor	$\Delta f_o'/f_o$	2.2	–
Ratio of on-time to total period in the case of increased frequency	ν'	52	%

Other applications

The frequency and the on/off ratio of the output voltage can be varied within a wide range by variation of the time-determining RC network. For the charging resistor R_a and the discharging resistor R_e the following conditions must be met:

$$1\ k\Omega < R_a < 120\ k\Omega$$

$$1\ k\Omega < R_e < 120\ k\Omega$$

The TAA 775 G can be used for frequencies up to 20 kHz. The approximate equations given below are, however, only valid for frequencies up to 4 kHz. Fig. 7 gives the output voltage wave form with load resistor connected.

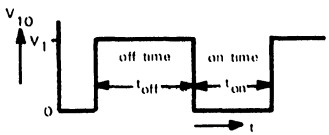


FIGURE 7 – BEHAVIOR OF THE OUTPUT VOLTAGE AS A FUNCTION OF TIME

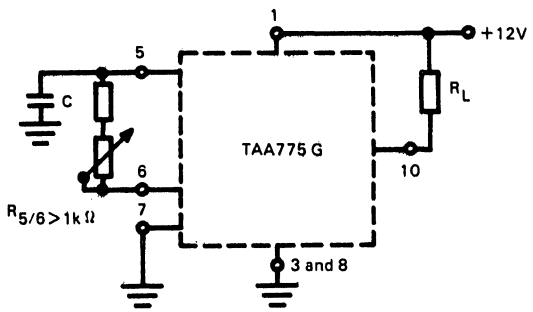
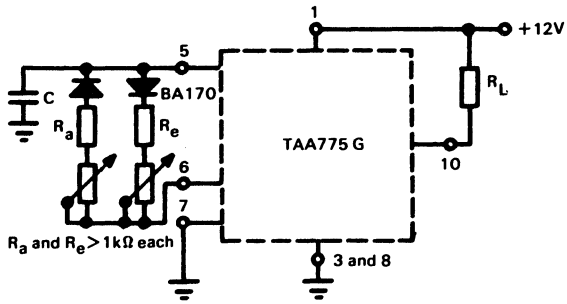


FIGURE 8 – AS PULSE GENERATOR WITH ADJUSTABLE FREQUENCY AND CONSTANT ON/OFF RATIO. CHARGING AND DISCHARGING OF THE TIME-DETERMINING CAPACITOR THROUGH THE SAME RESISTOR

For the circuit in Fig. 8 these equations are valid:

$$T = 1/f_o = \frac{R \cdot C}{800}\ \text{sec} \quad \begin{matrix} R \text{ in } k\Omega \\ C \text{ in } \mu F \end{matrix}$$

$$t_{on} = 0.45\ T$$
$$t_{off} = 0.55\ T$$

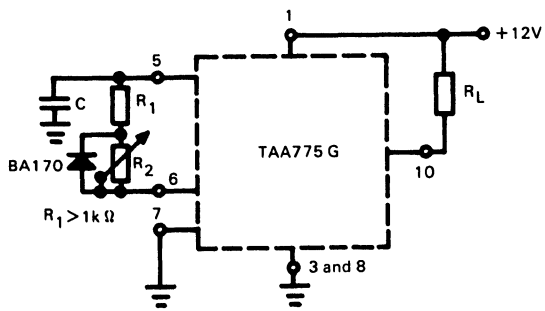


For the circuit in Fig. 9 these equations are valid:

$t_{on} = 0.7 \cdot C \cdot R_e$ msec R in kΩ

$t_{off} = C \cdot R_a$ msec C in μF

FIGURE 9 – AS PULSE GENERATOR WITH ADJUSTABLE FREQUENCY AND ADJUSTABLE ON/OFF RATIO. CHARGING AND DISCHARGING OF THE TIME-DETERMINING CAPACITOR IS EFFECTED THROUGH SEPARATE RESISTORS.

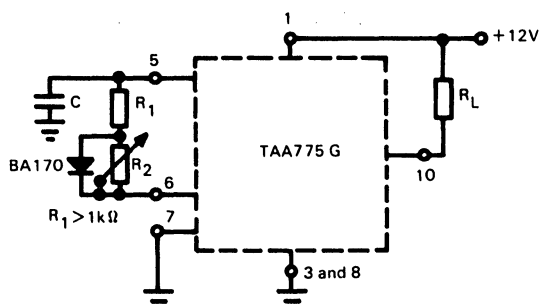


For the circuit in Fig. 10 these equations are valid:

$t_{on} = 0.6 \cdot C \cdot (R_1 + R_2)$ msec R in kΩ

$t_{off} = C \cdot R_1$ msec C in μF

FIGURE 10 – AS PULSE GENERATOR WITH ADJUSTABLE ON-TIME



For the circuit in Fig. 11 these equations are valid:

$t_{on} = 0.7 \cdot C \cdot R_1$ msec R in kΩ

$t_{off} = 0.75 \cdot C \cdot (R_1 + R_2)$ msec C in μF

FIGURE 11 – AS PULSE GENERATOR WITH ADJUSTABLE OFF-TIME

WIND-SHIELD WIPER

The interval wind-shield wiper circuit is shown in circuit Fig. 12. The pause duration between two consecutive wiping operations can be continously adjusted.

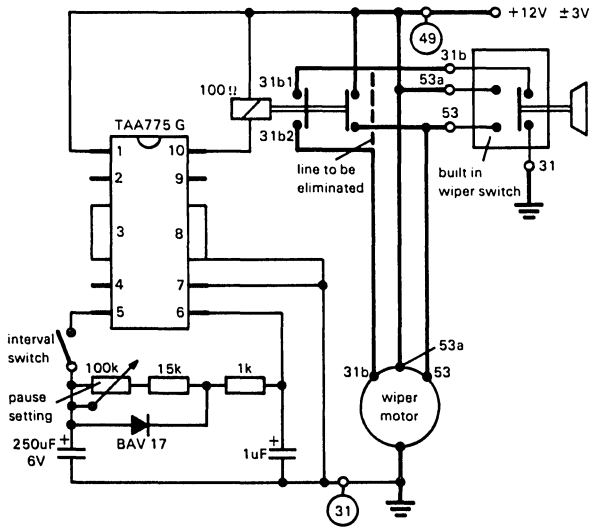


FIGURE 12 – CIRCUIT OF AN INTERVAL WIND-SHIELD WIPER USING TAA 775 G.

Characteristics of the circuit in Fig. 12

At V_1 = 12 Volts, T_{amb} = 25°C

On-time (constant) ..... 0.2 sec
Off-time (adjustable) ..... 4 to 20 sec

1.1V Stabilizing Circuit

Monolithic integrated circuit, e.g. for the stabilization of the operating point in transistor circuits and for the voltage-stabilized drive of clocks. The circuit comprises the operating transistor T1 (see fig. 2) and a control circuit for the stabilization of the output voltage $V_{3/4}$ to 1.1V.

Normally the TAA 780 is delivered with vertical leads (Fig. 1a, add suffix "A" to the type No.). Upon special request it is also available with horizontal leads (Fig. 1b, add suffix "B" to the type No.).

Fig. 1a: TAA 780 "A"
Plastic package
"Pancake"

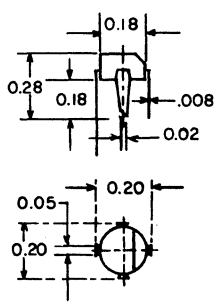
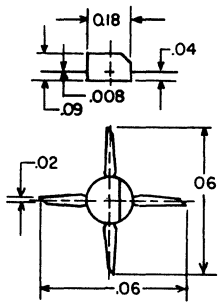


Fig. 1b: TAA 780 "B"
Plastic package
"Pancake"



All characteristics and maximum ratings indicated below refer to the test circuit (Fig. 2) shown below. The figure 0 in the index of some characteristics means that in this case all other terminals are open.

The following definitions apply:

$$S_{V3/4} = \frac{\Delta V_{2/4} \cdot V_{3/4}}{\Delta V_{3/4} \cdot V_{2/4}} \text{ and } \alpha_{V3/4} = \frac{\Delta V_{3/4}}{V_{3/4} \cdot \Delta T_{amb}}$$

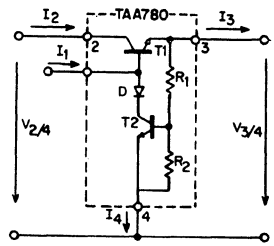


Fig. 2: Circuit Diagram and Test Circuit
T1 ..... Operating transistor
T2 ..... Regulation transistor
D ..... Blocking diode
R1, R2 ..... Voltage divider

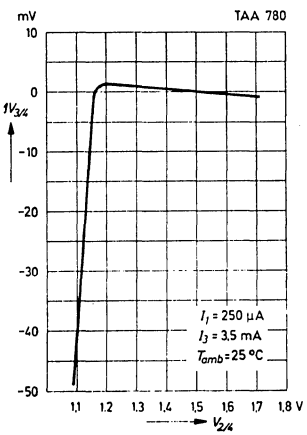
ABSOLUTE MAXIMUM RATINGS

Characteristics	Unit
Collector-Base Voltage	3 Volts
Collector-Emitter Voltage @$R_{1/3}$ = 5 k ohms (ext. connected)	2 Volts
Emitter-Base Voltage	2 Volts
Substrate-Base Voltage	2 Volts
Collector Current	15 mA
Stabilizing Current	1 mA
Ambient Temperature Range	−20 to +40°C
Storage Temperature Range	−20 to 125°C

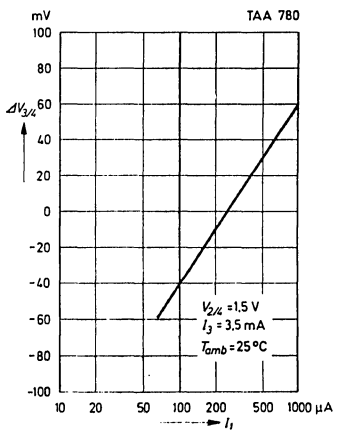
ELECTRICAL CHARACTERISTICS @ $T_{amb}=25°C$ **UNITS**

DC Current Gain of Transistor T1
@ $V_{2/3}$ = 1.5V, I_2 = 0.3 mA, I_4 = 0 ..... 250(> 120)
Collector-Saturation Voltage of Transistor T1
@ I_2 = 3.5 mA, I_1 = 35 µA, I_4 = 0 ..... 0.1 (> 0.12) Volt
Base-Saturation Voltage of Transistor T1
@ I_2 = 3.5 mA, I_1 = 35 µA, I_4 = 0 ..... 0.7 Volt
Total Resistance of Voltage Divider ..... 15 (> 10) k ohms
Stabilized Voltage
@ $V_{2/4}$ = 1.5V, I_1 = 250 µA, I_3 = 3.5 mA ..... 1.1±0.06 Volt
Voltage Stabilization Coefficient
@ $V_{2.4}$ = 1.3 to 1.7V, I_1 = 250 µA, I_3 = 3.5 mA ..... −200
Temperature Coefficient of the Stabilized Voltage
@ $V_{2/4}$ = 1.5V, I_1 = 250 µA, I_3 = 3.5 mA ..... $-2.8 \cdot 10^{-3}/°C$
Small Signal Current Gain of Transistor T1
@ $V_{2/3}$ = 1.5V, I_2 = 0.3 mA, I_4 = 0 250

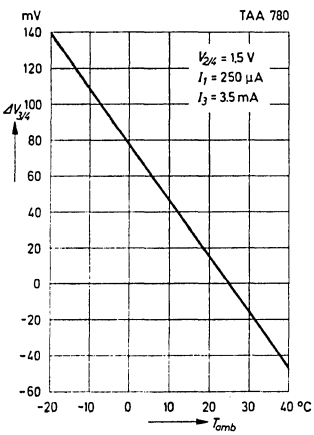
Variation of output voltage $V_{3/4}$ versus input voltage $V_{2/4}$, referred to $V_{2/4}=1.5$ V, $V_{3/4}=1.1$ V



Variation of output voltage $V_{3/4}$ versus current I_1 referred to $I_1=250$ µA, $V_{3/4}=1.1$ V



Variation of output voltage $V_{3/4}$ versus ambient temperature referred to T_{amb} = 25°C, $V_{3/4}$ = 1.1 V



MULTI-FUNCTION IC FOR TV RECIEVERS

- **Sync Separator**
- **A F C**
- **Horizontal Oscillator**
- **A P C**
- **Noise Suppression**

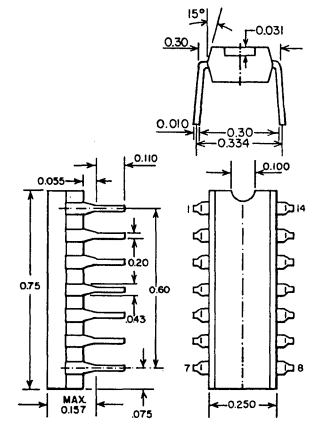
MAXIMUM RATINGS @ 25°C Case Temperature

CHARACTERISTICS		UNITS
Ambient temperature	T_u	0 . . . 60°C
Junction temperature	T_j	< 125°C
Currents: power supply	I_{13}	< 10 mA
signal inputs	I_8	< 1 mA
signal inputs	I_9	< 1 mA
signal inputs	I_3	< 5 mA
signal outputs	I_1	< 10 mA
signal outputs	I_7	< 10 mA
Voltages: supply voltage	V_2	< 10 mA
composite video signal	V_P	0 to < +6 V

ELECTRICAL CHARACTERISTICS @ 25°C Case Temp.

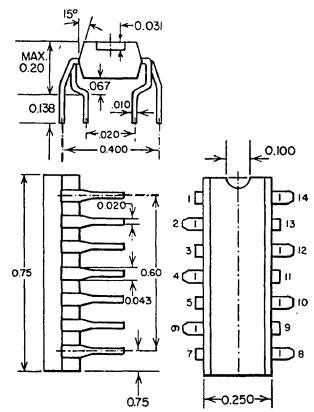
CHARACTERISTICS		UNITS
Input current of the synch separator stage, connection (9)		$+20\ \mu A < I_9 > +1$ mA
Input current of the noise suppressor, connection (8)		$-100\ \mu A < I_8 > -1$ mA $R_{2\text{-}8} \approx 27$ kΩ
Output current of the synch separator, connection (7)		I_7 6 mA
Load resistance		$R_{2\text{-}7}$ 1 kΩ
Amplitude of the line synch and frame pulse at output 7		V_7 +6 V
Nominal frequency of the oscillator		15750 Hz
Output of the oscillator:	Pulse current	I_1 3 mA
	Load resistor	$R_{1\text{-}14}$ 2 kΩ
	Amplitude	V_1 +2 V
	Pulse width	t_1 14 μs
Pull-in range		> ± 1 kHz
Hold-in range		> ± 2 kHz
Slope of the AFC-circuit		> 1 kHz/0.5 μs
Phase shift between oscillator output pulse and synch pulse (defined as the time between the leading edges of these pulses with the oscillator aligned to the nominal frequency).		$t_0 = 1.2\ \mu s$

PHYSICAL DIMENSIONS



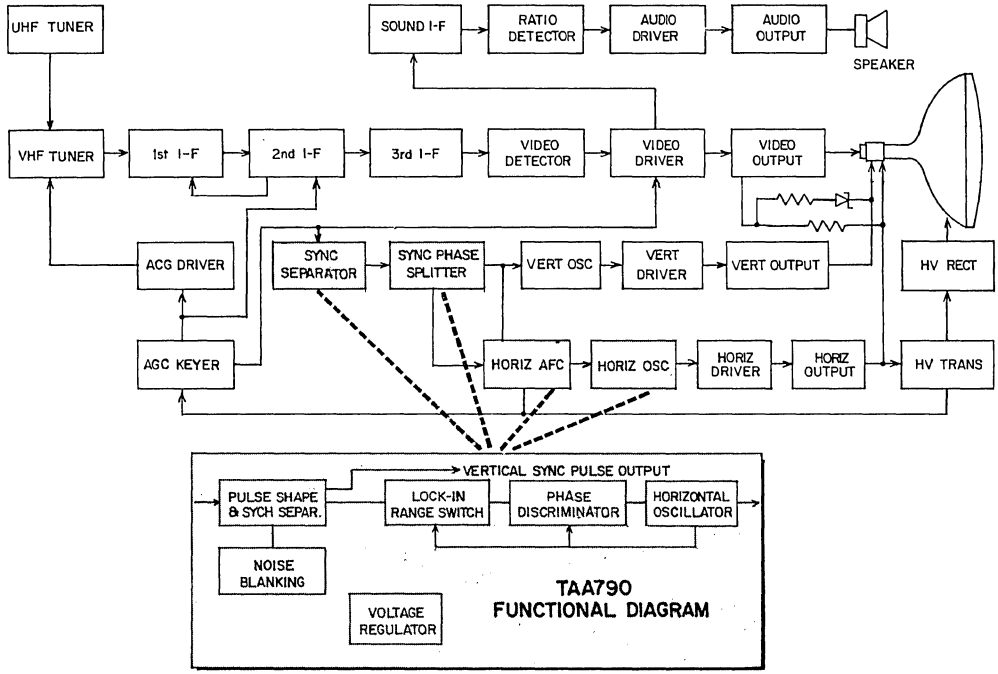
DUAL IN-LINE

PHYSICAL DIMENSIONS

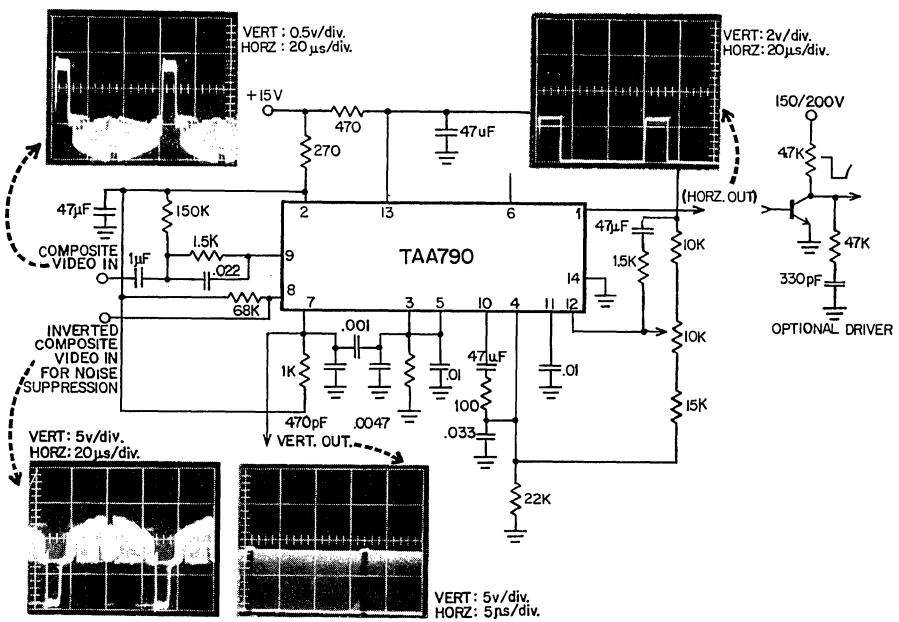


QUAD IN-LINE

BLOCK DIAGRAM OF A TELEVISION RECIEVER



NECESSARY EXTERNAL COMPONENTS



TBA120S

INTEGRATED FM/IF AMPLIFIER AND DEMODULATOR

Package: TO-116
Quad in-line

The monolithic integrated FM/IF amplifier TBA 120 S is designed specifically for use in the sound IF part of television receivers and the FM/IF part of radio receivers. It comprises a broadband symmetrical amplifier and a coincidence circuit for the demodulation. For the volume control, a potentiometer may be connected between terminal 5 and ground. Since the potentiometer carries DC only, the leads to and from the potentiometer will not be affected by hum; remote operation thus presents no difficulty.

Gain is 70 dB and AM rejection ratio 65 dB. The TBA 120 S has excellent limiting properties, and needs only very few external components. The frequency characteristic of the demodulator curve shows excellent stability. The permitted supply voltage range is 5...15V.

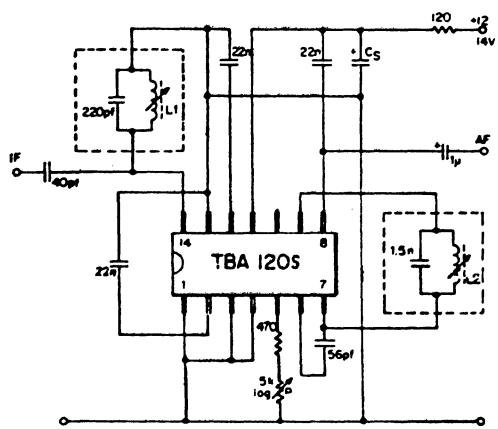
Terminal 3 is the collector and terminal 4 the base of an additional transistor suitable for use as an AF preamplifier or as a switching transistor for treble cut by means of an RC combination. An internal 12 V Zener diode connected to terminal 12 may be used for stabilizing of the supply voltage for the TBA 120 S or for other stages. Max. Zener current 10 mA.

ABSOLUTE MAXIMUM RATINGS

Characteristics	Unit
Supply voltage	15 Volts
Ambient temperature range	−15...+70°C
Storage temperature range	−35...+125°C

The 22 nF filtering capacitor between terminal 8 and 11, together with the integrated output resistor $R_{8/11}$ = 2.6 kΩ, determines the time-constant of the de-emphasis.

Circuit Diagram 4.5 MHz sound IF amplifier



ELECTRICAL CHARACTERISTICS @ V_{11} = 12 Volts, f_i = 0.5 MHz, P = 5 kΩ, T_{amb} = 25°C

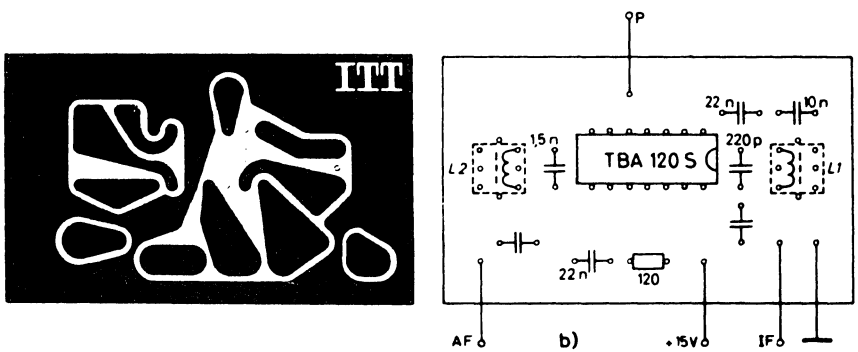
Characteristics	Unit
Recommended range of supply voltage	5...15 Volts
Current consumption	16.5 mA
IF voltage gain	70 dB
Limiting IF output voltage	240 mV
AF output voltage	
@ Δf_i = ± 50 kHz, V_i = 10 mV, f_{AF} = 1 kHz, Q = 45	1.7 Volts
@ Δf_i = ± 25 kHz, V_i = 10 mV, f_{AF} = 1 kHz, Q = 45	0.85 Volt
Distortion	
@ Δf_i = ± 25 kHz, V_i = 10 mV, f_{AF} = 1 kHz, Q = 45	1.8%
Input voltage for start of limitation	
@ Δf_i = ± 50 kHz, f_{AF} = 1 kHz, Q = 45	30 (<60) μV
Input impedance	
@ f_i = 4.5 MHz	20 kΩ parallel to 6 pF
@ f_i = 10.7 MHz	10 kΩ parallel to 5 pF
Output resistance	2.6 kΩ
Volume control range	75 dB
DC level of output signal at V_i = 0	7.3 Volts
AM rejection ratio	
@ Δf_i = ± 50 kHz, V_i = 10 mV, f_{AF} = 1 kHz, m = 30%	65 dB
@ Δf_i = ± 50 kHz, V_i = 200 μV, f_{AF} = 1 kHz, m = 30%	55 dB

Coil data for Circuit Diagram

Coil assemblies: 7mm x 7mm Neosid miniature filters

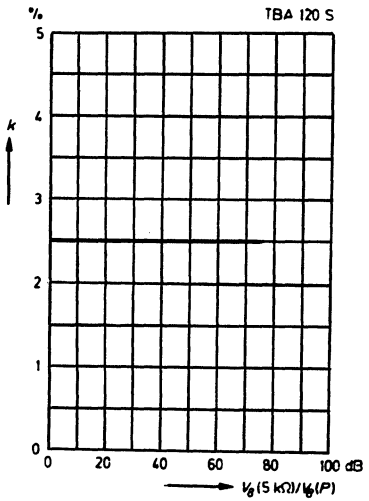
Input coil L1:
12 turns, 0, 1 mm ∅ En. Cu
Material of the core: F 10 B
$Q_0 \approx 80$

Demodulator coil L2:
4 turns, 0, 1 mm ∅ En. Cu
Material of the core: F 2
$Q_0 \approx 45$

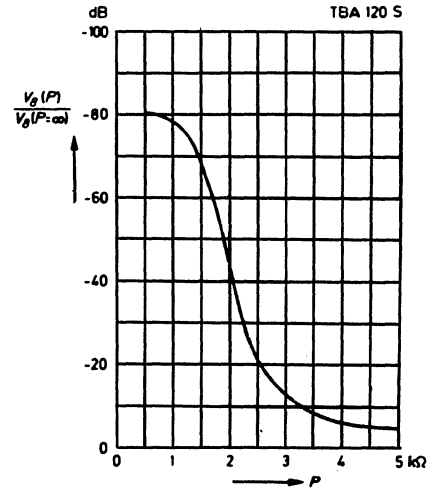


Printed circuit board for circuit diagram, scale 1:1
a) copper foil side b) component side

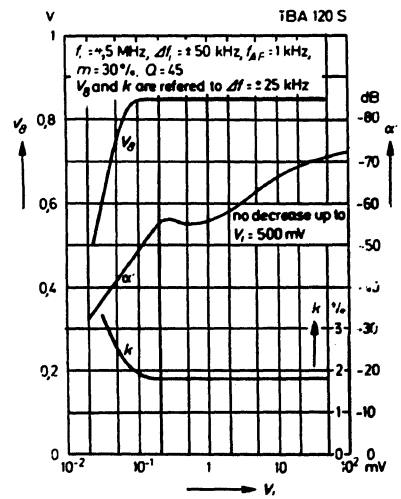
Distortion versus volume control



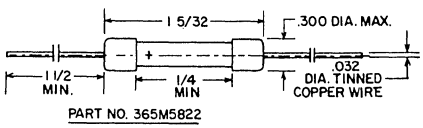
Volume control versus potentiometer resistance



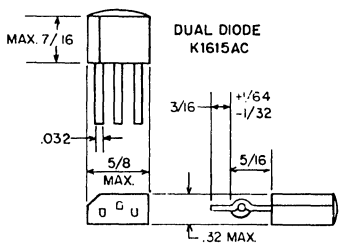
AF output voltage, distortion, and AM rejection ratio versus input voltage

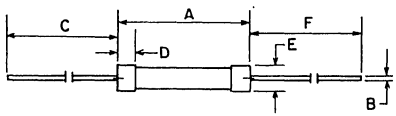


PART NO.	PIV—Based on 16 kHz application	OUTPUT—Tests point	FUNCTION
365M5822	800V	4mA	Color TV Boost Rectifier
K1615AC*	20V	2mA	Horizontal Osc.
034	1200V	4mA	Color TV Boost Rectifier
073	17,250V	3mA	Hi Voltage Rectifier
088	24,000V	3mA	Hi Voltage Rectifier
TV6.5	8,500V	3mA	Focus Rectifier
TV9-6K60	11,700V	3mA	Hi Voltage Rectifier
TV11-6K70	14,650V	3mA	Hi Voltage Rectifier
TV13-11K60	17,250V	3mA	Hi Voltage Rectifier
TV18-10K70	24,000V	3mA	Hi Voltage Rectifier
TV18-10K80	24,000V	3mA	Hi Voltage Rectifier
TV20-10K80	26,500V	3mA	Hi Voltage Rectifier



PART NO. 365M5822





Part No.	A	B	C	D	E	F
034	.820 +.086 -.180	.034 ±.004	.50 MIN.	.168 ±.078	.284 MAX.	.50 MIN.
073	3.345 ±.06	.032 ±.004	.50 MIN.	.236 ±.012	.228 ±.008	——
088	2.785 ±.06	.032 ±.004	.50 MIN.	.158 ±.012	.228 ±.008	——
TV6.5	1.98 ±.06	.03	1.50 ±.04	.236	.23 ±.008	1.50 ±.04
TV9-6K60	2.36 ±.06	.03	1.50 ±.04	.236	.23 ±.008	1.50 ±.04
TVII-6K70	2.76 ±.06	.03	1.50 ±.04	.236	.23 ±.008	1.50 ±.04
TVI3-IIK60	3.35 ±.06	.03	1.50 ±1.50	.236	.23 ±.008	1.50 ±.04
TVI8-IOK70	2.758 ±.06	——	——	.236	.23 ±.008	——
TVI8-IOK80	3.15 ±.06	——	——	.236	.23 ±.008	——
TV20-IOK80	3.15 ±.06	——	——	.236	.23 ±.008	——

SAH215
TELEPHONE PUSH-BUTTON DIALLING IC

MONOLITHIC INTEGRATED CIRCUIT IN MOS TECHNOLOGY FOR USE IN TELEPHONE SETS WHEN DIALLING PUSH-BUTTONS.

- **The off-normal relay is released during the interdigital pause**
- **Decoding by means of ROM gives flexible code**
- **Pulse storage with individual or block-wise recalling of numbers**
- **Two different dial pulse ratios available**
- **Two different inter digital pauses available**

The SAH215 - Design and Operation

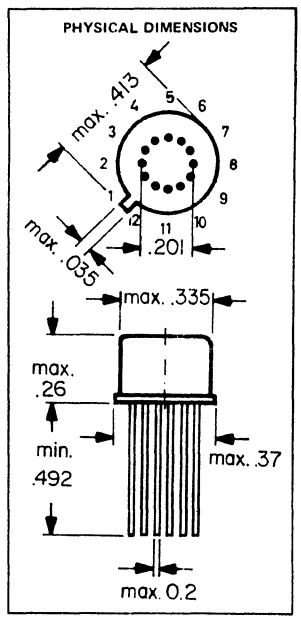
This circuit makes it possible to design push-button dialling telephone sets for connection to conventional telephone networks (quickstep-dialling).

The SAH215 controls a relay the contact of which generates the dialling pulses. It also controls a second relay which performs the function of the o. n. (off-normal) contact, i. e. short-circuits the receiver during the dialling operation. The supply source is a nickel/cadmium accumulator which is charged from the telephone network during conversations. Both relays are driven by the SAH215 through external transistors.

The MOS circuit requires a two-phase clock generator which delivers two non-overlapping clock pulses having an amplitude of approximately - 18 V. Its power consumption can be kept to the extremely low value of less than 4 mW.

Pin Configuration

1 Case, substrate, ground
2 o. n. output
3 d. p. output
4 Reset input
5 Strobe input
6 External register control input
7 Clock t1
8 Clock t2
9 Input A
10 Input B
11 Input C
12 Input D
13 Option t_z (ground-833/ open=433)
14 Option $t_{p/T}$ (ground=0.62/ open=0.66)



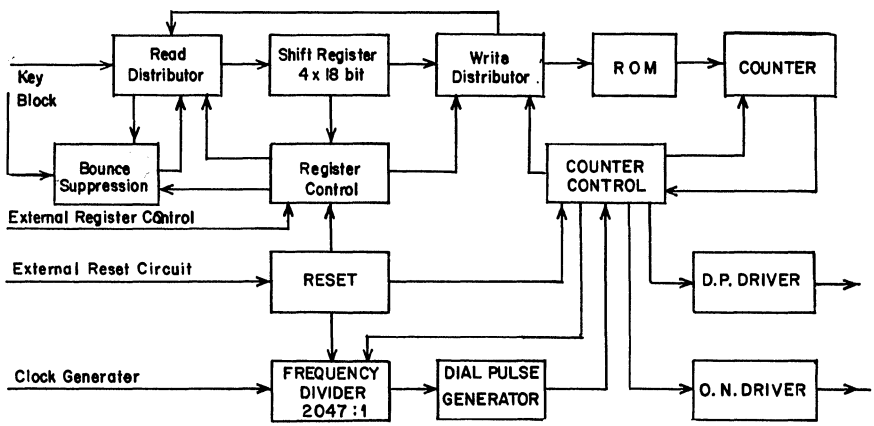


FIG. 1: Block diagram of the SAH215

Fig. 1 shows the block diagram of the SAH215. Four-bit data arriving from the key block are fed in parallel to the shift register via the read distributor. This register consists of four parallel individual registers of 18 bits each and serves for storing a maximum of 18 figures. A bounce-suppression circuit prevents a dialled figure from being written into the register more than once, due to contact bounce in the key block. The register control unit ensures the proper writing and reading sequence.

Through the write distributor the data are taken to a read only memory (ROM) which operates as a decoder and sets a counter in accordance with the entered figure. Through the counter control unit, the dial pulse generator transmits the number of pulses for which the counter was set to the d. p. (dial pulse) driver and drives the d. p. relay, maintaining the proper pulse duty factor. The counter control unit maintains the required interval between the several pulse trains and controls the o. n. relay via the o. n. driver.

The dial pulse generator frequency is derived from the clock frequency by means of a 2047 : 1 frequency divider. For the customary dialling frequency of 10 Hz the required clock frequency is therefore 20.47 kHz.

When applying the supply voltage to the MOS circuit, all stages of the control units have to be reset. This is achieved by a built-in reset unit. The reset time is determined by an external circuit (e. g. an RC-network).

The information in this data sheet relates to "negative logic", i. e. the more negative voltage level (Low) stands for logic "1", and the more positive voltage level (High) for logic "0". The symbol "X" may be an "0" or a "1"

When using a key block in which each key is provided with two ordinary contacts and one positively controlled n. o. (non-overlapping) contact it is possible to control the integrated circuit directly. The same applies to a key block with row and column switches each of which is provided with a common positively controlled n. o. contact. The positively controlled n. o. contacts which close after the other n. o. contacts and open before the other n. o. contacts, control the strobe input 5. Key blocks of different design may be adapted by using a diode matrix. A general requirement for key blocks is that the data signals must be free from bounce prior to the strobe signal as each key is depressed.

Further possibilities of adaptation are introduced by mask variations which enable any desired four-bit code to be set, as long as the tetrades 1111 and 1110 do not occur, because they are needed for register control.

An additional facility

In normal use the terminal 6 is not loaded. This corresponds to a logic "1", if a logic "0" signal is applied to this terminal the register output is blocked and the data made to circulate in the register. In this way, up to 17 figures can be stored. By applying appropriate pulse patterns to terminal 6 individual figures or figure blocks may be recalled. The input of data is not affected by a signal being applied to terminal 6, so that the storage of figures can continue.

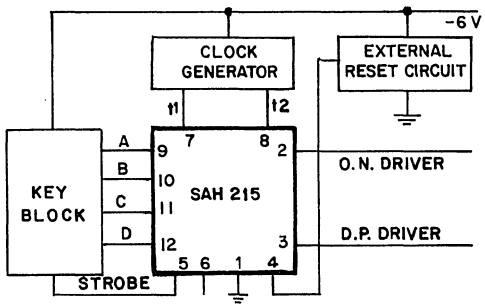


FIG. 2: Block diagram of the general layout

The SAH215 operates with the following code:

Figure	D	C	B	A
1	0	0	0	0
2	0	0	0	1
3	0	0	1	0
4	X	1	0	0
5	0	1	X	1
6	0	1	1	0
7	1	0	0	0
8	1	X	X	1
9	1	0	1	0
0	0	0	1	1

ABSOLUTE MAXIMUM RATINGS

Characteristics			Units
Voltages, clock pulse 1, clock pulse 2	V_7. V_8	-30 . . . +0.3	V
Input voltages Inputs 4, 5, 9, 10, 11 and 12	V_{in}	-30 . . . +0.3	V
Output current	I_2, I_3	-5	mA
Ambient temperature range	T_{amb}	-40 . . . +70	°C

RECOMMENDED OPERATING CONDITIONS

Characteristics			Units
Clock pulse voltages	V_{7M}, V_{8M}	-18	V
Clock frequency	f_t	20 (10 . . . 50)	kHz
Duration of clock pulses	t_t	> 5	*u*s
Time interval between clock pulses 1 and 2	t_a	> 3	*u*s
Reset voltage	$-V_4$	< 3	V
Duration of normalisation pulse	t_4	> 1	ms
Strobe input time (free from bounce)	t_E	> 17	ms
Bounce/strobe pulse spacing	t_B	< 7	ms

Characteristics						Units
at $V_{7M} = V_{8M} = -18$ V, $T_{amb} = 25$ °C						
Input voltages						
Inputs 4, 5, 9, 10, 11 and 12						
Logic "0"	V_{in}			Terminal open		
Logic "1"	V_{in}			-6 (-5 . . . -12)		V
Input 6						
Logic "0"	V_{in}			0 . . . -3		V
Logic "1"	V_{in}			Terminal open		
Input cutoff current at $V_{in} = -12$ V	$-I_R$			< 5		*u*A
Output frequency	f_{out}			$f_t/2047$		
Power consumption	P_{tot}			< 4		mW
Capacitance of clock inputs	C_7, C_8			< 150		pF
	Type:	1	2	3	4	
Dial break ratio of dial pulses	t_p/T	0.66	0.62	0.66	0.62	
Interdigital pause at $f_t = 20$ kHz	t_z	833	838	433	438	ms

ITT SAJ110 IN FREQUENCY DIVIDER CIRCUITS

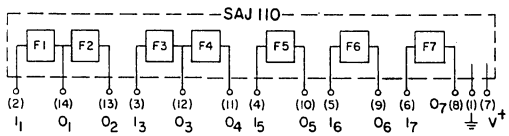
1. Introduction

Integrated digital frequency dividers have for long been widely used in professional digital equipment but have so far found little application in the entertainment sector of the electronic industry. This, no doubt, is due to the fact that the devices presently available do not quite meet the specific requirements of the consumer market, and that they were, until recently, rather expensive. Advances in integration techniques have now made it possible to produce inexpensive linear, as well as digital integrated circuits which should be of special interest to the electronic consumer industry. These devices offer many advantages when compared with circuits employing discrete components and are in many instances already cheaper. It is certain that the availability of these new integrated circuits will lead to rapid new developments in all branches of the electronic industry.

The new monolithic integrated frequency divider circuit SAJ 110, developed by ITT Semiconductors, incorporates seven divider stages which can be used either individually or interconnected to form a divider chain. Because the SAJ 110 requires no additional components and can be used in place of conventional discrete-component flipflop dividers, its use as a frequency divider in electronic organs is particularly advantageous.

2. The Integrated Circuit SAJ 110

Integration of a conventional flipflop circuit would offer virtually no advantage over a discrete component circuit – only a circuit which does not incorporate capacitors or other charge-storing elements is suitable for integration. Because the master slave flipflop (a frequency divider often used in digital equipment) is far too complex for consumer applications, development of a new circuit was necessary. This circuit had to function in a similar manner to a conventional flipflop but had to be designed so that no additional charge-storing elements were required. The result is a device which combines seven single divider stages on a single chip.



SAJ 110 Block diagram—The figures in brackets are the same as the pin numbers of package

In order to make maximum use of the 14 connections available on a TO-116 package the pins are connected as shown in Fig. 1, being arranged so that access to two divider pairs and three single divider stages is possible. The circuits can thus be used either singly or interconnected in various combinations.

Figs. 2a and 2b give dimensioned outline drawings of the SAJ 110 „A" and „B" versions respectively.

2.1. Functional Description of an SAJ110 Divider Stage

Each stage used in the SAJ 110 comprises basically a trigger network, two transistors connected as a flipflop, and an output stage (Fig. 3). The input is first applied to a trigger network which always steers the input pulse to that transistor which is cut off at the time. Fig. 3 shows the input and output waveforms produced by one such stage. Each positive edge of the input waveform causes the flipflop to change state so that frequency division by two results. The flipflop output is fed to a transistor connected as an emitter follower output stage, this being provided to isolate the flipflop from an external load and to supply output pulses of constant amplitude. The output pin is connected to the emitter of this transistor.

2.2. Performance Requirement Summary for the Integrated Frequency Divider SAJ110

The integrated frequency divider had to meet the following customer requirements:

Supply voltage	7 - 11 V
Input (trigger waveforms)	Sinusoid or square wave
Output voltage	Not less than 6 V – high enough to permit reliable triggering of another divider stage under all operating conditions
Permissible load range	2 to 100 kΩ
Ambient operating temperature range	0 to 60°C
Number of stages to be accommodated in one package	7
Packaging	14-pin DIP or QIL plastic package

*Application notes will be found in the last pages of this section.

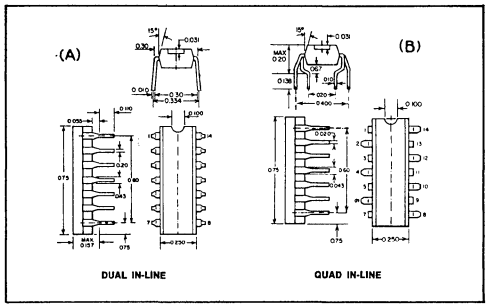


Fig. 2: SAJ 110 Dimensional outline drawings
a) Version "A", TO-116 dual in-line plastic package
b) Version "B", quad in-line plastic package

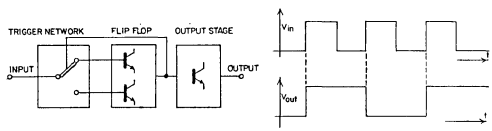


Fig. 3: Block diagram of one divider stage with input and output waveforms

For reason of economy and reliability, it was also considered desirable that the number of integrated elements and the total resistance of all the resistors used in the IC should be kept to a minimum.

2.3. Summary of the Most Important SAJ 110 Data

Maximum ratings

Supply voltage	V_7	11 V
Input voltage	V_{in}	see fig. 4
Output current per stage	I_{out}	5 mA
External output biasing	V_{ext}	± 5 V
Ambient temperature range	T_{amb}	− 0 to +60°C
Storage temperature range	T_{stor}	−30 to +125°C

Single stage characteristics
(@ V_7 = 9 V, R_L = 2.2 kΩ, T_A = 25°C)

Current consumption (output in "low" state)	I	< 3 mA
Input voltage ("high" state)	V_{in}	6 . . . 9 V
Input voltage ("low" state)	V_{in}	< 3 V
Output voltage ("low" state)	V_{out}	< 1.0 V
Output voltage ("high" state)	V_{out}	> 7.0 V
Rise time of output pulse	t_r	< 1.0 µs
Input resistance (see fig. 5)	R_{in}	6 to 9 kΩ
Output resistance ("low" state)	r_{out}	≥ 1 MΩ
Output resistance ("high" state)	r_{out}	< 100 Ω

Recommended Operating Conditions

Supply voltage	V_7	9 V ± 20%
Maximum input frequency	f_{max}	100 kHz
Output load resistor	R_L	2 to 20 kΩ

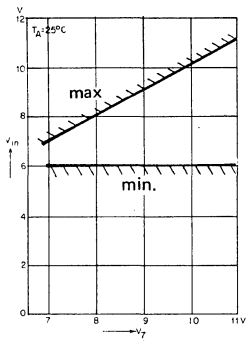


Fig. 4: Maximum permissible input pulse amplitude ("high" state) as a function of supply voltage

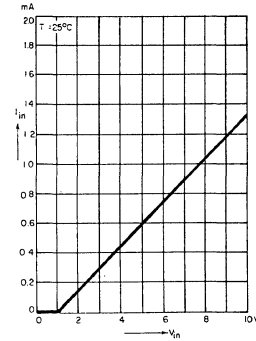


Fig. 5: Input characteristic of a divider stage

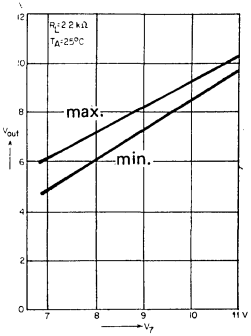


Fig. 6: Output voltage as a function of supply voltage

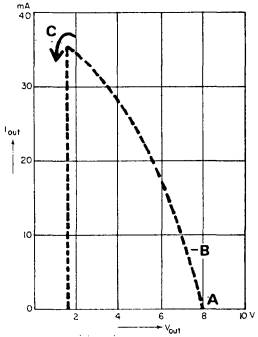


Fig. 7: Output current vs output voltage (pulsed)

The curves shown in Figs. 4 to 7 illustrate the performance of the divider in more detail.

The input parameters of a frequency divider stage at various supply voltages can be deduced from Figs. 4 and 5. The input pulse amplitude should be not less than 6 V, but should, on the other hand, not exceed the supply voltage. The curves in Fig. 4 give the maximum permissible input pulse amplitude range as a function of supply voltage. The input corresponding to "low" level should be less than 1 V. Fig. 5 may be used to determine the static input resistance, which varies between 6 and 9 kΩ.

In the curve shown in Fig. 6 the output voltage is plotted as a function of supply voltage. As can be seen, the output voltage is 1 to 1.5 V lower than the supply voltage and varies somewhat with the load. Assuming the same loading conditions the output voltages of all individual stages are within ±5% − this applies to stages on the same IC as well as to stages on different IC's.

Fig. 7 shows the loading characteristic of a divider stage which gives a "high" output. Note that as the output current of the stage is increased (by reducing the load resistor, for example), point "B" on the curve moves towards "C" (I_{out} = 35 mA and V_{out} = 1.7 V) at which point the stage flips into the "low" state and remains there.

This bistable output effect is discussed further on in connection with the resetting of dividers used in counting circuits.

3. Applications for the SAJ 110

3.1 Use in Electronic Organs

The heart of modern electronic organs is usually a set of LC master oscillators tuned to the frequencies of the highest octave. The frequencies of the lower octaves are then derived from these master oscillators by frequency division. In most conventional organs this frequency division is accomplished by the use of bistable multivibrators (flip-flops). These have the disadvantage of producing a square wave output, which contains practically no even harmonics and offers only limited scope for modifying the character of the notes produced.

However, if the SAJ 110 is used, simple RC networks can be connected across the outputs to generate sawtooth waveforms which contain even harmonics. An additional advantage of the SAJ 110 is its small size, making it particularly suitable for use in portable instruments.

Fig. 8 shows the usual frequency generating circuits employed in electronic organs. Twelve master oscillators produce the frequencies of the highest octave while all the frequencies for the lower octaves are generated by frequency division. The arrangement shown in Fig. 8 requires up to twelve SAJ 110 circuits for one organ. If the organ has less than seven octaves, then there are several spare divider stages which may be utilized in the divider chains associated with other frequencies so that in this case less than 12 integrated circuits are required.

Depression of one of the organ keys, T, causes several outputs to be switched to a common line, S, via high value resistors, R, and this signal, which is a combination of several frequencies, is then further processed. The spectrum of this signal is considerably richer in harmonics than that of an ordinary square wave.

It is an advantage to give a signal to the following filters the mean value of which does little change when the organ keys are pressed. In order to obtain this, the ground of resistor R/10 (Fig. 8) should be connected to a positive potential. Another possibility is to ensure that the divider outputs supply proper AC signals. Fig. 9 shows such an alternative circuit. Use of a suitable bias causes the full alternating divider output component to be developed across the load R_L.

The circuit shown in Fig. 10 fully exploits the high output voltage and low output resistance of the frequency divider SAJ 110. In this circuit RC networks are connected, via protection diodes, to the outputs of individual divider stages so that waveforms which are not very different from that of an ideal sawtooth are presented across the load R_L. The protective resistor R_S connected in series with each capacitor C_L is included to limit the capacitor surge to a value which the output stage can safely handle.

In Fig. 11 the frequency spectrum of the waveform V_{RL} is compared with that of two sawtooth waveforms, and it can be seen that the spectrum attained with the circuit arrangement of Fig. 10 approaches that of an ideal

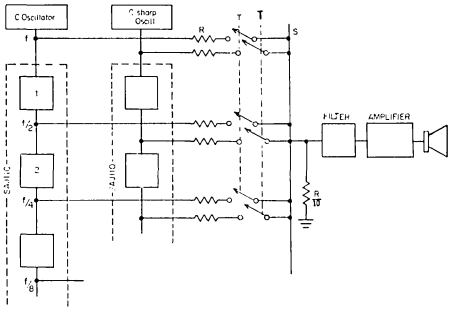


Fig. 8: Block diagram of the tone generating circuits in electronic organs

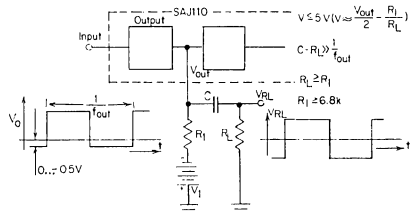


Fig. 9: Conversion of divider unidirectional output into alternating output

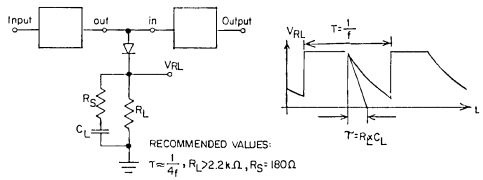


Fig. 10: Modification of the divider frequency spectrum using RC networks

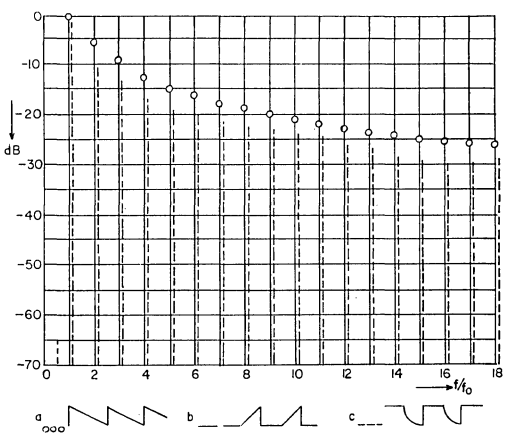


Fig. 11: Frequency spectrum associated with various waveforms

sawtooth. Note that the sub-harmonic component is extremely small – much smaller than is necessary for this application.

3.2. Use of the SAJ 110 in Counting Circuits

Use of the SAJ 110 in a counting circuit raises the problem of how to reset the flipflops. With the SAJ 110 it is possible to reset a single stage as well as several stages connected in a counting chain. However, when designing a suitable reset circuit the following features of the device must be taken into account:

The output of a divider stage can change state only while its input is positive going.

The frequency divider SAJ 110, unlike a master slave flipflop, does not possess a buffer stage between input and output, nor a special reset input.

It is, however, possible to use the inputs and outputs for reset purpose. Because the reset capability of an SAJ 110 stage depends on its input state, it is necessary to use both the input and the output terminals for reset purpose.

3.2.1. Output Characteristic

Referring to the output characteristic of a single stage (Fig. 7) it can be seen that a "high" output can only be flipped to "low" if the output is pulled down to 1.5 V or less by some external means, and this can only be accomo plished while the input voltage V_{in} is "low". The output characteristic in Fig. 7 is divided into the sections A-B and B-C, section A-B being the normal operating range. As mentioned previously, in order to initiate a reset it is necessary to force the output through the range B-C to point "C", and this should be effected in the shortest time possible (t_r < 0.1 msec) to avoid overheating the device (the output transistor dissipates considerable power during this period).

If the divider input potential is higher than 0 V, then the trigger point C is shifted to the left on the curve, which means that the output potential would then have to be pulled down to a level below 1.5 V. If the input and output of a divider stage or if several inputs and outputs of a divider chain are to be pulled down to a low potential together, then this potential should be less than 1.5 V to ensure that the circuits reset reliably under any condition (refer to Fig. 12).

3.2.2. Reset Circuit

Fig. 12 outlines a reset circuit suitable for a seven stage counting chain. All the output points as well as the input point I are connected, via isolating diodes, to the collector of a switching transistor type 2N2218, or alternatively to a RESET switch. It is important that the transistor collector voltage drops to a saturation level of less than 0.6 V for the duration of the reset pulse, and that the transistor is capable of passing up to 400 mA of collector current under the most unfavorable conditions (i.e. when all outputs are in "high" condition prior to the application of a reset pulse). The pulse source must therefore be capable of supplying at lease approximately 15 mA to the base of the 2N2218 so that the requirement $V_{I_1} = V_{O_1} = \ldots V_{O7} < 1.5$ V is fulfilled. The reset pulse duration is, however, not very critical provided it is not less than approximately 1 μ sec.

As mentioned previously, the output state of all the stages depends on the input state of the first stage immediately after the occurrence of the reset pulse. There are two possible conditions:

V_{I_1} = "low" (Fig. 13)

V_{I_1} = "high" (Fig. 14)

In Fig. 13 I_1 was "low" at the instant when the reset was applied; under this condition all the outputs which were in the "high" state immediately before application of the reset pulse change to "low" and maintain this state after the reset pulse has been removed. The next input pulse to I_1 then causes all the outputs to be triggered to "high", this corresponding to a "PRESET" condition of the counter. Only the second input pulse is counted. These conditions are summarized in the truth table in Fig. 13 and it can be seen that the counter counts (n-1).

Fig. 14, on the other hand, illustrates a condition in which all the outputs are in the "PRESET" state immediately after the occurrence of the reset pulse so that the next pulse is correctly counted as No. 1. The explanation for this is as follows: Although in this case the reset pulse initially pulls all the outputs, as well as the input I_1, to "low", the input I_1 is immediately returned to "high" at the end of the pulse ($t = t_1$), because the positive edge at the end of the pulse is equivalent to the application of a logic "H" to the input. This positive edge triggers first output O_1 and then, in turn, all the other outputs to "high" – this corresponding to the "PRESET" state of the counter.

4. Conclusion

The SAJ 110 is an inexpensive seven-stage frequency divider which, in comparison with equivalent discrete-component circuits, offers many advantages, the most important ones being: small size and low wiring and assembly cost. The device, because of its electrical characteristics, is particularly suitable for use in electronic organs where its performance is superior to that of discrete component flipflops. Being insensitive to the waveform of the input signal, the SAJ 110 will accept a square wave as well as other types of waveforms (e.g. sinusoids); moreover, the low output impedance ensures that the output remains virtually constant irrespective of load, the lowest permissible load being approximately 2 kΩ. At maximum loading the output amplitude is only 1.5 V less than supply voltage.

The generation of output waveforms which are very similar to, and possess virtually the same frequency spectrum as, that of an ideal sawtooth, is possible simply by connection of RC networks across the outputs.

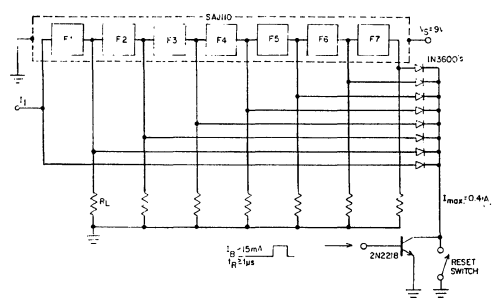


Fig. 12: Reset circuit for a seven stage counter

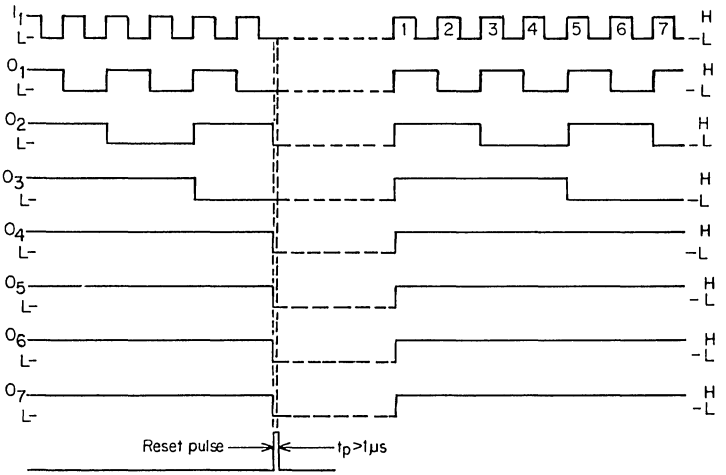


Fig. 13: Reset action at V_{I_1} = "low"

TRUTH TABLE

I_1	O_1	O_2	O_3	O_4	O_5	O_6	O_7
0	L	L	L	L	L	L	L
1	H	H	H	H	H	H	H
2	L	H	H	H	H	H	H
3	H	L	H	H	H	H	H
4	L	L	H	H	H	H	H
5	H	H	L	H	H	H	H
6	L	H	L	H	H	H	H
7	H	L	L	H	H	H	H

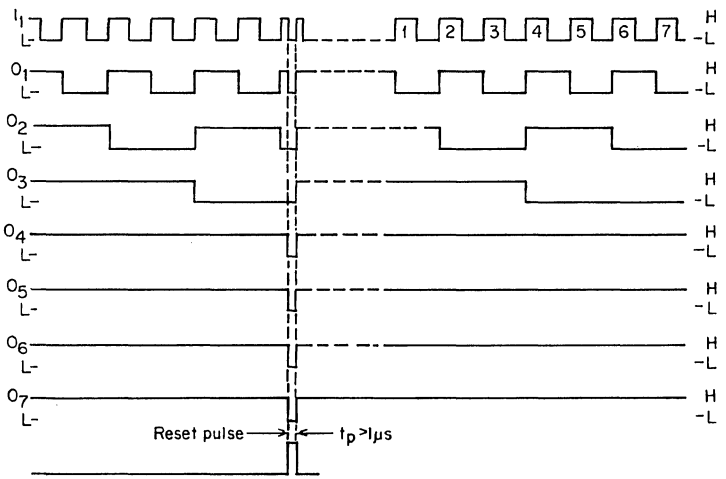


Fig. 14: Reset action at V_{I_1} = "high"

TRUTH TABLE

I_1	O_1	O_2	O_3	O_4	O_5	O_6	O_7
0	H	H	H	H	H	H	H
1	L	H	H	H	H	H	H
2	H	L	H	H	H	H	H
3	L	L	H	H	H	H	H
4	H	H	L	H	H	H	H
5	L	H	L	H	H	H	H
6	H	L	L	H	H	H	H
7	L	L	L	H	H	H	H

ITT'S New Unabridged DTL Design Data Book

ITT DTL 930 SERIES

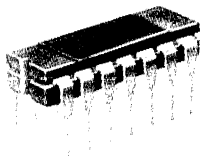
The ITT DTL 930 Series is a family of compatible integrated circuits using diode- transistor logic. The advantages of this family are:

- Choice of dual in-line, ¼″ × ¼″ flat pack, or TO-5 packages.
- Choice of full (−55° to +125°C) or limited (0 to +75°C) temperature ranges.
- Operation from a single power supply, and over a wide voltage range.
- Low power dissipation
- High worst-case noise immunity
- High fan-out capability
- Fan-out/noise immunity trade-off ability
- Specified operation over full temperature range
- Wide and proven application
- Gate outputs can be "wired OR"

FLAT PACK

SIMILAR TO TO-5

DUAL IN-LINE



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GLOSSARY OF TERMS USED WITH DTL 930 SERIES

In General, Subscripts are used as follows:

O = output
I = input
R = reverse, applying to high inputs.
F = forward, applying to low inputs.
L = low, applying to a low signal level or when with V_{CC} to low V_{CC} value.
H = high, applying to a high-signal level or when used with V_{CC} to high V_{CC} value.

Non-operational Terms:

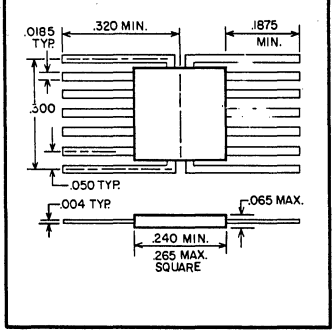
$V_{(MAX)}$ = Maximum rated V_{CC} pin voltage.
$I_{(MAX)}$ = Maximum rated current into V_{CC} pin, with $V_{(MAX)}$ applied.
V_{PD} = V_{CC} pin voltage applied during power dissipation test.
I_{PD} = Current into V_{CC} pin with V_{PD} applied. I_{PDL} means gate or buffer inputs are low or clock pin input is low. I_{PDH} means the inputs are high.
V_R = Input reverse (high) voltage for input diode leakage test.
I_R = Reverse input diode current with V_R applied to input.
I_{RCP} = Reverse clock pin input leakage current with V_R applied to input.
V_{CEX} = Output transistor collector to emitter voltage. With output pull-up resistor connected, V_{CEX} = V_{CC} to avoid drop across output pull-up resistor.

Operational Terms:

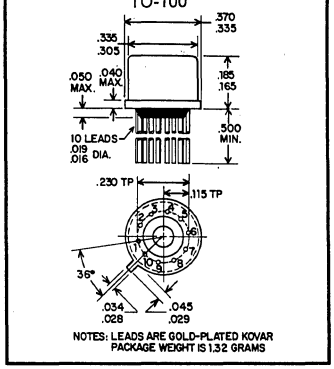
V_{IL} = Input low (threshold) voltage.
V_{OL} = Output low voltage, with rated fanout current I_{OL} into output.
LV_{CE} = Collector emitter latching voltage.
V_B = Breakdown voltage of capacitor input.
I_{CEX} = Output transistor collector to emitter leakage current with V_{CEX} applied to output.
V_{FD} = Forward diode drop in 933 Element.
I_{FD} = Forward diode current in 933 Element.
V_{IH} = Input high (threshold) voltage.
V_{OH} = Output high voltage, with high current (I_{OH}) flowing out of output.
V_F = Forward (low) input voltage, for forward input current (I_F) test. V_F is usually ground.
I_F = Forward input diode current, for unit input load. Also shown will be 2/3 I_F, I_{FCP}, and I_{FS}.
I_{OL} = Output low current.
I_{OH} = Output high current, flowing out of output in V_{OH} test.
I_{SC} = Short circuit output current to ground, with one or more inputs low. I_{SC} minimum confirms output ability to pull up capacitive loads; I_{SC} maximum confirms subtraction of fanout rules when "OR"ing outputs.
V_{CC} = Supply voltage.
V_{CCL} = Low V_{CC} pin voltage. Used for V_{OL} (I_{OL}) and V_{OH} (I_{OH}) tests.
V_{CCH} = High V_{CC} pin voltage. Used for V_F — I_F input forward diode current tests.
CP_X = Clock Pin, pulsed. The subscript if any refers to pulse waveshape. Used in testing binary elements.
V_{CPTH} = Input Clock Pin threshold voltage (low). With Clock Pin at or below V_{CPTH}, the "master" Flip-Flop holds the proper "slave" (output) Flip-Flop output high.
V_X = Input low (threshold) voltage extendable inputs.
I_{RK} = Monitoring current through resistance.

PACKAGES

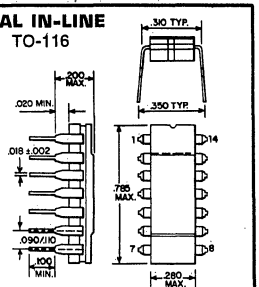
FLAT PACK
TO-86



SIMILAR TO TO-5
TO-100



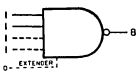
DUAL IN-LINE
TO-116



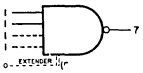
NOTES:
1. Leads are a modified hexagon in cross section. Board-drilling dimensions should equal your practice for a conventional .020 inch diameter lead.
2. Max. envelope for all planned packages of this design family.

INPUT-OUTPUT LOADING FACTORS

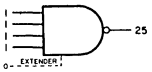
The number of elements that may be driven by an output terminal may consist of any combination of elements whose summation of input loading does not exceed the output terminal driving capability. Fanout for 0°C to +75°C range is given in parenthesis.



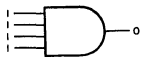
½ MIC 930.
¼ 946.
⅓ 962
⅛ 936



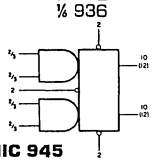
½ MIC 961.
¼ 949.
⅓ 963
⅛ 937



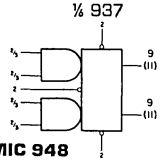
½ MIC 932
½ MIC 944



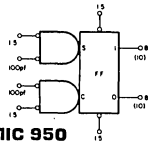
½ MIC 933



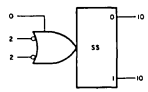
MIC 945



MIC 948



MIC 950



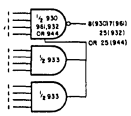
MIC 951

LOADING RULES

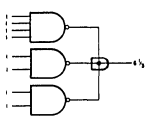
1. Extension of inputs with the MIC 933 does not affect quiescent loading of the supplemented element (MIC 930 or 932). However, capacitance due to wiring to the MIC 933 will affect noise tolerance and propagation delay, and thus establish a fan-in limit for the particular application. Please refer to the typical curves on the MIC 933 Dual Extender Element specifications.
2. For operation with a nominal supply voltage of 4.0 volts from −55°C to +125°C, reduce element fanout as follows: MIC 930=5, MIC 945=7, MIC 932=18. If temperature is maintained above −20°C, no fan-out reduction is necessary.
3. For operation with a nominal supply voltage of 6.0 volts from −55°C to +125°C, reduce element fan-out as follows: MIC 930=6, MIC 945=8, MIC 932=20. If ambient temperature remains below +100°C or if worst case noise threshold is considered to be 250 mV, no fan-out reduction is necessary. Except as noted, these rules apply over the entire military temperature range with a supply voltage of 4.5 to 5.5 volts. These rules also permit a 50°C temperature differential between individual elements. These rules guarantee a worst case signal-line or ground noise threshold of at least 350 mV. Practical noise thresholds exceed 500 mV.
4. All rules for MIC 930 apply to MIC 946, 962, and 936. All rules for MIC 961 apply to MIC 949, 963, and 937. **All rules for MIC 945 apply to MIC 9093 and 9099. All rules for MIC 948 apply to MIC 9094 and 9097.**
5. For increased current, inputs and outputs of ½ MIC 932 or ½ MIC 944 may be simultaneously paralleled up to 4 common outputs. Each combined input=4 loads. Combined output=100 loads.
6. An external resistor should be used with MIC 944. With external R to 5 volt V_{CC} ±0.5 V; subtract output loads as follows: R=2KΩ, subtract 2 loads, R=1KΩ, subtract 4 loads, R=510Ω, subtract 8 loads.

INPUT EXTENSION AND "wired OR" LOADING

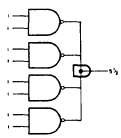
EXTENSION OF INPUTS



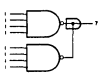
GATES WHEN "wired OR"



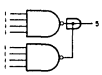
½ 930 and
2 x ¼ 946



4 x ¼ MIC 946



MIC 930 "wired OR"
ALSO 946, 962



MIC 961 "wired OR"
ALSO 949, 963

RULES FOR "wired OR"

1. Outputs of DTL gates with 6KΩ pull-up resistors, 930,946,962 and 936 may be tied together for the "wired OR" function. Subtract 1 unit of fan-out for each added gate. Subtract 5 fan-outs for 6 added gates.
2. Outputs of DTL gates with 2KΩ pull-up resistors, 949,961,963 and 937 may be tied together for the "wired OR" function. Subtract 2 units of fan-out for each added gate.
3. Outputs of MIC 932 may not be tied together for the "wired OR" function, however MIC 944 outputs may be used in the "wired OR" configuration.

NOISE IMMUNITY

There are two important types of noise immunity that must be considered when designing with ITT DTL 930 Series circuits. Both types are discussed below.

SIGNAL NOISE IMMUNITY

Signal Noise Immunity, V_{NS}, is defined by the equations

$$V_{NS} = |V_{IL}(\max) - V_{OL}(\max)|$$

or

$$V_{NS} = |V_{OH}(\min) - V_{IH}(\min)|$$

Where

$V_{OH}(\min)$ = Minimum high output voltage
$V_{IH}(\min)$ = Minimum high input voltage that will guarantee $V_{OL}(\max)$ at the output
$V_{IL}(\max)$ = Maximum low input voltage that will guarantee $V_{OH}(\min)$ at the output
$V_{OL}(\max)$ = Maximum low output voltage

The meaning of these equations is indicated in Fig. 1 and 2. The pulse shown at A in Fig. 2 is a noise signal induced on the signal line connecting two gates. The pulse at A is not sufficient to make the input voltage rise from V_{OL} (max) to $V_{IL}(\max)$ and, therefore the output of gate 2 will remain unchanged. However, the pulse at B will cause the input level to rise above $V_{IL}(\max)$ and, consequently, gate 2 may turn on, and its output voltage falls undesirably.

When gate 1 output is high, the output voltage is guaranteed to be greater or equal to $V_{OH}(\min)$ under the specified worst case conditions. The noise signal at C will not make the signal level fall below $V_{IH}(\min)$. Gate 2 will therefore maintain a low output level. However, the pulse at D may cause gate 2 to turn off, and its output voltage rises undesirably.

FIG. 1

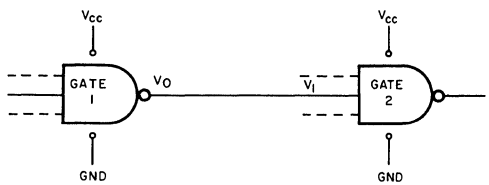
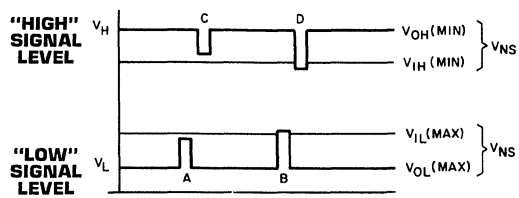


FIG. 2



GROUND NOISE IMMUNITY

Ground Noise immunity, V_{NG}, is usually the worst case noise immunity for DTL 930 Series circuits.

Notice that some curves show two values of V_{CC} at a given temperature for the same noise immunity. The upper V_{CC} ensures that the driving device is hard in saturation. Ground noise signals will therefore only add to output level $V_{OL}(\max)$. The noise immunity for this case will be defined by

$$V_{NG} = V_{NS} \simeq |V_{IL}(\max) - V_{OL}(\max)|$$

When the drive gate is hard in saturation due to high V_{CC}, ground noise signals will probably exceed the immunity defined by this equation before they reach a level tending to turn off the drive gate. As the V_{CC} is reduced, the load current in the output transistor will decline with a corresponding decrease in V_{OL}. The gate is still hard in saturation and we obtain a gain in noise immunity. However, as V_{CC} is lowered further, the gate reaches a region of soft saturation and the ground noise signal may turn off the drive gate. The gate amplifies the ground noise signal and the noise immunity is significantly less than $|V_{IL}(\max) - V_{OL}(\max)|$. Each of the curves shows V_N, the worst case of V_{NG} and V_{NS}.

As an example, the curves for a fan-out of 7 show a worst case $V_N = V_{NG}$ of 200 mV at $V_{CC} = 4V$ and $-55°F$. This, however, corresponds to a worst case signal noise immunity of $|V_{IL}(\max) - V_{OL}(\max)| \geqq 500$ mV for the same fan-out temperature and V_{CC}. This happens because V_{NS} only adds to $V_{OL}(\max)$ but V_{NG} deprives the output transistor of the drive gate of base current, thus turning it off.

FIG. 3

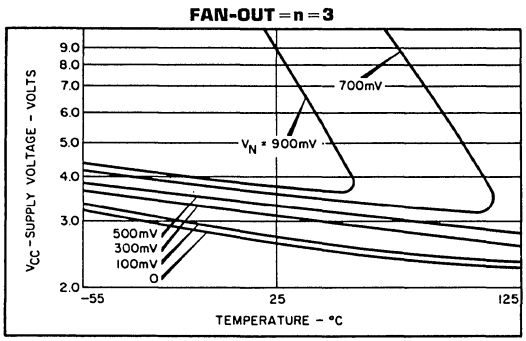


FIG. 4

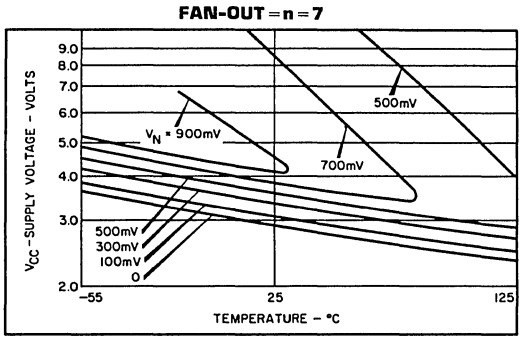


FIG. 5

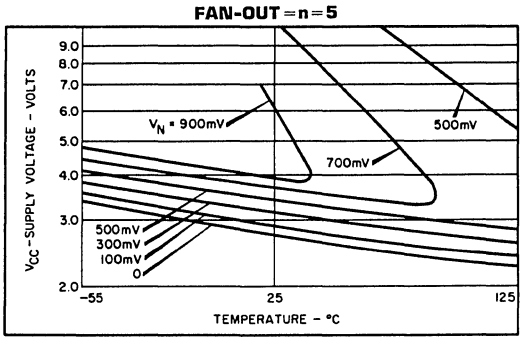
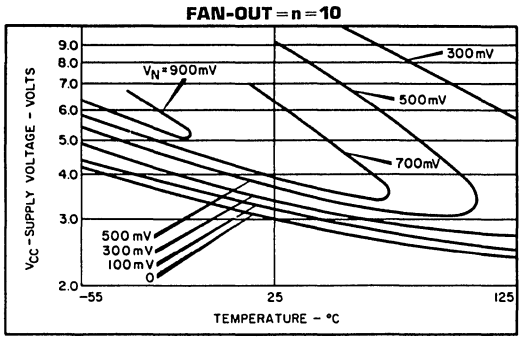
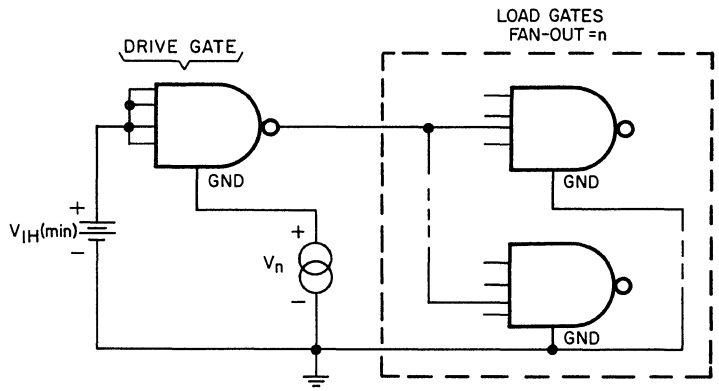


FIG. 6



TEST CONDITIONS FOR FIGURES 3, 4, 5, 6



PROPAGATION DELAY

AVERAGE tpd VS. TEMPERATURE

TEST CONDITION A, INACTIVE FAN-OUT

FAN-OUT=n, 5pf CAPACITANCE PER FAN-OUT
PULL UP RESISTOR=6KΩ

FIG. 7

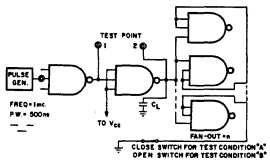
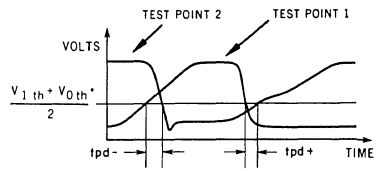


FIG. 8



$$AV.\,tpd = \frac{tpd- + tpd+}{2}$$

FIG. 9
Vcc=6V

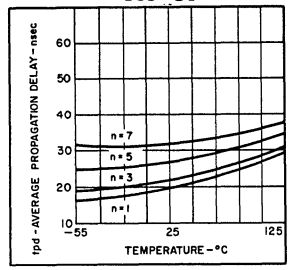


FIG. 10
Vcc=5V

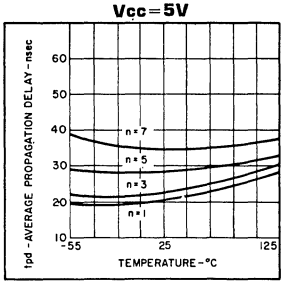


FIG. 11
Vcc=4V

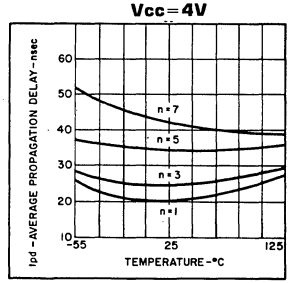
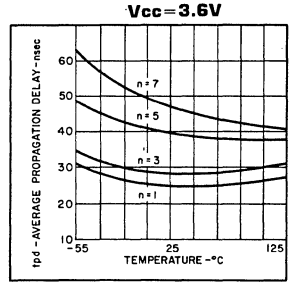


FIG. 12
Vcc=3.6V



TEST CONDITION B, ACTIVE FAN-OUT

FAN-OUT=n, 5pf CAPACITANCE PER FAN-OUT
PULL UP RESISTOR=6KΩ

FIG. 13

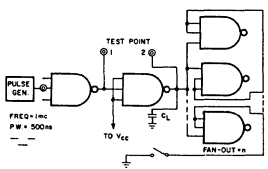
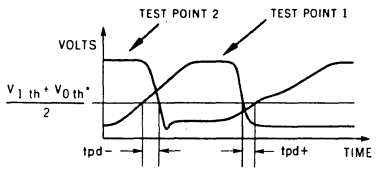


FIG. 14



$$AV.\,tpd = \frac{tpd- + tpd+}{2}$$

FIG. 15
Vcc=6V

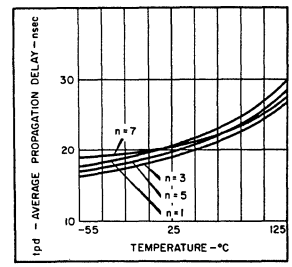


FIG. 16
Vcc=5V

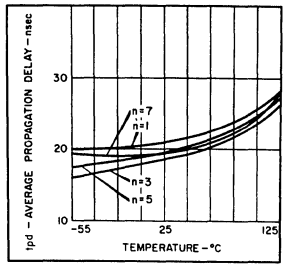


FIG. 17
Vcc=4V

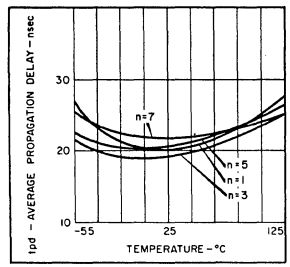
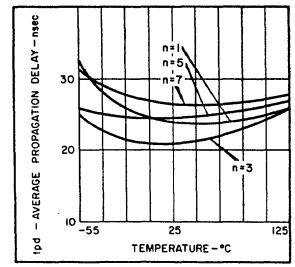


FIG. 18
Vcc=3.6V



TIME DELAY VERSUS CAPACITIVE LOADS

(THRESHOLD ≈ +1.5 V. T = 25°C, Vcc = +5.0 V)

FIG. 19
2K PULL-UP RESISTOR

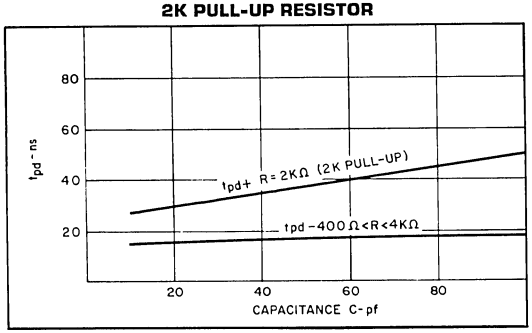


FIG. 20
6K PULL-UP RESISTOR

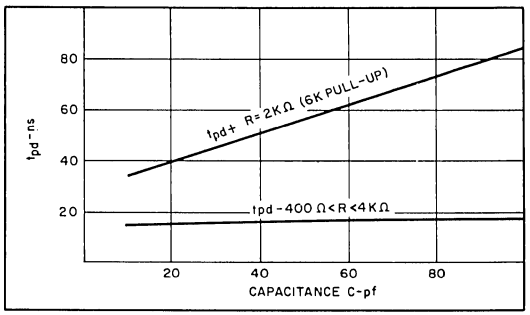
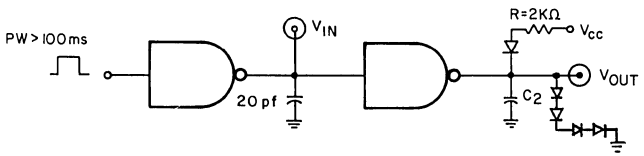


FIG. 21



ADDITIONAL DELAY TIME CHARACTERIZATION INTO CAPACITIVE LOADS

The curves on page 10 give extensive delay characterizations as functions of V_{CC}, temperature, fan-out and ratio of active to inactive fan-out. For each fan-out, active or inactive, 5pf wiring capacity was added. This page will show the effects of greater wiring capacities.

Most delay attributable to capacitive loads is associated with the positive going output. Two R-C time constants are seen in the positive going output, as shown in the pictures below. In the 1st time period, from the saturated low level to threshold, the R of the R-C time constant can be given by 6KΩ in parallel with $\frac{3.75K\Omega}{\text{active fan-out}}$.

Above the threshold which occurs at about 1.4 to 1.5 volts at 25°C, the R of the 2nd R-C time constant is 6KΩ and the rate of the voltage rise above threshold is slow. The logic signal propagates through at the threshold level; so voltage rise above threshold does not affect speed. By noting that both rise domains drive toward V_{CC}, the voltage rise waveform may be calculated. MIC 930, 932, 933, 936, 937, 946, 949, 961, 962, 963 are ~ 2pf per input for active or inactive fan-out; the remaining capacitance is from board, wiring, and connectors. Gates with 2KΩ pull resistors should be treated similarly.

The t_{pd} average curves, with one active fan-out, Fig. 23 below, gives the prediction of capacitive effects on switching speeds. In Fig. 22 below each output has 1 active fan-out, which is worst case.

FIG. 22

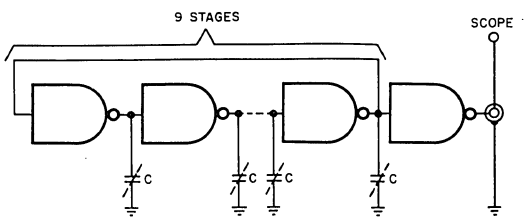
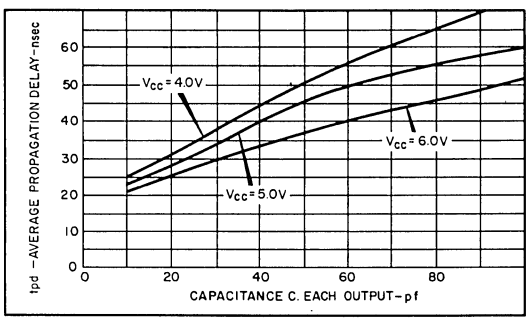


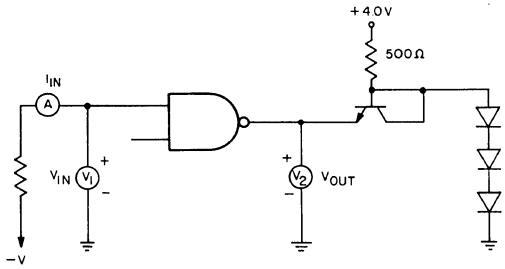
FIG. 23
t_{pd} AVERAGE VS. CAPACITY
MIC 930, 946, 962. (+25°C)



TRANSFER CHARACTERISTICS

TYPICAL CHARACTERISTICS, FAN-OUT = 7, V_{CC} = 4V

FIG. 24



NOTE: 500Ω RESISTOR SIMULATES WORST CASE.
FAN-OUT = 7 SINCE $\frac{R1+R2}{7}$ = 500Ω NOMINAL.

FIG. 25
V_{OUT} VS V_{IN}

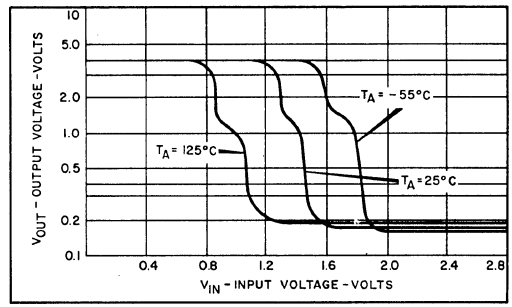


FIG. 26
V_{OUT} VS I_{IN}

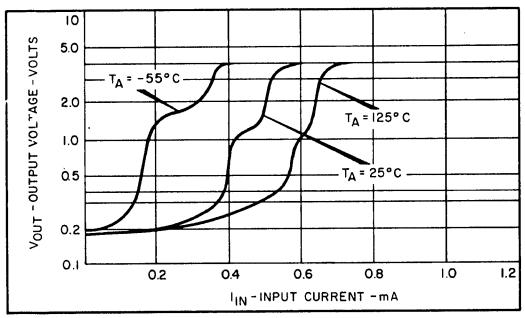
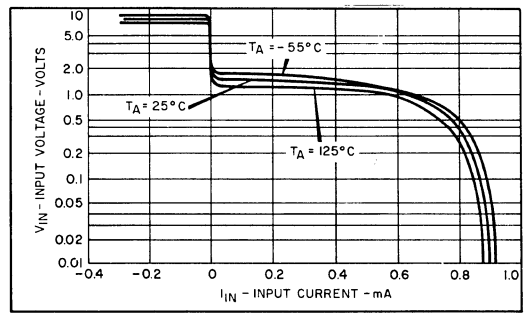


FIG. 27
V_{IN} VS I_{IN}



TRANSFER CHARACTERISTICS

TYPICAL CHARACTERISTICS, FAN-OUT = 0, V_{CC} = 4V

FIG. 28

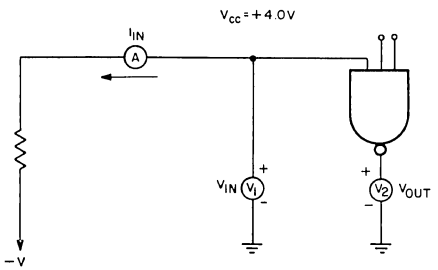


FIG. 29
VOUT VS. VIN

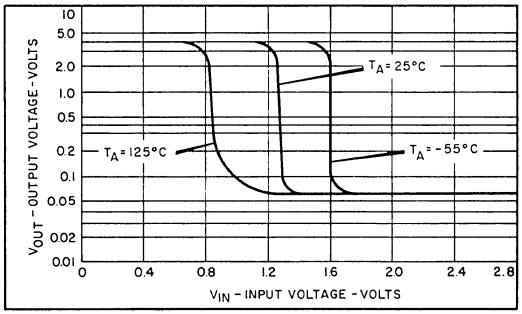


FIG. 30
VOUT VS. IIN

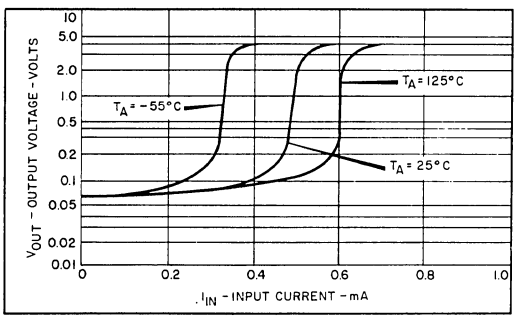
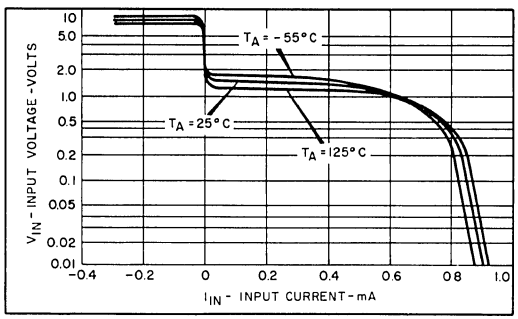


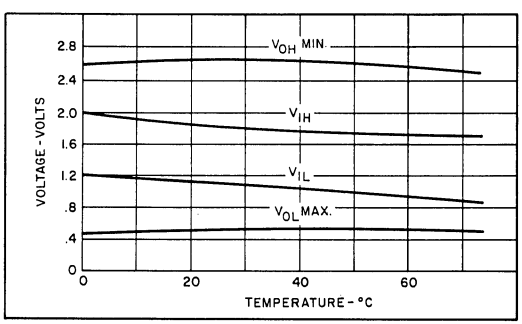
FIG. 31
VIN VS. IIN



OPERATING VOLTAGE PARAMETERS

VOH, VIH, VIL, VOL VS TEMPERATURE, Vcc = 5V

FIG. 32



DC CURVES

AVERAGE POWER DISSIPATION VS. TEMPERATURE FOR GATES

FIG. 33
Vcc = 5V

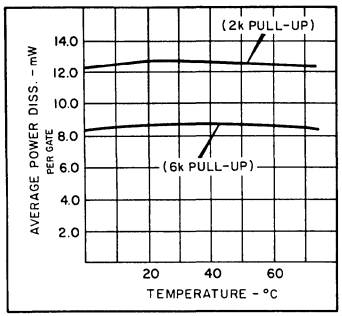
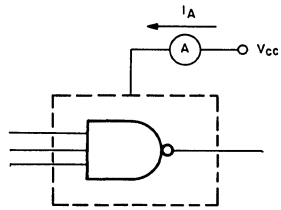
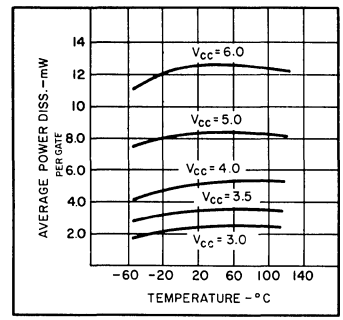


FIG. 34
TEST CIRCUIT



AV. POWER DISS. = $\frac{V_{CC}\ I_A}{2}$

FIG. 35
2K PULL-UP RESISTOR



NOTES: 1. Fig. 33, 6K pull-up curve for MIC 930, 936, 946, 962; 2K pull-up for MIC 937, 949, 961, 963.
2. Fig. 35 applies to MIC 937, 949, 961, 963 only.

TYPICAL-MAXIMUM I_F CURVES FOR GATES

FIG. 36
V_F = 0V

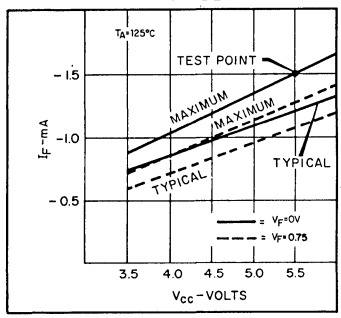


FIG. 37

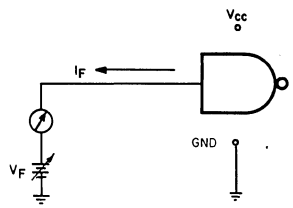
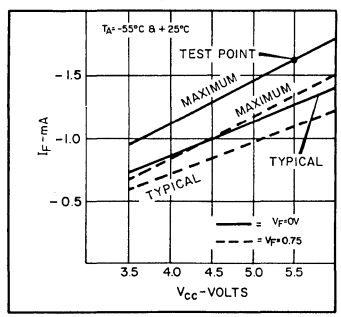


FIG. 38
V_F = 0.75V



OUTPUT CURRENT VS. OUTPUT VOLTAGE FOR 930, 936, 946, 962.

FIG. 39

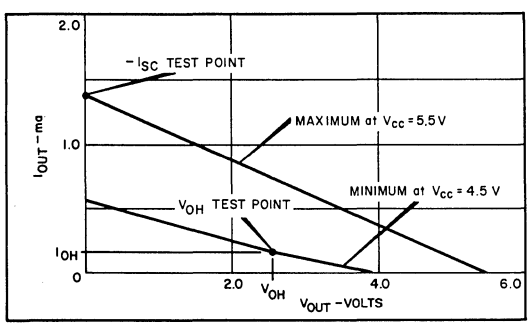
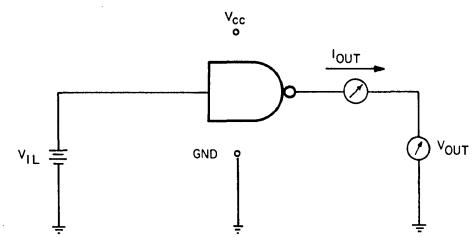


FIG. 40



OUTPUT LOW CURRENT VS. V_{CC} OR V_{OL} FOR MIC 930, 936, 946, 962.

FIG. 41

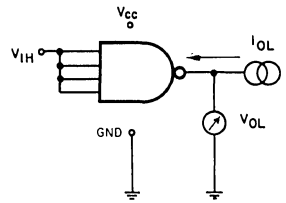


FIG. 42
I_{OL} VS. Vcc

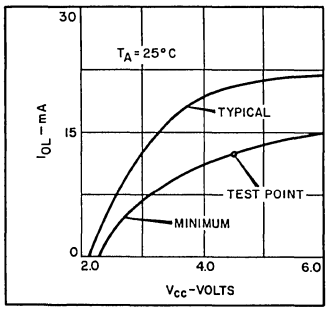


FIG. 43
I_{OL} VS. Vcc

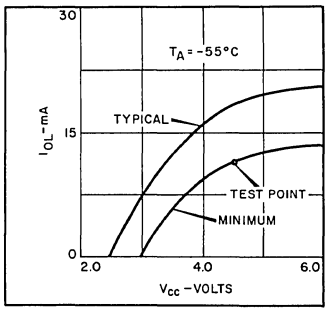
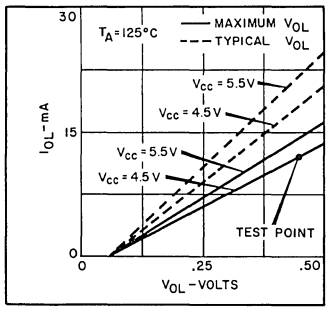


FIG. 44
I_{OL} VS. V_{OL} VS. Vcc

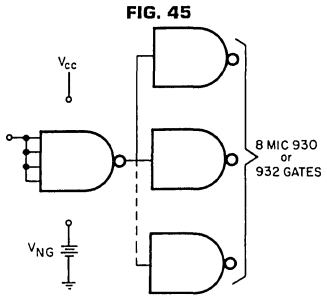


EXAMPLES OF USES FOR THE MINIMUM-MAXIMUM DC CURVES

EXAMPLE 1.

A low MIC 930 output at −55°C fans out to 8 inputs of MIC 930 or 932. V_{CC}=5V. Positive DC ground noise (V_{NG}) of 350 mV is applied to the 1st 930. Its output may thus rise to .75 Volt ($V_{NG}+V_{OL}$). 4.65 Volts ($V_{CC}-V_{NG}$) remain from V_{CC} pin to ground pin; this is above V_{CCL}=4.50 V, and test I_{OL} is conservative. Maximum current flowing out of each input of the 8 930/932's is given by Fig. 38 on Page 14 with V_F=0.75V and V_{CC}=5V; the current (I_F) is less than 1.25 mA and total current ($\leq 8\times 1.25=10$ mA) is less than the I_{OL} test current used at −55°C to saturate the low output. Above the 350 mV of V_{NG} already applied, the difference between the common node voltage ($\leq$.75V) and the low input threshold (V_{IL}=1.10V) of the 8 930/932's is still =350 mV, allowing for signal noise to be superposed above ground noise.

FIG. 45



EXAMPLE 2.

The I_F and I_{OL} curves on Pages 12 & 13 may be expressed in analytical form, as follows: I_F (930 and 932) $\leq \frac{V_{CC}-V_F-V_{FD}}{3K\Omega}$ T_A <25°C.

For T_A greater than 25°C, the 3KΩ rises by 0.12%/°C to approximately 3.36KΩ at +125°C. V_{FD} is the temperature dependent silicon forward diode drop and is about 0.70V at 25°C and 1 mA. ΔV_{FD}/°C is roughly 1.8 mV/°C. The ratio of I_{OL}, on 930 (Figs. 41, 42, and 43) at V_{CC} below test V_{CC}, to I_{OL} at test V_{CC} can be given by

$$\frac{I_{OL}\ @\ -55°C}{\text{Test } I_{OL}\ @\ V_{CCL}=4.5V} \geq \frac{V_{CC}-3.0V}{4.5V-3.0V}$$

and by

$$\frac{I_{OL}\ @\ 25°C}{\text{Test } I_{OL}\ @\ V_{CCL}=4.5V} \geq \frac{V_{CC}-2.3V}{4.5V-2.3V}$$

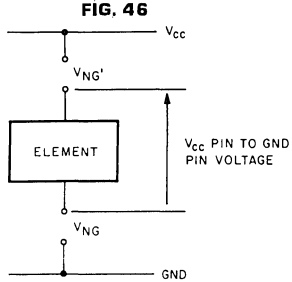
Since, at 25°C, $I_{OL}\geq$12 mA at V_{CCL}=4.5V is guaranteed by the device specifications, I_{OL} at V_{CC} pin to GND pin voltage of 3.6V is $\left(\frac{3.6-2.3.}{4.5-2.3.}\right)$12 mA = 7.1 mA.

The similar expression for the 932 gives a very conservative value due to the phase splitter gain. Above V_{CCL}, I_{OL} is limited by V_{OL} with an essentially resistive $\left(\frac{V_{OL}}{I_{OL}}\right.$ saturation resistance$\left.\right)$ slope. Fig. 44 at +125°C shows this, with V_{CC} having relatively small effect.

EXAMPLE 3.

The test sequences and tables of conditions and limits, use two values of V_{CC}, V_{CCL} and V_{CCH}. With a nominal 5 volts V_{CC}, for example, and assuming $\Delta V_{CC}=\pm.2V$, testing at V_{CCL}=4.5V and V_{CCH}=5.5V allows simulation of a 0.3V ground noise V_{NG} or V_{CC} line noise V_{NG}. Since there is gain associated with V_{NG} (refer to Page 7), particularly at lower temperatures and V_{CC} values; the test guarantees of output low current and voltage are the worst case test conditions to simulate worst case ground noise. Much better numbers could be shown, for example, in the ratio of output current to input current (I_{OL}/I_F) if both I_{OL} and I_F were measured at identical V_{CC} values and if input current was sunk into $V_F=V_{OL}$, the worst case low output level, or even into $V_F=V_{IL}$, the input threshold value. However, the test values would then guarantee only signal line noise immunity, where there is no gain associated with V_{NS}. By use of the Minimum/Maximum DC curves on Pages 12 & 13 or by the Example 2 equations, limits for the single V_{CC} testing approach could be recovered. More important, each design or components engineer can develop the fan-out, power, and noise margin tradeoffs for this unique application.

FIG. 46



DUAL FOUR—INPUT GATE MIC 930
FAST DUAL FOUR—INPUT GATE MIC 961

DESCRIPTION

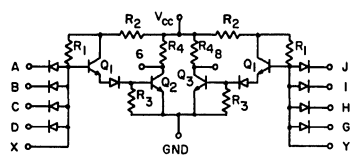
The MIC 930 and MIC 961 elements are dual four-input NAND/NOR gates.

In addition to performing the positive NAND and negative NOR logic functions, the gates can be cross-coupled to form a flip-flop or the outputs can be tied together to perform the "wired OR" function. Both gate inputs may be extended using MIC 933 elements to allow increased fan-in.

The MIC 930 incorporates a 6K output pull-up resistor which allows for a fan-out of up to 8 DTL loads.

The MIC 961 incorporates a 2K output pull-up resistor which typically results in a 30% faster rise time with capacitive loads at a fan-out of up to 7 DTL loads.

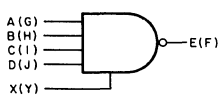
CIRCUIT SCHEMATIC



TYPICAL RESISTOR VALUES

$R_1 = 2.0\ K\Omega$
$R_2 = 1.75\ K\Omega$
$R_3 = 5.0\ K\Omega$
$R_4 = 6.0\ K\Omega$ (930)
$R_4 = 2.0\ K\Omega$ (961)

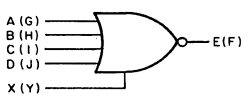
POSITIVE (NAND) LOGIC



$$E = \overline{A \cdot B \cdot C \cdot D \cdot (X)}$$

$$F = \overline{G \cdot H \cdot I \cdot J \cdot (Y)}$$

NEGATIVE (NOR) LOGIC



$$E = \overline{A + B + C + D + (X)}$$

$$F = \overline{G + H + I + J + (Y)}$$

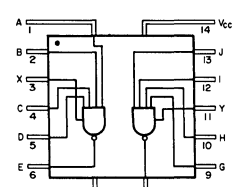
NOTE: Positive logic is used in specifications

TRUTH TABLE

A	B	C	D	X	E
G	H	I	J	Y	F
1	1	1	1	1	0
0	1	1	1	1	1
1	0	1	1	1	1
1	1	0	1	1	1
1	1	1	0	1	1
1	1	1	1	0	1
0	0	0	0	0	1

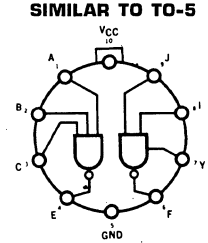
1 IS HIGH VOLTAGE
0 IS LOW VOLTAGE

FLAT PACK



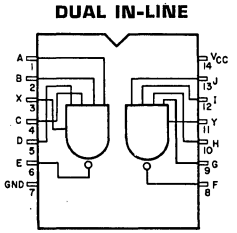
TOP VIEW

SIMILAR TO TO-5



TOP VIEW

DUAL IN-LINE



TOP VIEW

ABSOLUTE MAXIMUM RATINGS[1]

	UNITS
Supply Voltage (V_{CC}), −55°C to +125°C, Continuous ..... −.5 to +8	Volts
Supply Voltage (V_{CC}), Pulsed, <1 sec ..... +12	Volts
Output Current, Into Outputs 30	mA
Input Forward Current ..... −10	mA
Input Reverse Current 1	mA
Operating Temperature ..... −55 to +125	°C
Storage Temperature ..... −65 to +150	°C
Operating Junction Temperature[2] ..... +175	°C
Input Voltage Applied to Input ..... −1.5 to +5.5	V
Lead Temp. (soldering, 60 sec.) 300	°F

NOTES: 1. Above which useful life may be impaired.
2. Allow 200°C/Watt θ_{J-A} for TO-5; 300°C/Watt θ_{J-A} for ¼" x ¼" flatpack and dual in-line. Allow 50°C/Watt θ_{J-C} for TO-5; 180°C/Watt θ_{J-C} for ¼" x ¼" flatpack and dual in-line. Heat removal in ¼" x ¼" flatpack is highly dependent upon contact surfaces or air flow and on lead attachment and thermal paths thru leads, as well as number of soldered leads.

SUMMARY OF MIC 930 AND 961 CHARACTERISTICS (25°C)

Parameter		Note	FULL TEMPERATURE RANGE			LIMITED TEMPERATURE RANGE			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Operating Supply Voltage		1	4.5	5.0	5.5		5.0		Volts
Network Dissipation	930	2		17	32.5		17	40	mW
	961			25	54.5		25	59	
Loading D.C. fan-out	930			8			8		DTL Unit
	961			7			7		Load
Output Logic 'I' (High)	930		2.6			2.6			Volts
	961		2.6			4.3			
'O' (Low)	930				0.4			0.45	
	961				0.4			0.5	
Input Threshold 'I' (High)		3	1.9			1.9			Volts
'O' (Low)					1.1			1.1	
Propagation t_{pd}+	930	4	25		80	25		80	Nano-
Delay Time	961		15		50	15		50	Second
t_{pd}−	930		10		30	10		30	
	961		10		30	10		30	
Noise Immunity		5	0.35	>.50		0.35	>.50		Volts

NOTES: 1. Exact specification limits for operating temperature range may be obtained by reference to the appropriate test.
2. Power supplied from V_{CC} supply (V_{CC} = 5V) during "ON" state, fan-out = 0.
3. Input threshold voltage is defined as the minimum (or maximum) voltage at the circuit input to guarantee a low (or high) output.
4. Propogation delay time terms (t_{pd}+ and t_{pd}−) are described in the t_{pd} test circuit, Page 8.
5. See Noise test circuit, Page 7, and Loading Factors, Page 5.

MIC 930 TIME DELAYS VS. CAPACITIVE LOADS

FIG. 47

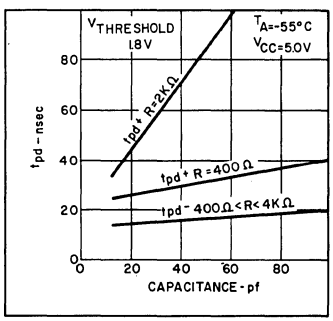


FIG. 48

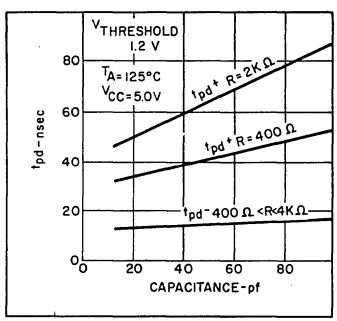
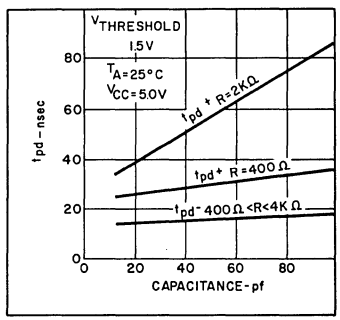


FIG. 49



TEST SEQUENCE

Abbreviated Test Sequences for the 930 and 961 elements are shown below. The ground pin is grounded on all tests.

Test No.	Notes	FORCING CONDITIONS								LIMITS	
		Pin A (G)	Pin B (H)	Pin C (I)	Pin D (J)	Pin X (Y)	Pin E (F)	V_{CC}	Sense	Min.	Max.
1, (2)		V_{IH}	V_{IH}	V_{IH}	V_{IH}		I_{OL}	V_{CCL}	V_E (V_F)		V_{OL}
3, 4, 5, 6 (7, 8, 9, 10)	2, 3	V_{IL}	V_{IL}	V_{IL}	V_{IL}		$-I_{OH}$	V_{CCL}	V_E (V_F)	V_{OH}	
11, (12)		V_R	GND	GND	GND			V_{CCH}	I_A (I_G)		I_R
13, (14)		GND	V_R	GND	GND			V_{CCH}	I_B (I_H)		I_R
15, (16)	3	GND	GND	V_R	GND			V_{CCH}	I_C (I_I)		I_R
17, (18)	3	GND	GND	GND	V_R			V_{CCH}	I_D (I_J)		I_R
19, (20)		V_F	V_R	V_R	V_R			V_{CCH}	I_A (I_G)		$-I_F$
21, (22)		V_R	V_F	V_R	V_R			V_{CCH}	I_B (I_H)		$-I_F$
23, (24)	3	V_R	V_R	V_F	V_R			V_{CCH}	I_C (I_I)		$-I_F$
25, (26)	3	V_R	V_R	V_R	V_F			V_{CCH}	I_D (I_J)		$-I_F$
27, (28)		GND					V_{CEX}	V_{CEX}	I_E (I_F)		I_{CEX}
29, (30)		GND					GND	V_{CCH}	I_E (I_F)	$-I_{SC}$	$-I_{SC}$
31								V_{PD}	I_{VCC}		I_{PDH}
32	4	GND						V(max)	I_{VCC}		I(max)
33, (34)	3					V_X	$-I_{OH}$	V_{CCL}	V_E (V_F)	V_{OH}	
35, 36		$t_{pd}+$, $t_{pd}-$ —See table of test circuit conditions and limits, Page 17									
37, (38)		V_F	V_R	V_R	V_R			V_{CCL}	I_A (I_G)		$-I_{F2}$
39, (40)		V_R	V_F	V_R	V_R			V_{CCL}	I_B (I_H)		$-I_{F2}$
41, (42)	3	V_R	V_R	V_F	V_R			V_{CCL}	I_C (I_I)		$-I_{F2}$
43, (44)	3	V_R	V_R	V_R	V_F			V_{CCL}	I_D (I_J)		$-I_{F2}$
45, (46)		V_{IH}	V_{IH}	V_{IH}	V_{IH}		I_{OL2}	V_{CCH}	V_E (V_F)		V_{OL2}
47	6	GND	GND	GND	GND			V_{PD}	I_{VCC}		I_{PDL}

NOTES:

1. Both elements are dual "NAND" gates; therefore, the test sequences for each are identical. Tests on each side of the dual are identical; therefore, matching test and pin numbers are shown in parentheses.
2. V applied individually to 1 input each test. Other inputs open.
3. Delete these tests for 10-pin TO-5 package: 6, 9, 10, 16, 17, 18, 24, 25, 26, 33, 41, 42, 43, 44.
4. Ground one input on each gate.
5. Tests 37/47 apply to full temperature range only.
6. Ground all inputs simultaneously.

FORCING CONDITIONS — 930,961

FULL TEMPERATURE RANGE					LIMITED TEMPERATURE RANGE				
Parameter	Units	−55° C	+25° C	+125° C	Parameter	Units	0° C	+25° C	+75° C
V(max)	Volts		8.0		V (max)	Volts		8.0	
V_{PD}	Volts		5.0		V_{PD}	Volts		5.0	
V_{CCH}	Volts	5.5	5.5	5.5	V_{CCH}	Volts	5.0	5.0	5.0
V_{CCL}	Volts	4.5	4.5	4.5	V_{CCL}	Volts	5.0	5.0	5.0
V_R	Volts	4.0	4.0	4.0	V_R	Volts	4.0	4.0	4.0
V_F	Volts	0.4	0.4	0.4	V_F	Volts	0.45	0.45	0.5
V_{CEX}	Volts		4.5		V_{CEX}	Volts		5.0	
$-I_{OH}$(930)	mA	.18	.18	.18	$-I_{OH}$	mA	.12	.12	.12
I_{OL1} 930	mA	12.0	12.0	12.0	I_{OL} 930	mA	12.0	12.0	11.4
I_{OL1} 961	mA	10.8	10.8	10.8	I_{OL} 961	mA	10.5	10.5	10.2
V_{IL}	Volts	1.4	1.1	0.8	V_{IL}	Volts	1.2	1.1	0.95
V_{IH}	Volts	2.1	1.9	1.7	V_{IH}	Volts	2.0	1.9	1.8
V_X	Volts		1.8		V_X	Volts		1.8	
$-I_{OH}$(961)	mA	0.54	0.54	0.54					
I_{OL2}(930)	mA	15.0	15.0	15.0					
I_{OL2}(961)	mA	13.5	13.5	13.5					

TEST LIMITS

Parameter MIC 930	Units	FULL TEMPERATURE RANGE						LIMITED TEMPERATURE RANGE					
		−55°C		+25°C		+125°C		0°C		+25°C		+75°C	
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.
V_{OL1}	Volts		.40		.40		.40		.45		.45		.50
V_{OH}	Volts	2.5		2.6		2.5		2.6		2.6		2.5	
I_R	μA		2.0		2.0		5.0		5.0		5.0		10.0
$-I_{F1}$	mA		1.5		1.5		1.4		1.40		1.40		1.33
I_{CEX}	μA				50.0						100		
$-I_{SC}$	mA	.610	1.34	.610	1.34	.535	1.30	.610	1.30	.610	1.30	.535	1.25
I(max)	mA				5.50						8.0		
I_{PDH}	mA				6.50						8.0		
$-I_{F2}$	mA		1.16		1.16		1.08						
V_{OL2}	Volts		.4		.4		.4						
I_{PDL}	mA		2.0		2.94								
MIC 961													
V_{OL1}	Volts		.40		.40		.45		0.50		0.50		0.55
V_{OH}	Volts	2.5		2.6		2.5		4.3		4.3		4.2	
I_R	μA		2.0		2.0		5.0		5.0		5.0		10.0
$-I_{F1}$	mA		1.5		1.5		1.4		1.40		1.40		1.33
I_{CEX}	μA				50.0						100		
$-I_{SC}$	mA	2.1	3.7	2.1	3.7	1.86	3.28			1.85	3.68		
I(max)	mA				5.2						5.72		
I_{PDH}	mA				10.9						11.8		
$-I_{F2}$	mA		1.16		1.16		1.08						
V_{OL2}	Volts		.4		.4		.4						
I_{PDL}	mA				2.94								

PROPAGATION DELAY Tpd TESTS

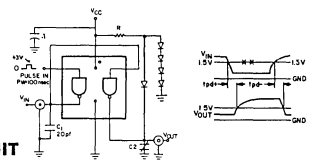


FIG. 50 tpd TEST CIRCUIT

t_{pd}— of 930, 961 elements will be read from input at 1.5 V.

All diodes 1N916 or equivalent.

C_1 and C_2 includes probe and jig capacitance.

$V_{Threshold}$= 1.5V at 25°C; at other temperatures $V_{Threshold}$ will be stated.

TABLE OF CONDITIONS & LIMITS t_{pd} TESTS

(See Test Circuit.)
(V_{CC} = 5V, T = 25°C)

		R	C_2 (pf)	Min. (nsec)	Max. (nsec)
$t_{pd}+$	930	3.9 K	30	25	80
$t_{pd}-$	930	400 Ω	50	10	30
$t_{pd}+$	930	400 Ω	50	15	40 [1]
$t_{pd}-$	930	3.9 K	20	5	20 [1]
$t_{pd}+$	961	3.9 K	30	15	50
$t_{pd}-$	961	400 Ω	50	10	30

NOTE: 1. Correlating limit provided as design information only.

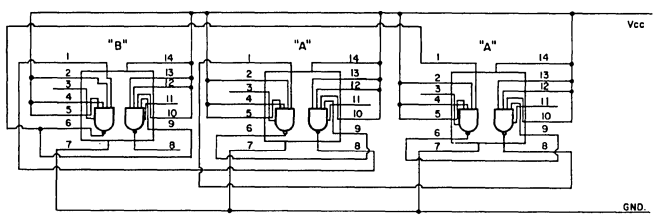
RELIABILITY TESTS

PERFORMED DURING ITT RELIABILITY PROGRAM

MEASUREMENTS OF THE FOLLOWING PARAMETERS ARE RECORDED:

Parameter	Test Sequence Number on Page 16
V_{OL}	#1
V_{OH}	#4
I_R	#15 & #16
I_F	#20 & #25
I(max)	#32

FIG. 51 LIFE TEST CIRCUIT



NOTE: V_{CC}= +5.5 Volts Ambient Temperature= +125° C
Circuit may have any number of units connected like "A", with one connected like "B". The circuit must contain an odd number of gates in series in the ring.

DUAL FOUR-INPUT BUFFER MIC 932
DUAL FOUR-INPUT POWER GATE MIC 944

DESCRIPTION

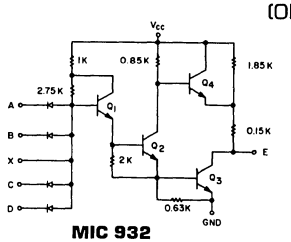
The MIC 932 and MIC 944 elements are dual four-input NAND/NOR buffer and power gates respectively.

Both elements have typical output currents of up to 100 ma. This enables them to provide much higher fan-out than a typical NAND/NOR gate. Both elements are extendable. The MIC 932 incorporates an emitter follower pull-up which combines high fan-out with superior capacitance driving capability.

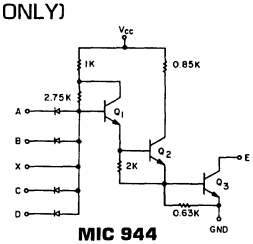
The MIC 932 cannot be externally connected to perform the "wired OR" logic function. The MIC 944, which does not incorporate the emmitter pull-up, can be used either as a high fan-out interface driver or low power lamp driver. The output can be tied to an external pull-up resistor and returned to a supply voltage of up to 12 volts. The supply may be located near the output or at the far end of an open transmission line or twisted pair interconnection. This allows the MIC 944 to be used as a line driver.

The MIC 944 can be externally connected to perform the "wired OR" logic function.

CIRCUIT SCHEMATIC
(ONE GATE ONLY)



MIC 932



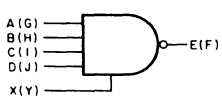
MIC 944

TRUTH TABLE

A	B	C	D	X	E
G	H	I	J	Y	F
1	1	1	1	1	0
0	1	1	1	1	1
1	0	1	1	1	1
1	1	0	1	1	1
1	1	1	0	1	1
1	1	1	1	0	1
0	0	0	0	0	1

1 IS HIGH VOTAGE
0 IS LOW VOLTAGE

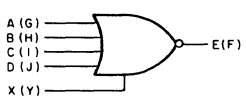
POSITIVE (NAND) LOGIC



$E = \overline{A \cdot B \cdot C \cdot D \cdot (X)}$

$F = \overline{G \cdot H \cdot I \cdot J \cdot (Y)}$

NEGATIVE (NOR) LOGIC

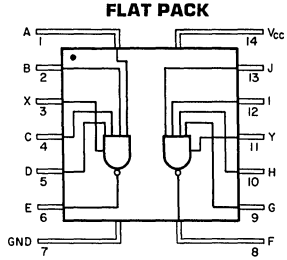


$E = \overline{A + B + C + D + (X)}$

$F = \overline{G + H + I + J + (Y)}$

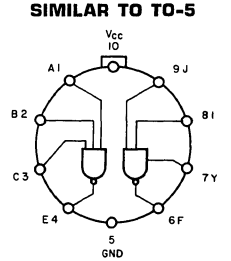
NOTE: Positive logic is used in specifications

FLAT PACK



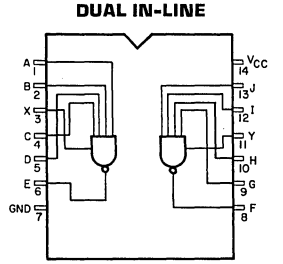
TOP VIEW

SIMILAR TO TO-5



TOP VIEW

DUAL IN-LINE



TOP VIEW

ABSOLUTE MAXIMUM RATINGS[1]

	UNITS
Supply Voltage (V_{CC}), −55°C to +125°C, Continuous ..... −.5 to +8.0	Volts
Supply Voltage (V_{CC}), pulsed, <1.0 sec. ..... +12	Volts
Output Current, into Outputs, Continuous 150	mA
Output Current, into Outputs, pulsed, <30 milliseconds 300	mA
Input Forward Current ..... −10	mA
Input Reverse Current 1	mA
Operating Ambient Temperature ..... −55 to +125	°C
Storage Temperature ..... −65 to +150	°C
Operating Junction Temperature[2] ..... +175	°C
Input Voltage Applied to Input ..... −1.5 to +5.5	Volts
Lead Temp. (soldering, 60 sec.) 300	°C

NOTES: 1. Above which useful life may be impaired.

2. Allow 200°C/Watt θ_{J-A} for TO-5; 300°C/Watt θ_{J-A} for ¼" x ¼" flatpack and dual in-line. Allow 50°C/Watt θ_{J-C} for TO-5; 180°C/Watt θ_{J-C} for ¼" x ¼" flatpack and dual in-line. Heat removal in ¼" x ¼" flatpack is highly dependent upon contact surfaces or air flow and on lead attachment and thermal paths thru leads, as well as number of soldered leads.

SUMMARY OF MIC 932 AND 944 CHARACTERISTICS (25°C)

Parameter		Note	FULL TEMPERATURE RANGE			LIMITED TEMPERATURE RANGE			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Operating Supply Voltage		1	4.5	5.0	5.5		5.0		Volts
Network Dissipation	932	2		56.0	133.0		56.0	150.0	mW
	944			44.0	100.0		44.0	100.0	
Loading D.C. Fanout					25.0			25.0	DTL Unit Load
Output Logic '1' (High)	932		2.6			2.6			Volts
	944								
'0' (Low)	932				0.4			0.45	
	944				0.4			0.45	
Input Threshold '1' (High)		3	1.9			1.9			Volts
'0' (Low)					1.1			1.1	
Propagation $t_{pd}+$	932	4	25.0		80.0	25.0		80.0	Nano-
Delay Time	944		15.0		50.0	15.0		50.0	Second
$t_{pd}-$	932		15.0		40.0	15.0		40.0	
	944		10.0		35.0	10.0		35.0	
Noise Immunity		5	0.35	>0.5		0.35	>0.5		Volts

NOTES: 1. Exact specification limits for operating temperature range may be obtained by reference to the appropriate test.

2. Power supplied from V_{CC} (5V) during "ON" state fan-out = 0.

3. Input threshold voltage is defined as the minimum (or maximum) voltage at the circuit input to guarantee a low (or high) output.

4. Propogation delay time terms ($t_{pd}+$ and $t_{pd}-$) are described in the t_{pd} test circuit, Page 8.

5. See Loading Factors, Page 5.

TEST SEQUENCE

Both elements are dual "NAND" gates; therefore, the test sequences for each are identical. Tests on each side of the dual are identical; therefore, matching test and pin numbers are shown in parentheses.

Test No.	Notes	Pin A (G)	Pin B (H)	Pin C (I)	Pin D (J)	Pin X (Y)	Pin E (F)	V_{CC}	Sense	LIMITS Min.	LIMITS Max.
1, (2)		V_{IH}	V_{IH}	V_{IH}	V_{IH}		I_{OL}	V_{CCL}	$V_E(V_F)$		V_{OL}
3, 4, 5, 6, (7, 8, 9, 10)	1, 3	V_{IL}	V_{IL}	V_{IL}	V_{IL}		I_{OH}	V_{CCL}	$V_E(V_F)$	V_{OH}	
11, (12)		V_R	GND	GND	GND			V_{CCH}	$I_A(I_G)$		I_R
13, (14)		GND	V_R	GND	GND			V_{CCH}	$I_B(I_H)$		I_R
15, (16)		GND	GND	V_R	GND			V_{CCH}	$I_C(I_I)$		I_R
17, (18)		GND	GND	GND	V_R			V_{CCH}	$I_D(I_J)$		I_R
19, (20)		V_F	V_R	V_R	V_R			V_{CCH}	$I_A(I_G)$		I_F
21, (22)		V_R	V_F	V_R	V_R			V_{CCH}	$I_B(I_H)$		I_F
23, (24)		V_R	V_R	V_F	V_R			V_{CCH}	$I_C(I_I)$		I_F
25, (26)		V_R	V_R	V_R	V_F			V_{CCH}	$I_D(I_J)$		I_F
27, (28)	3	GND					V_{CEX}	V_{CEX}	$I_E(I_F)$		I_{CEX}
29, (30)	2, 3	GND					GND	V_{CCH}	$I_E(I_F)$	I_{SC}	
31								V_{PD}	I_{VCC}		I_{PDH}
32	2,	GND						V(max)	I_{VCC}		I(max)
33, (34)	3					V_X	I_{OH}	V_{CCL}	$V_E(V_F)$	V_{OH}	
35, 36			$t_{pd}+$, $t_{pd}-$	See Table of test circuit conditions and limits, Page 21							
35, 36, 37, 38, (39, 40, 41, 42)	1, 4	V_{IL}	V_{IL}	V_{IL}	V_{IL}		V_{CEX}	V_{CCH}	$I_E(I_F)$		I_{CEX}
43, (44)	4					V_X	V_{CEX}	V_{CCH}	$I_E(I_F)$		I_{CEX}
45, (46)	4	GND					I_{CE}	V_{CCH}	$V_E(V_F)$	LV_{CE}	
47, (48)		V_F	V_R	V_R	V_R			V_{CCL}	$I_A(I_G)$		$-I_{F2}$
49, (50)		V_R	V_F	V_R	V_R			V_{CCL}	$I_B(I_H)$		$-I_{F2}$
51, (52)		V_R	V_R	V_F	V_R			V_{CCL}	$I_C(I_I)$		$-I_{F2}$
53, (54)		V_R	V_R	V_R	V_F			V_{CCL}	$I_D(I_J)$		$-I_{F2}$
54, (55)		V_{IH}	V_{IH}	V_{IH}	V_{IH}		I_{OL2}	V_{CCH}	$V_E(V_F)$		V_{OL2}
56	6	GND	GND	GND	GND			V_{PD}	I_{VCC}		I_{PDL}

NOTES: 1. V applied individually to 1 input each test. Other inputs open. 2. Apply GND to both pins A and G. 3. MIC 932 only. 4. MIC 944 only. 5. On 10 Pin TO-5 units, pins D, X, I and J are omitted. Thus tests 6, 9, 10, 16, 17, 18, 24, 25, 26, 33, 38, 41, 42 and 43 do not apply. 6. Ground all inputs simultaneously. 7. Tests 45/56 apply to full temperature range only.

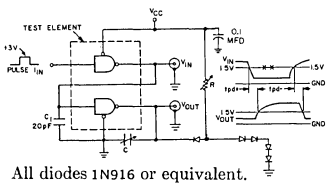
FORCING CONDITIONS

Parameter	Units	FULL TEMPERATURE RANGE −55°C	FULL TEMPERATURE RANGE +25°C	FULL TEMPERATURE RANGE +125°C	Parameter	Units	LIMITED TEMPERATURE RANGE 0°C	LIMITED TEMPERATURE RANGE +25°C	LIMITED TEMPERATURE RANGE +75°C
V_{CCH}	Volts	5.5	5.5	5.5	V_{CCH}	Volts	5.0	5.0	5.0
V_{CCL}	Volts	4.5	4.5	4.5	V_{CCL}	Volts	5.0	5.0	5.0
V_{CEX} (932)	Volts		4.5		V_{CEX}(932)	Volts		5.0	
V_{MAX}	Volts		8.0		V_{MAX}	Volts		8.0	
V_{PD}	Volts		5.0		V_{PD}	Volts		5.0	
V_{IH}	Volts	2.1	1.9	1.7	V_{IH}	Volts	2.0	1.9	1.8
V_{IL}	Volts	1.4	1.1	0.8	V_{IL}	Volts	1.2	1.1	0.95
V_F	Volts	0.4	0.4	0.4	V_F	Volts	0.45	0.45	0.5
V_R	Volts	4.0	4.0	4.0	V_R	Volts	4.0	4.0	4.0
V_X	Volts		1.8		V_X	Volts		1.8	
$-I_{OH}$ (932)	mA	2.0	2.5	4.0	$-I_{OH}$ (932)	mA	2.0	2.5	3.0
I_{OL1}	mA	36.0	36.0	36.0	I_{OL1}	mA	36.0	36.0	34.0
I_{OL2}	mA	37.5	37.5	37.5	I_{OL2}				
I_{CE} (944)	mA	5.0	5.0	5.0	I_{CE} (944)	mA	5.0	5.0	5.0
V_{CEX} (944)	Volts	4.5	4.5	4.5	V_{CEX}(944)	Volts		5.0	

TEST LIMITS

Parameter	Units	FULL TEMPERATURE RANGE						LIMITED TEMPERATURE RANGE					
		−55°C		+25°C		+125°C		0°C		+25°C		+75°C	
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.
V_{OL}	Volts		0.4		0.4		0.45		0.45		0.45		0.5
V_{OH} (932)	Volts	2.5		2.6		2.50		2.6		2.6		2.5	
I_R	μA		2.0		2.0		5.0		5.0		5.0		10.0
$-I_F$	mA		1.6		1.6		1.5		1.4		1.4		1.33
$-I_{SC}$ (932)	mA	16.0		18.0		16.0		15.0		16.0		14.0	
I_{PDH} (932)	mA				26.6						30.0		
I_{PDH} (944)	mA				20.0						20.0		
$-I_{MAX}$ (932)	mA				6.0						8.0		
$-I_{MAX}$ (944)	mA				6.0						6.0		
I_{CEX} (932)	μA				50.0						100.0		
I_{CEX} (944)	μA		50.0		100.0		200.0				100.0		
LV_{CE}(944)	Volts			6.0						6.0			
$-I_{F2}$	mA		1.16		1.16		1.08						
V_{OL2}	Volts		.4		.4		.4						
I_{PDL}	mA				2.94								

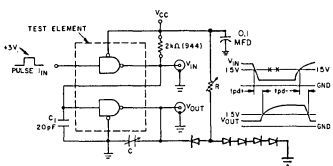
CIRCUIT FOR MIC 932
FIG. 52



All diodes 1N916 or equivalent.

C_1 and C includes probe and jig capacitance.

CIRCUIT FOR MIC 944
FIG. 53



C_1 and C includes probe and jig capacitance.

PROPAGATION DELAY

tpd TESTS

TABLE OF CONDITIONS & LIMITS tpd TESTS

(See Test Circuit.) (V_{CC} = 5V, T = 25°C)	R (Ω)	C (pf)	Min. (nsec)	Max. (nsec)
$t_{pd}+$	944	510	20	15	50
$t_{pd}-$	944	150	100	10	35
$t_{pd}+$	932	510	500	25	80
$t_{pd}-$	932	150	500	15	40
$t_{pd}+$	944	150	20	10	35 (1)
$t_{pd}-$	944	510	20	5.0	20 (1)
$t_{pd}+$	932	150	500	20	65 (1)
$t_{pd}-$	932	510	200	8.0	30 (1)

NOTE: 1. Correlating limit provided as design information only.

TYPICAL tpd VS. CAPACITY

FIG. 54 MIC 932, 944

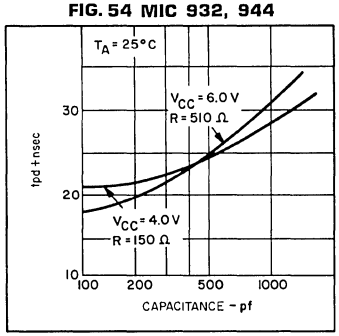


FIG. 55 MIC 944

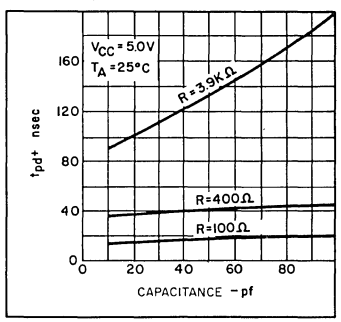
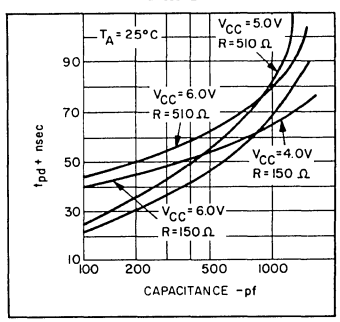


FIG. 56 MIC 932



ADDITIONAL CHARACTERISTICS

FIG. 57 TYPICAL POWER DISSIPATION PER SIDE VS. SUPPLY VOLTAGE
(OUTPUT NOT LOADED) (932, 944)

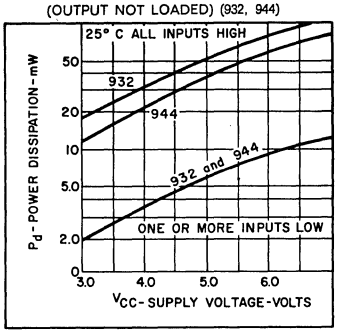


FIG. 58 DTL INPUT THRESHOLDS VS. TEMPERATURE (932, 944)

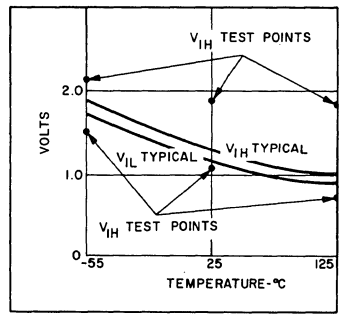


FIG. 59 TYPICAL OUTPUT CURRENT WITH INPUTS LOW (932)

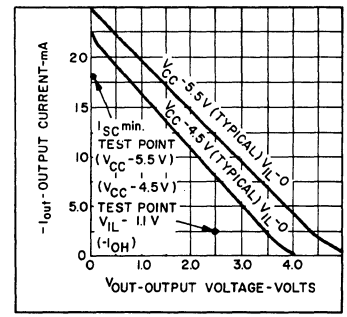


FIG. 60

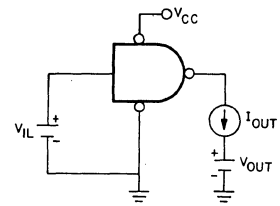


FIG. 61

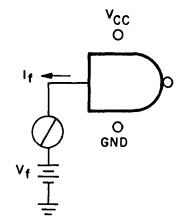


FIG. 62 $1 I_F$ MIC 932, 944 MAXIMUM VS. TYPICAL
(T_A = −55°C & +25°C)

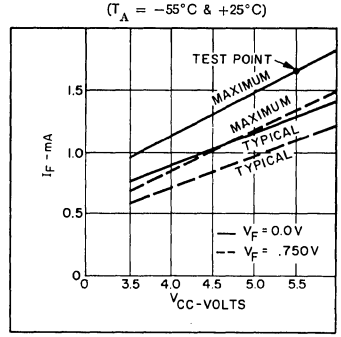


FIG. 63 $1 I_F$ MIC 932, 944 MAXIMUM VS. TYPICAL
(V_F = OV & V_F = .750V T_A = +125°C)

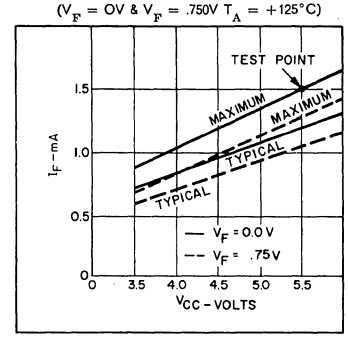


FIG. 64 TYPICAL OUTPUT LOW CURRENT VS. SUPPLY VOLTAGE
(−55°C and +25°C) (932)

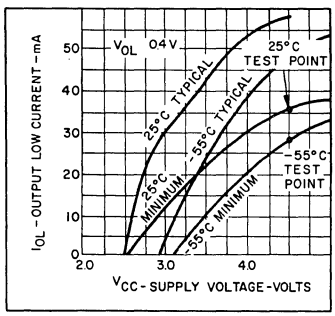


FIG. 65 TYPICAL OUTPUT LOW CURRENT VS. OUTPUT VOLTAGE
(+125°C) (932)

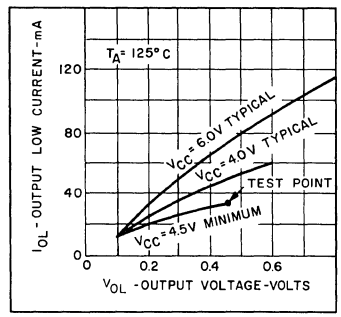


FIG. 66 TYPICAL OUTPUT LOW CURRENT VS. OUTPUT VOLTAGE
(+125°C) (944)

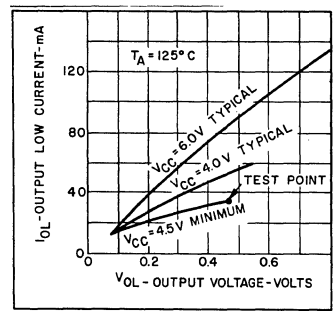
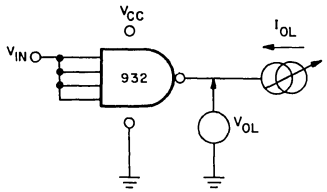


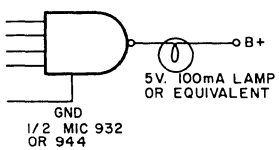
FIG. 67



MISCELLANEOUS APPLICATIONS

NOTE: In some of these applications, use of the elements is made within the design of the element but beyond the guaranteed test limits on page 23. Consult your sales representative for additional information and/or selection requirements.

5V V_{CC} 6.3 **FIG. 68**



LAMP DRIVING

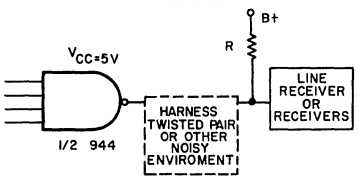
Suggested Ratings $T_A \leq 75°C$: Power Dissipation TO-5 400 mW Maximum—Power Dissipation Flatpak 240 mW Maximum.

Maximum "hot" lamp current		Maximum "hot" lamp current	
120 mA TO-5	one side only ON	90 mA TO-5	both sides ON
100 mA Flatpak	one side only ON	75 mA Flatpak	both sides ON

"Cold" lamp current is limited by saturation resistance, emitter resistance, and base current to about 200 to 250 mA.
The most significant thermal time constants for 932 and 944: TO-5 Package 50 msec Cerpak 100 msec.
Thermal time constant is measured by forward diode drop in one gate with power pulsed into opposite gate. A high current β selection is desirable in this application.

INTERFACING

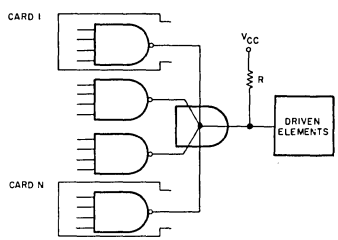
FIG. 69



B^+ up to 12 volts. Line Receiver may have nominal low level ≤ 1 volt; nominal threshold $\approx$ 4V and nominal high level $\geq 8V$, for example. Resistor selected should be as low as possible consistent with required low input level of receiver, number of receivers, and power dissipation of system. For a guaranteed V_{OH} level above 6 volts, an LV_{CE} selection may be desirable; for use of resistor that requires the 944 to sink more than 40 mA (at V_{OL} above .40 volt), a high current $I_{OL} - V_{OL}$ selection may be desirable.

POWER GATING

FIG. 70



Each output driver is ½ MIC 944. Note that the MIC 944 is a direct high fan-out replacement for MIC 930, except that an external resistor must be used.

RELIABILITY TESTS

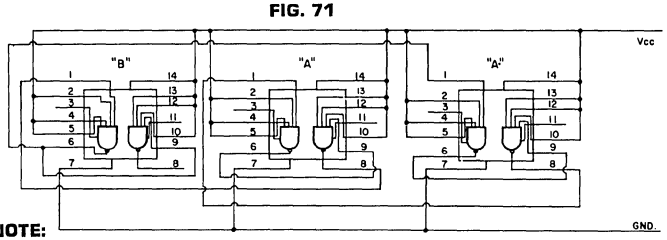
PERFORMED DURING ITT RELIABILITY PROGRAM

MEASUREMENTS OF THE FOLLOWING PARAMETERS ARE RECORDED:

	Parameter	Test Sequence Number on Page 20
932	V_{OL}	#1
	V_{OH}	#1
	I_R	#15 & #16
	I_F	#20 & #25
	I_{MAX}	#32
944	V_{OL}	#1
	I_R	#15
	I_R	#16
	I_F	#20
	I_F	#25
	I_{MAX}	#32
	I_{CEX}	#36

LIFE TEST CIRCUIT

FIG. 71



NOTE:
V_{CC} = +5.5 Volts Ambient Temperature = +125°C
Circuit may have any number of units connected like "A", with one connected like "B". The circuit must contain an odd number of gates in series in the ring.

EXTENDABLE HEX INVERTER MIC 935
HEX SINGLE-INPUT GATE MIC 936
FAST HEX SINGLE-INPUT GATE MIC 937

DESCRIPTION

The MIC 935, MIC 936, and MIC 937 elements are hex single-input inverters.

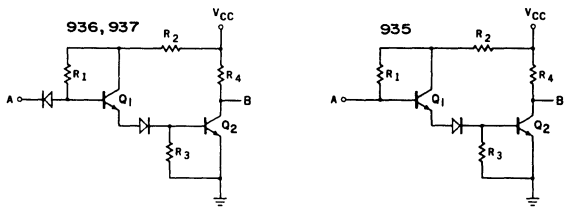
The MIC 935 is intended for use with discrete diode expansion of the input. When extending inputs with diodes, care should be taken to minimize capacitance on the input node.

These inverter gates can be cross-coupled to form a flip-flop or the outputs can be tied together to perform the "wired OR" function.

The MIC 936 incorporates a 6K output pull-up resistor which allows for a fan-out of up to 8 DTL loads.

The MIC 937 incorporates a 2K output pull-up resistor which typically results in a 30% faster rise time with capacitive loads at a fan-out of up to 7 DTL loads.

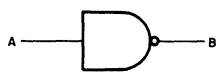
CIRCUIT SCHEMATICS
(ONE GATE ONLY)



TYPICAL RESISTOR VALUES

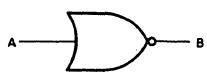
	935, 936	937
R_1 =	2.00K Ω	2.00K Ω
R_2 =	1.75K Ω	1.75K Ω
R_3 =	5.00K Ω	5.00K Ω
R_4 =	6.00K Ω	2.00K Ω

POSITIVE (NAND) LOGIC



$B = \overline{A}$

NEGATIVE (NOR) LOGIC



$B = \overline{A}$

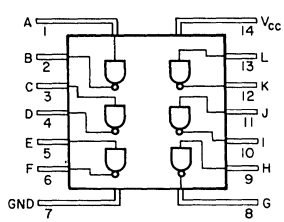
TRUTH TABLE

A	B
1	0
0	1

"1" IS HIGH
"0" IS LOW

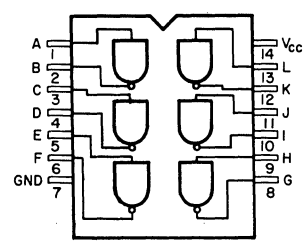
NOTE: POSITIVE LOGIC IS USED IN SPECIFICATION

FLAT PACK



TOP VIEW

DUAL IN-LINE



TOP VIEW

ABSOLUTE MAXIMUM RATINGS[1]

	UNITS
Supply Voltage (V_{CC}), −55°C to +125°C, Continuous ..... −1.5 to +8	Volts
Supply Voltage (V_{CC}), Pulsed, <1 sec. ..... +12	Volts
Output Current, Into Outputs 30	mA
Input Current (935) 5	mA
Input Forward Current ..... −10	mA
Input Reverse Current 1	mA
Operating Temperature ..... −55 to +125	°C
Storage Temperature ..... −65 to +150	°C
Operating Junction Temperature[2] ..... +175	°C
Input Voltage Applied to Input ..... −1.5 to +5.5	V
Lead Temp. (soldering, 60 sec.) 300	°C

NOTES: 1. Above which useful life may be impaired.

2. Allow 200°C/Watt θ_{J-A} for TO-5; 300°C/Watt θ_{J-A} for ¼" x ¼" flatpack and dual in-line. Allow 50°C/Watt θ_{J-C} for TO-5; 180°C/Watt θ_{J-C} for ¼" x ¼" flatpack and dual in-line. Heat removal in ¼" x ¼" flatpack is highly dependent upon contact surfaces or air flow and on lead attachment and thermal paths thru leads, as well as number of soldered leads.

SUMMARY OF MIC 936 AND 937 CHARACTERISTICS (25°C)

Parameter		Note	FULL TEMPERATURE RANGE			LIMITED TEMPERATURE RANGE			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Operating Supply Voltage		1	4.5	5.0	5.5		5.0		Volts
Network Dissipation	935	2			93.0			110.0	mW
	936	2			97.5			115.0	mW
	937				163.5			177.5	mW
Loading D.C. fan-out	935, 936				8.0			8.0	DTL Unit
	937				7.0			7.0	Load
Output Logic '1'	935, 936		2.6			2.6			Volts
Levels (High)	937		2.6			3.8			Volts
Output Logic 'O'	935, 936				0.4			0.45	Volts
Levels (Low)	937				0.4			0.50	Volts
Input Threshold '1'	936	3	1.9			1.9			Volts
	935	3	2.6						Volts
'O'					1.8			1.8	Volts
Propagation $t_{pd}+$	935, 936	4	25.0		80.0	25.0		80.0	Nanosec.
Delay Time	937		15.0		50.0	15.0		50.0	Nanosec.
$t_{pd}-$	936, 937		10.0		30.0	10.0		30.0	Nanosec.
	935		10.0		40.0				
Noise Immunity		5	350.0	>500.0		350.0	>500.0		mV

NOTES: 1. Exact specification limits for operating temperature range may be obtained by reference to the appropriate test.

2. Power supplied from V_{CC} (5V) during "ON" state fan-out = 0.

3. Input threshold voltage is defined as the minimum (or maximum) voltage at the circuit input to guarantee a low (or high) output.

4. Propogation delay time terms ($t_{pd}+$ and $t_{pd}-$) are described in the t_{pd} test circuit, Page 8.

5. See Loading Factors, Page 5.

FIG. 72

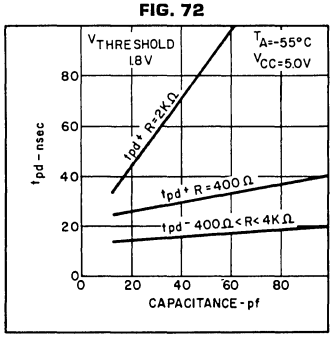


FIG. 73

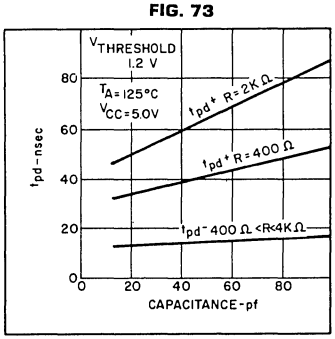
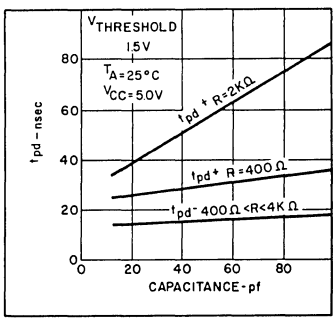


FIG. 74



TEST SEQUENCE*

Test No.	FORCING CONDITIONS AT PINS A L	B K	C J	D I	E H	F G	V_{CC}	Sense	TEST LIMITS Min.	Max.
1, (2)	V_{IH}	I_{OL1}	GND		GND		V_{CCL}	$V_B(V_K)$		V_{OL1}
3, (4)	GND		V_{IH}	I_{OL1}	GND		V_{CCL}	$V_D(V_I)$		V_{OL1}
5, (6)	GND		GND		V_{IH}	I_{OL1}	V_{CCL}	$V_F(V_G)$		V_{OL1}
7, (8)	V_F						V_{CCH}	$I_A(I_L)$		I_F
9, (10)			V_F				V_{CCH}	$I_C(I_J)$		I_F
11, (12)					V_F		V_{CCH}	$I_E(I_H)$		I_F
13, (14)	V_R						V_{CCH}	$I_A(I_L)$		I_R
15, (16)			V_R				V_{CCH}	$I_C(I_J)$		I_R
17, (18)					V_R		V_{CCH}	$I_E(I_H)$		I_R
19, (20)	V_{IL}	$-I_{OH}$					V_{CCL}	$V_B(V_K)$	V_{OH}	
21, (22)			V_{IL}	$-I_{OH}$			V_{CCL}	$V_D(V_K)$	V_{OH}	
23, (24)					V_{IL}	$-I_{OH}$	V_{CCL}	$V_F(V_G)$	V_{OH}	
25, (26)	V_{IL2}	V_{CEX}					V_{CEX}	$I_B(I_K)$		I_{CEX}
27, (28)			V_{IL2}	V_{CEX}			V_{CEX}	$I_D(I_I)$		I_{CEX}
29, (30)					V_{IL2}	V_{CEX}	V_{CEX}	$I_F(I_G)$		I_{CEX}
31, (32)	GND	GND					V_{CCH}	$I_B(I_K)$		$-I_{SC}$
33, (34)	GND	GND					V_{CCH}	$I_B(I_K)$	$-I_{SC}$	
35, (36)			GND	GND			V_{CCH}	$I_D(I_I)$		$-I_{SC}$
37, (38)			GND	GND			V_{CCH}	$I_D(I_I)$	$-I_{SC}$	
39, (40)					GND	GND	V_{CCH}	$I_F(I_G)$		$-I_{SC}$
41, (42)					GND	GND	V_{CCH}	$I_F(I_G)$	$-I_{SC}$	
43, (44)							V_{PD}	I_{VCC}		I_{pdh}
45	GND		GND		GND		V_{MAX}	I_{VCC}		I_{MAX}
46, 47	For $t_{pd}+$ and $t_{pd}-$ Conditions and Limits See Page 27.									
48, (49)	V_F						V_{CCL}	$I_A(I_L)$		$-I_{F2}$
50, (51)			V_F				V_{CCL}	$I_C(I_J)$		$-I_{F2}$
52, (53)					V_F		V_{CCL}	$I_E(I_H)$		$-I_{F2}$
54, (55)	V_{IH}	I_{OL2}					V_{CCH}	$V_B(V_K)$		V_{OL2}
56, (57)			V_{IH}	I_{OL2}			V_{CCH}	$V_D(V_I)$		V_{OL2}
58, (59)					V_{IH}	I_{OL2}	V_{CCH}	$V_F(V_G)$		V_{OL2}
60	GND		GND		GND		V_{PD}	I_{VCC}		I_{PDL}

FORCING CONDITIONS

FULL TEMPERATURE RANGE Parameter	Units	−55°C	+25°C	+125°C
V_{MAX}	Volts		8.0	
V_{PD}	Volts		5.0	
V_{CCH}	Volts	5.5	5.5	5.5
V_{CCL}	Volts	4.5	4.5	4.5
V_R	Volts	4.0	4.0	4.0
V_F	Volts	0.4	0.4	0.4
V_{IL} 936, 937	Volts	1.4	1.1	0.8
V_{IL} 935	Volts	2.1	1.8	1.5
V_{IL2}	Volts		0.0	
V_{IH} 936, 937	Volts	2.1	1.9	1.7
V_{IH} 935	Volts	2.8	2.6	2.4
V_{CEX}	Volts		4.5	
I_{OL1} 935, 936	mA	12.0	12.0	12.0
I_{OL1} 937	mA	10.8	10.8	10.8
I_{OL2} 935, 936	mA	15.0	15.0	15.0
I_{OL2} 937	mA	13.5	13.5	13.5
$-I_{OH}$ 935, 936	μA	180.0	180.0	180.0
I_{OH} 937	μA	0.54	0.54	0.54

LIMITED TEMPERATURE RANGE Parameter	Units	0°C	+25°C	+75°C
V_{MAX}	Volts		8.0	
V_{PD}	Volts		5.0	
V_{CCH}	Volts	5.0	5.0	5.0
V_{CCL}	Volts	5.0	5.0	5.0
V_R	Volts	4.0	4.0	4.0
V_F	Volts	0.45	0.45	0.5
V_{IL} 935	Volts	1.9	1.8	1.65
V_{IL} 936, 937	Volts	1.4	1.1	0.8
V_{IL2}	Volts		0.0	
V_{IH} 936, 937	Volts	2.1	1.9	1.7
V_{IH} 935	Volts	2.7	2.6	2.5
V_{CEX}	Volts		5.0	
I_{OL1} 936	mA	12.0	12.0	11.4
I_{OL1} 937	mA	10.5	10.5	10.2
I_{OL} 935, 936	mA	12.0	12.0	11.4
$-I_{OH}$	μA	120.0	120.0	120.0

*1. Ground pin is grounded for all tests.
2. Tests 45 and 60, all inputs are grounded simultaneously.
3. Tests 48/60 apply to full temperature units only.

TEST LIMITS

Parameter	Units	FULL TEMPERATURE RANGE						LIMITED TEMPERATURE RANGE					
		−55°C		+25°C		+125°C		0°C		+25°C		+75°C	
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.
V_{OL}(935, 936)	Volts		0.4		0.4		0.45		0.45		0.45		0.5
V_{OL} (937)	Volts		0.4		0.4		0.45		0.5		0.5		0.55
V_{OH}(935 936)	Volts	2.5		2.6		2.5		2.6		2.6		2.5	
V_{OH} (937)	Volts	2.5		2.6		2.5		4.3		4.3		4.2	
I_R	μA		2.0		2.0		5.0		5.0		5.0		10.0
$-I_F$	mA		1.5		1.5		1.4		1.4		1.4		1.33
I_{CEX}	μA				50.0						100.0		
$-I_{SC}$(935, 936)	mA	0.61	1.34	0.61	1.34	0.535	1.3	0.61	1.3	0.61	1.3	0.535	1.25
$-I_{SC}$ (937)	mA	2.1	3.7	2.1	3.7	1.86	3.28			1.85	3.68		
I_{PDH}(935, 936)	mA				19.2						23.0		
I_{PDH} (937)	mA				32.7						35.5		
I_{MAX}(935,936)	mA				16.5						24.0		
I_{MAX} (937)	mA				16.5						24.0		
$-I_{F2}$ (936, 937)	mA		1.16		1.16		1.08						
$-I_{F2}$ (935)	mA		1.2		1.2		1.2						
V_{OL2}	Volts		0.4		0.4		0.4						
I_{PDL}(936, 937)	mA				8.82								
I_{PDL} (935)	mA				10.2								

PROPAGATION DELAY

tpd TESTS

tpd TEST CIRCUIT MIC 936/937

FIG. 75

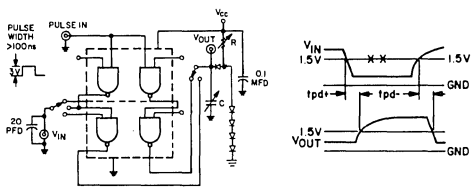


TABLE OF CONDITIONS & LIMITS tpd TESTS

(See Test Circuit.)

(V_{CC} = 5V, T = 25°C)

		R	C	Min.	Max.
$t_{pd}+$	936	3.9 K	30 pf	25 nsec	80 nsec
$t_{pd}-$	936	400 Ω	50 pf	10 nsec	30 nsec
$t_{pd}+$	936	400 Ω	50 pf	15 nsec	40 nsec[1]
$t_{pd}-$	936	3.9 K	20 pf	5 nsec	20 nsec[1]
$t_{pd}+$	937	3.9 K	30 pf	15 nsec	50 nsec
$t_{pd}-$	937	400 Ω	50 pf	10 nsec	30 nsec

NOTE: 1. Correlating limit provided as design information only.

RELIABILITY TESTS

PERFORMED DURING ITT RELIABILITY PROGRAM

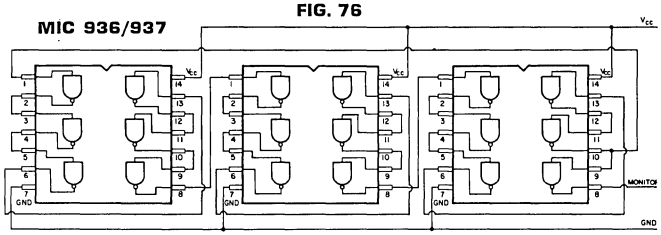
MEASUREMENTS OF THE FOLLOWING PARAMETERS ARE RECORDED:

Parameter	Test Sequence Number on Page 26
935/937 V_{OL}	#1, #2
I_R	#13, #14
I_F	#7, #8
V_{OH}	#19, #20
I_{MAX}	#45

LIFE TEST CIRCUITS

FIG. 76

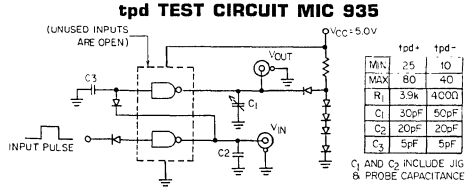
MIC 936/937



NOTES: 1. V_{CC}=5.5V 2. T_a= +125°C

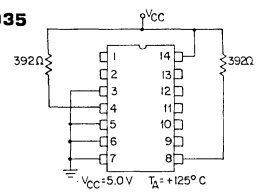
3. Ring must be made up of an odd number of inverters.

tpd TEST CIRCUIT MIC 935



	tpd+	tpd-
MIN.	25	10
MAX	80	40
R_1	3.9k	400Ω
C_1	30pF	50pF
C_2	20pF	20pF
C_3	5pF	5pF

MIC 935



QUAD TWO-INPUT GATE MIC 946
FAST QUAD TWO-INPUT GATE MIC 949

DESCRIPTION

The MIC 946 and MIC 949 elements are quad two-input NAND/NOR gates.

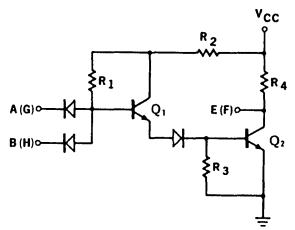
In addition to performing the positive NAND and negative NOR logic functions, the gates can be cross-coupled to form a flip-flop or the outputs can be tied together to perform the "wired OR" function.

These quad two-input gates can also be wired to perform the "exclusive OR" function, while two elements can be wired together to form a full adder.

The MIC 946 incorporates a 6K output pull-up resistor which allows for a fan-out of up to 8 DTL loads.

The MIC 949 incorporates a 2K output pull-up resistor which allows for typically 30% faster rise times with capacitive loads at a fan-out of up to 7 DTL loads.

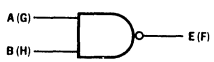
CIRCUIT SCHEMATIC
(ONE GATE ONLY)



TYPICAL RESISTOR VALUES

	946	949
R_1 =	2.00K Ω	2.00K Ω
R_2 =	1.75K Ω	1.75K Ω
R_3 =	5.00K Ω	5.00K Ω
R_4 =	6.00K Ω	2.00K Ω

POSITIVE (NAND) LOGIC



$E = \overline{A \cdot B}$

$F = \overline{G \cdot H}$

NEGATIVE (NOR) LOGIC

$E = \overline{A + B}$

$F = \overline{G + H}$

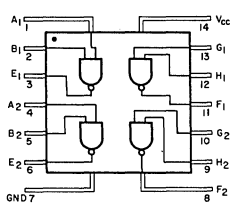
NOTE: POSITIVE LOGIC IS USED IN SPECIFICATION

TRUTH TABLE

A	B	E
G	H	F
I	I	O
O	I	I
I	O	I
O	O	I

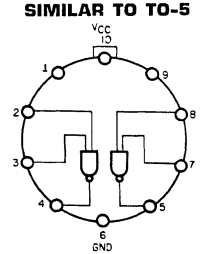
"I" IS HIGH
"O" IS LOW

FLAT PACK



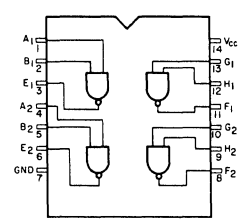
TOP VIEW

SIMILAR TO TO-5



TOP VIEW

DUAL IN-LINE



TOP VIEW

ABSOLUTE MAXIMUM RATINGS[1]

	UNITS
Supply Voltage (V_{CC}), −55°C to +125°C, continuous ..... −.5 to +8	Volts
Supply Voltage (V_{CC}), pulsed, <1 sec ..... +12	Volts
Output Current, into outputs 30	mA
Input Forward Current ..... −10	mA
Input Reverse Current 1	mA
Operating Temperature ..... −55 to +125	°C
Storage Temperature ..... −65 to +150	°C
Operating Junction Temperature[2] ..... +175	°C
Input Voltage Applied to Input ..... −1.5 to +5.5	Volts
Lead Temp. (soldering, 60 sec.) 300	°C

NOTES: 1. Above which useful life may be impaired.
2. Allow 200°C/Watt θ_{J-A} for TO-5; 300°C/Watt θ_{J-A} for ¼" x ¼" flatpack and dual in-line. Allow 50°C/Watt θ_{J-C} for TO-5; 180°C/Watt θ_{J-C} for ¼" x ¼" flatpack and dual in-line. Heat removal in ¼" x ¼" flatpack is highly dependent upon contact surfaces or air flow and on lead attachment and thermal paths thru leads, as well as number of soldered leads.

SUMMARY OF MIC 946 AND 949 CHARACTERISTICS (25°C)

Parameter		Note	FULL TEMPERATURE RANGE			LIMITED TEMPERATURE RANGE			Unit
			Min.	Typ	Max.	Min.	Typ.	Max.	
Operating Supply Voltage		1	4.5	5.0	5.5		5.0		Volts
Network Dissipation	946	2		35.0	65.0		35.0	80.0	mW
	949			50.0	109.0		50.0	117.0	
Loading D.C. fan-out	946				8.0			8.0	DTL Unit
	949				7.0			7.0	Load
Output Logic '1' (High)	946		2.6			2.6			Volts
Levels	949		2.6			4.3			Volts
'O' (Low)	946				0.4			0.45	Volts
	949				0.4			0.50	Volts
Input Threshold '1' (High)		3	1.9			1.9			Volts
'O' (Low)					1.1			1.1	
Propagation	946	4	25.0		80.0	25.0		80.0	Nano-
Delay Time t_{pd}+	949		15.0		50.0	15.0		50.0	Second
t_{pd}−			10.0		30.0	10.0		30.0	
Noise Immunity		5	350.0	>500.0		350.0	>500.0		mV

NOTES: 1. Exact specification limits for operating temperature range may be obtained by reference to the appropriate test.
2. Power supplied from V_{CC} supply (V_{CC} = 5V) during "ON" state, fan-out = 0.
3. Input threshold voltage is defined as the minimum (or maximum) voltage at the circuit input to guarantee a low (or high) output.
4. Propogation delay time terms (t_{pd}+ and t_{pd}−) are described in the t_{pd} test circuit, Page 8.
5. See Noise test circuit, Page 7, and Loading Factors, Page 5.

TIME DELAY VS. CAPACITIVE LOADS

FIG. 77

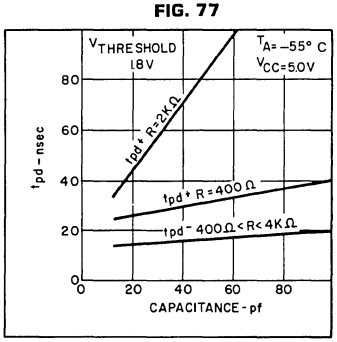


FIG. 78

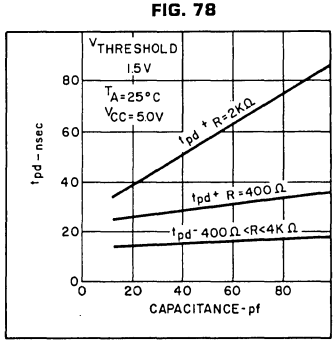
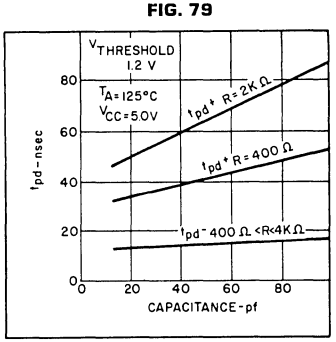


FIG. 79



TEST SEQUENCE

Both elements are "NAND" gates; therefore, the test sequences for each are identical. Tests on each side of the dual are identical; therefore, matching test and pin numbers are shown in parentheses.

Test No.	Notes	FORCING CONDITIONS AT PINS							Sense	TEST LIMITS	
		A_1 (G_1)	B_1 (H_1)	E_1 (F_1)	A_2 (G_2)	B_2 (H_2)	E_2 (F_2)	V_{CC}		Min.	Max.
1, (2)	1	V_{IH}	V_{IH}	I_{OL1}				V_{CCL}	V_{E1} (V_{F1})		V_{OL}
3, (4)	1				V_{IH}	V_{IH}	I_{OL1}	V_{CCL}	V_{E2} (V_{F2})		V_{OL}
5, (6)	1	V_{IL}		$-I_{OH}$				V_{CCL}	V_{E1} (V_{F1})	V_{OH}	
7, (8)	1		V_{IL}	$-I_{OH}$				V_{CCL}	V_{E1} (V_{F1})	V_{OH}	
9, (10)	1				V_{IL}		$-I_{OH}$	V_{CCL}	V_{E2} (V_{F2})	V_{OH}	
11, (12)	1					V_{IL}	$-I_{OH}$	V_{CCL}	V_{E2} (V_{F2})	V_{OH}	
13, (14)	1	V_R	GND					V_{CCH}	I_{A1} (I_{G1})		I_R
15, (16)	1	GND	V_R					V_{CCH}	I_{B1} (I_{H1})		I_R
17, (18)	1				V_R	GND		V_{CCH}	I_{A1} (I_{A2})		I_R
19, (20)	1				GND	V_R		V_{CCH}	I_{B2} (I_{H2})		I_R
21, (22)	1	V_F	V_R					V_{CCH}	I_{A1} (I_{G1})		$-I_F$
23, (24)	1	V_R	V_F					V_{CCH}	I_{B1} (I_{H1})		$-I_F$
25, (26)	1				V_F	V_R		V_{CCH}	I_{A2} (I_{G2})		$-I_F$
27, (28)	1				V_R	V_F		V_{CCH}	I_{B2} (I_{H2})		$-I_F$
29, (30)	1	V_{IL2}		V_{CEX}				V_{CEX}	I_{E1} (I_{F1})		I_{CEX}
31, (32)	1				V_{IL2}		V_{CEX}	V_{CEX}	I_{E2} (I_{F2})		I_{CEX}
33, (34)	1	GND		GND				V_{CCH}	I_{E1} (I_{F1})	$-I_{SC}$	
35, (36)	1				GND		GND	V_{CCH}	I_{E2} (I_{F2})	$-I_{SC}$	
37, (38)	1	GND		GND				V_{CCH}	I_{E1} (I_{F1})		$-I_{SC}$
39, (40)	1				GND		GND	V_{CCH}	I_{E2} (I_{F2})		$-I_{SC}$
41	1							V_{PD}	I_{VCC}		I_{PDH}
42	1, 2	GND			GND			V_{MAX}	I_{VCC}		I_{MAX}
43, 44		For $t_{pd}+$ and $t_{pd}-$ Conditions and Limits see Page 31.									
45, (46)	1,3	V_F	V_R					V_{CCL}	I_{A1} (I_{G1})		$-I_{F2}$
47, (48)	1,3	V_R	V_F					V_{CCL}	I_{B1} (I_{H1})		$-I_{F2}$
49, (50)	1,3				V_F	V_R		V_{CCL}	I_{A2} (I_{G2})		$-I_{F2}$
51, (52)	1,3				V_R	V_F		V_{CCL}	I_{B2} (I_{H2})		$-I_{F2}$
53, (54)	1,3	V_{IH}	V_{IH}	I_{OL2}				V_{CCH}	V_{E1} (V_{F1})		V_{OL2}
55, (56)	1, 3				V_{IH}	V_{IH}	I_{OL2}	V_{CCH}	V_{E2} (V_{F2})		V_{OL2}
57	1, 4	GND	GND		GND	GND		V_{PD}	I_{VCC}		I_{PDL}

NOTES: 1. Ground pin is grounded for all tests. 2. One input of each gate is grounded.
3. Tests 45/57 apply to full temperature range only. 4. Ground all inputs.

PROPAGATION DELAY

tpd TESTS

tpd TEST CIRCUIT

FIG. 80

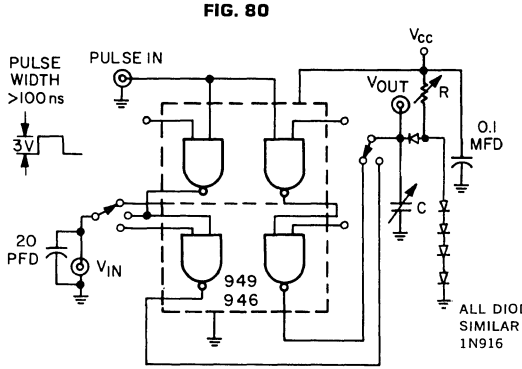


TABLE OF CONDITIONS & LIMITS tpd TESTS

(See Test Circuit.)
(V_{CC} = 5V, T = 25°C)

		R	C	Min.	Max.
$t_{pd}+$	946	3.9 K	30 pf	25 nsec	80 nsec
$t_{pd}-$	946	400 Ω	50 pf	10 nsec	30 nsec
$t_{pd}+$	946	400 Ω	50 pf	15 nsec	40 nsec[1]
$t_{pd}-$	946	3.9 K	20 pf	5 nsec	20 nsec[1]
$t_{pd}+$	949	3.9 K	30 pf	15 nsec	50 nsec
$t_{pd}-$	949	400 Ω	50 pf	10 nsec	30 nsec

NOTE: 1. Correlating limit provided as design information only.

TEST LIMITS

Parameter	Units	FULL TEMPERATURE RANGE						LIMITED TEMPERATURE RANGE					
		−55°C		+25°C		+125°C		0°C		+25°C		+75°C	
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.
V_{OL} (946)	Volts		0.40		0.40		0.45		0.45		0.45		0.5
V_{OL} (949)	Volts		0.40		0.40		0.45		0.50		0.50		0.55
V_{OH} (946)	Volts	2.50		2.60		2.50		2.60		2.60		2.50	
V_{OH} (949)	Volts	3.80		3.80		3.70		4.30		4.30		4.20	
I_R	μA		2.0		2.0		5.0		5.0		5.0		10.0
$-I_F$	mA		1.5		1.5		1.4		1.4		1.4		1.33
I_{CEX}	μA				50.0						100.0		
$-I_{SC}$ (946)	mA	0.61	1.34	0.61	1.34	0.535	1.30	0.61	1.30	0.61	1.30	0.535	1.25
$-I_{SC}$ (949)	mA	2.1	3.7	2.10	3.7	1.86	3.28			1.85	3.68		
I_{PDH} (946)	mA				12.5						16.0		
I_{PDH} (949)	mA				21.8						23.3		
I_{MAX} (946)	mA				11.0						16.0		
I_{MAX} (949)	mA				10.4						11.44		
V_{OL2} (946)	Volts		0.40		0.40		0.40						
V_{OL2} (949)	Volts		0.40		0.40		0.40						
$-I_{F2}$	mA		1.16		1.16		1.08						
I_{PDL} (949)	mA				5.88								

FORCING CONDITIONS

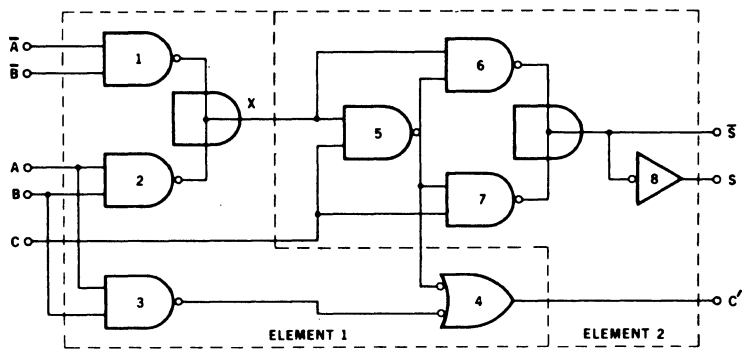
FULL TEMPERATURE RANGE					LIMITED TEMPERATURE RANGE				
Parameter	Units	−55°C	+25°C	+125°C	Parameter	Units	0°C	+25°C	+75°C
V_{MAX}	Volts		8.0		V_{MAX}	Volts		8.0	
V_{PD}	Volts		5.0		V_{PD}	Volts		5.0	
V_{CCH}	Volts	5.5	5.5	5.5	V_{CCH}	Volts	5.0	5.0	5.0
V_{CCL}	Volts	4.5	4.5	4.5	V_{CCL}	Volts	5.0	5.0	5.0
V_R	Volts	4.0	4.0	4.0	V_R	Volts	4.0	4.0	4.0
V_F	Volts	0.4	0.4	0.4	V_F	Volts	0.45	0.45	0.50
V_{IL}	Volts	1.4	1.1	0.8	V_{IL}	Volts	1.2	1.1	0.95
V_{IL2}	Volts		0.0		V_{IL2}	Volts		0.0	
V_{IH}	Volts	2.1	1.9	1.7	V_{IH}	Volts	2.0	1.9	1.8
V_{CEX}	Volts		4.5		V_{CEX}	Volts		5.0	
I_{OL1} 946	mA	12.0	12.0	12.0	I_{OL1} 946	mA	12.0	12.0	11.4
I_{OL1} 949	mA	10.8	10.8	10.8	I_{OL1} 949	mA	10.5	10.5	10.2
$-I_{OH}$ 946	μA	180.0	180.0	180.0	$-I_{OH}$	μA	120.0	120.0	120.0
$-I_{OH}$ 949	mA	.54	.54	.54					
I_{OL2} 946	mA	15.0	15.0	15.0					
I_{OL2} 949	mA	13.5	13.5	13.5					

APPLICATIONS

Most of the advantages in reducing element count and assembly cost by having four 2-Input gates in one package are obvious. Considering the large percentage of occurrences of fan-in 1 and 2 in the typical system, savings of 50% of elements needed to accomplish the fan-in 1 and 2 gating is substantial. However, some logic manipulation using the output "OR"ing capability may lead to yet greater savings. Thus, it is a further advantage of ITT Diode-Transistor Logic that the gates (MIC 930 Dual 4-Input Gate Element and MIC 946 Quad 2-Input Gate Element) may be output "OR"ed with fractional fan-out subtraction and without a separate gate with open collector required.
The example 1 , a 2-element full adder, shows the typical use of the Quad 2-Input Gate in an optimized logic configuration.

DESIGN OF A BINARY FULL ADDER

FIG. 81



The classical Binary Full Adder is often split into two half-adder circuits for economy. Such a mechanization, while slower, significantly reduces the logic circuitry involved. The arrangement given in 1 accomplishes all of the functions required of a full-adder with only two MIC 946 elements and introduces a logic delay of only four gate propagation times. All of the signals required for a "carry lookahead" organization are also present.
The rationale for this mechanization derives from the following factorization of the expressions for the full-adder sum (S) and carry (C). Output carry signals are distinguished from the carry input by a prime mark:

$$S = \bar{A}\bar{B}C + \bar{A}B\bar{C} + A\bar{B}\bar{C} + ABC$$
$$= (\bar{A}B + A\bar{B})\bar{C} + (\bar{A}\bar{B} + AB)C$$

$$C = \bar{A}BC + A\bar{B}C + AB\bar{C} + ABC$$
$$= (\bar{A}B + A\bar{B})C + AB(\bar{C} + C)$$
$$= (\bar{A}B + A\bar{B})C + AB$$

Note also that

$$(\bar{A}B + A\bar{B}) = \bar{A}B + A\bar{B}$$

It is apparent that the sum is the exclusive "OR" of the carry input with the result of the exclusive "OR" of the arguments A and B.
Two different exclusive "OR" circuits are used. In the first, composed of NAND Gates 1 and 2, it is assumed that both true and complement values of the arguments are available. The direct connection of the outputs at point X has logical effect; namely, that of ANDing the NAND outputs together.
Therefore, $\bar{A}B \cdot A\bar{B} = \bar{A}B + A\bar{B} = \bar{A}B + A\bar{B}$
The second exclusive "OR", composed of NAND Gates 5, 6, 7, and 8, requires only true inputs, avoiding the need for two inverters at its input.
Both the true and complement sum outputs are obtained by the "wired OR" connection and NAND Gate 8, which is used as an inverter.
The output of NAND Gate 5 is the term $(\bar{A}B + A\bar{B})C$ with the proper polarity for NOR Gate 4.
The remaining term of the carry originates in NAND Gate 3 with the proper polarity for NOR Gate 4. The output polarity of NOR Gate 4 is correct for a cascaded full-adder.

RELIABILITY TESTS

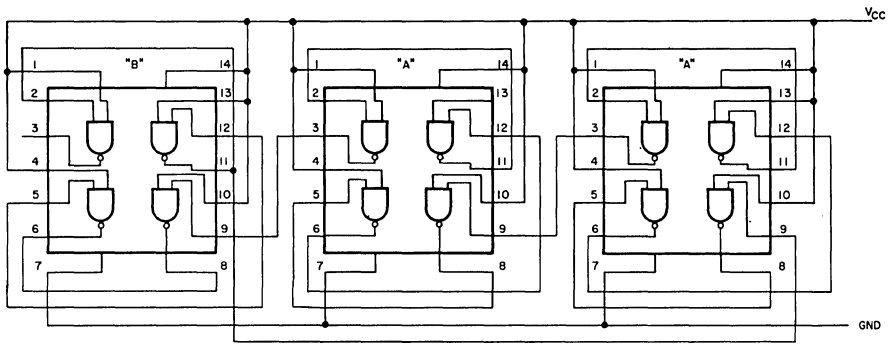
PERFORMED DURING ITT RELIABILITY PROGRAM

MEASUREMENTS OF THE FOLLOWING PARAMETERS ARE RECORDED:

Parameter	Test Sequence Number on Page 30
V_{OL}	#1
V_{OH}	#5
I_R	#13 & #15
I_F	#27 & #28
I_{MAX}	#42

LIFE TEST CIRCUIT

FIG. 82



NOTE: V_{CC} = +5.5 Volts Ambient Temperature = +125°C.
Circuit may have any number of units connected like "A", and one connected like "B". Circuit must contain an odd number of gates connected in series in the ring.

TRIPLE THREE-INPUT GATE MIC 962
FAST TRIPLE THREE-INPUT GATE MIC 963

DESCRIPTION

The MIC 962 and MIC 963 elements are triple three-input NAND/NOR gates.

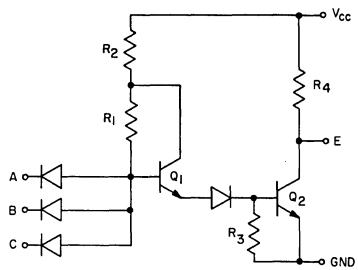
In addition to performing the positive NAND and negative NOR logic functions, the gates can be cross-coupled to form a flip-flop or the outputs can be tied together to perform the "wired OR" function.

These triple three-input gates can also be wired together to perform the "exclusive OR" function.

The MIC 962 incorporates a 6K output pull-up resistor which allows for a fan-out of up to 8 DTL loads.

The MIC 963 incorporates a 2K output pull-up resistor which typically results in a 30% faster rise time with capacitive loads at a fan-out of up to 7 DTL loads.

CIRCUIT SCHEMATIC
(ONE GATE ONLY)



TYPICAL RESISTOR VALUES

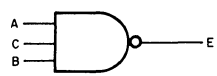
R_1 = 2.00 KΩ
R_2 = 1.75 KΩ
R_3 = 5.00 KΩ
R_4 = 6.00 KΩ (962)
R_4 = 2.00 KΩ (963)

TRUTH TABLE

A	B	C	E
1	1	1	0
0	1	1	1
1	0	1	1
1	1	0	1
0	0	0	1

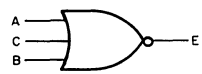
"1" is High Voltage.
"0" is Low Voltage.

POSITIVE (NAND) LOGIC



$E = \overline{A \cdot B \cdot C}$

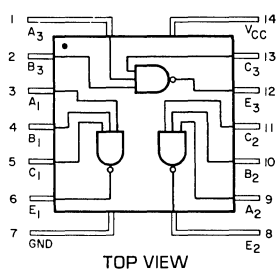
NEGATIVE (NOR) LOGIC



$E = \overline{A + B + C}$

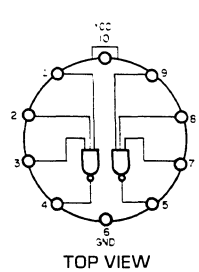
NOTE: Positive Logic is used in this specification.

FLAT PACK



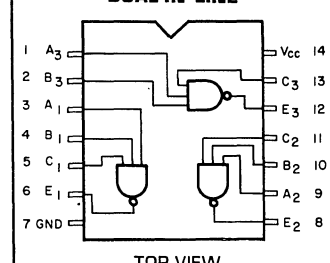
TOP VIEW

SIMILAR TO TO-5



TOP VIEW

DUAL IN-LINE



TOP VIEW

ABSOLUTE MAXIMUM RATINGS[1]

		UNITS
Supply Voltage (V_{CC}), −55°C to +125°C, continuous	−.5 to +8.0	Volts
Supply Voltage (V_{CC}), pulsed, <1 sec	+12	Volts
Output Current, into outputs	30	mA
Input Forward Current	−10	mA
Input Reverse Current	1	mA
Operating Temperature	−55 to +125	°C
Storage Temperature	−65 to +125	°C
Input Voltage Applied to Input	−1.5 to +5.5	Volts
Lead Temp. (soldering, 60 sec.)	300	°C

NOTES: 1. Above which useful life may be impaired.
2. Allow 200°C/Watt θ_{J-A} for TO-5; 300°C/Watt θ_{J-A} for ¼" x ¼" flatpack and dual in-line. Allow 50°C/Watt θ_{J-C} for TO-5; 180°C/Watt θ_{J-C} for ¼" x ¼" flatpack and dual in-line. Heat removal in ¼" x ¼" flatpack is highly dependent upon contact surfaces or air flow and on lead attachment and thermal paths thru leads, as well as number of soldered leads.

SUMMARY OF MIC 962 AND 963 CHARACTERISTICS (25°C)

Parameter		Note	FULL TEMPERATURE RANGE			LIMITED TEMPERATURE RANGE			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Operating Supply Voltage		1	4.5	5.0	5.5		5.0		Volts
Network Dissipation	962	2		25.5	48.8		25.5	60.0	mW
	963			37.5	81.5		37.5	88.5	
Loading D.C. fan-out	962				8.0			8.0	DTL Unit
	963				7.0			7.0	Load
Output Logic '1' (High)	962		2.6			2.6			Volts
	963		2.6			4.3			
'0' (Low)	962				0.4			0.45	
	963				0.4			0.5	
Input Threshold '1' (High		3	1.9			1.9			Volts
'0' (Low)					1.1			1.1	
Propogation	962	4	25.0		80.0	25.0		80.0	Nano-
Delay Time $t_{pd}+$	963		15.0		50.0	15.0		50.0	Second
	962		10.0		30.0	10.0		30.0	
$t_{pd}-$	963		10.0		30.0	10.0		30.0	
Noise Immunity		5	0.35	>0.5		0.35	>0.5		Volts

NOTES: 1. Exact specification limits for operating temperature range may be obtained by reference to the appropriate test.
2. Power supplied from V_{CC} (5V) during on state fan-out = 0.
3. Input threshold voltage is defined as the minimum (or maximum) voltage at the circuit input to guarantee a low (or high) output.
4. Propogation delay time terms ($t_{pd}+$ and $t_{pd}-$) are described in the t_{pd} test circuit, Page 8.
5. See noise test circuit, Page 7, and Loading Factors, Page 5.

TEST SEQUENCE

Both elements are triplet "NAND" gates; therefore, the test sequences for each are identical. Tests on each side of the triplet are identical; therefore, matching test and pin numbers are shown in parentheses.

Test No.	Notes	FORCING CONDITIONS AT PINS A_1 (A_2,A_3)	B_1 (B_2,B_3)	C_1 (C_2,C_3)	E_1 (E_2,E_3)	V_{CC}	Sense	TEST LIMITS Min.	Max.
1,(2,3)	1	V_{IH}	V_{IH}	V_{IH}	I_{OL1}	V_{CCL}	V_{E1}(V_{E2}, V_{E3})		V_{OL1}
4,(5,6)	1	V_R	GND	GND		V_{CCH}	I_{A1}(I_{A2}, I_{A3})		I_R
7,(8,9)	1	GND	V_R	GND		V_{CCH}	I_{B1}(I_{B2}, I_{B3})		I_R
10,(11,12)	1	GND	GND	V_R		V_{CCH}	I_{C1}(I_{C2}, I_{C3})		I_R
13,(14,15)	1	V_F	V_R	V_R		V_{CCH}	I_{A1}(I_{A2}, I_{A3})		$-I_{F1}$
16,(17,18)	1	V_R	V_F	V_R		V_{CCH}	I_{B1}(I_{B2}, I_{B3})		$-I_{F1}$
19,(20,21)	1	V_R	V_R	V_F		V_{CCH}	I_{C1}(I_{C2}, I_{C3})		$-I_{F1}$
22,(23,24)	1	V_{IL}			$-I_{OH}$	V_{CCL}	V_{E1}(V_{E2}, V_{E3})	V_{OH}	
25,(26,27)	1		V_{IL}		$-I_{OH}$	V_{CCL}	V_{E1}(V_{E2}, V_{E3})	V_{OH}	
28,(29,30)	1			V_{IL}	$-I_{OH}$	V_{CCL}	V_{E1}(V_{E2}, V_{E3})	V_{OH}	
31,(32,33)	1	GND			GND	V_{CCH}	I_{E1}(I_{E2}, I_{E3})	$-I_{SC}$	
34,(35,36)	1	GND			GND	V_{CCH}	I_{E1}(I_{E2}, I_{E3})		$-I_{SC}$
37,(38,39)	1		V_{IL2}		V_{CEX}	V_{CEX}	I_{E1}(I_{E2}, I_{E3})		I_{CEX}
40	1					V_{PD}	I_{VCC}		I_{PDH}
41	1, 2	GND				V_{MAX}	I_{VCC}		I_{MAX}
42 $t_{pd}+$				$t_{pd}+$ and $t_{pd}-$ See page 37 for test conditions and limits					
43 $t_{pd}-$									
44,(45,46)	1	V_F	V_R	V_R	V_{CEX}	V_{CCL}	I_{A1}(I_{A2}, I_{A3})		$-I_{F2}$
47,(48,49)	1	V_R	V_F	V_R		V_{CCL}	I_{B1}(I_{B2}, I_{B3})		$-I_{F2}$
50,(51,52)	1	V_R	V_R	V_F		V_{CCL}	I_{C1}(I_{C2}, I_{C3})		$-I_{F2}$
53,(54,55)	1	V_{IH}	V_{IH}	V_{IH}	I_{OL2}	V_{CCH}	V_{E1}(V_{E2}, V_{E3})		V_{OL2}
56,	1,3,4	GND	GND	GND		V_{PD}	I_{VCC}		I_{PDL}

NOTES: 1. Ground pin is grounded for all tests.
2. One input of all four gates is grounded.
3. Tests 44/56 apply to full temperature range only.
4. Ground all inputs.

FORCING CONDITIONS

FULL TEMPERATURE RANGE					LIMITED TEMPERATURE RANGE				
Parameter	Units	−55°C	+25°C	+125°C	Parameter	Units	0°C	+25°C	+75°C
V_{CCH}	Volts	5.5	5.5	5.5	V_{CCH}	Volts	5.0	5.0	5.0
V_{CCL}	Volts	4.5	4.5	4.5	V_{CCL}	Volts	5.0	5.0	5.0
V_{MAX}	Volts		8.0		V_{MAX}	Volts		8.0	
V_{PD}	Volts		5.0		V_{PD}	Volts		5.0	
V_R	Volts	4.0	4.0	4.0	V_R	Volts	4.0	4.0	4.0
V_F	Volts	0.4	0.4	0.4	V_F	Volts	0.45	0.45	0.5
V_{CEX}	Volts		4.5		V_{CEX}	Volts		5.0	
V_{IL}	Volts	1.4	1.1	0.8	V_{IL}	Volts	1.20	1.10	0.95
V_{IL2}	Volts		0.0		V_{IL2}	Volts		0.0	
V_{IH}	Volts	2.1	1.9	1.7	V_{IH}	Volts	2.0	1.9	1.8
I_{OL1} 962	mA	12.0	12.0	12.0	I_{OL1} 962	mA	12.0	12.0	11.4
I_{OL1} 963	mA	10.8	10.8	10.8	I_{OL1} 963	mA	10.5	10.5	10.2
$-I_{OH}$ 962	μA	180.0	180.0	180.0	$-I_{OH}$	μA	120.0	120.0	120.0
$-I_{OH}$ 963	mA	.54	.54	.54					
I_{OL2} 962	mA	15.0	15.0	15.0					
I_{OL2} 963	mA	13.5	13.5	13.5					

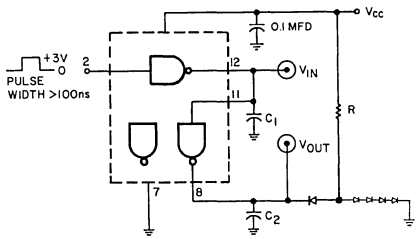
TEST LIMITS

		FULL TEMPERATURE RANGE						LIMITED TEMPERATURE RANGE					
		−55°C		+25°C		+125°C		0°C		+25°C		+75°C	
Parameter	Units	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.
V_{OL1} (962)	Volts		0.4		0.4		0.40		0.45		0.45		0.5
V_{OL1} (963)	Volts		0.4		0.4		0.40		0.5		0.5		0.55
V_{OH} (962)	Volts	2.5		2.6		2.5		2.6		2.6		2.5	
V_{OH} (963)	Volts	2.5		2.6		2.5		4.3		4.3		4.2	
I_R	μA		2.0		2.0		5.0		5.0		5.0		10.0
$-I_{F1}$	mA		1.5		1.5		1.4		1.4		1.4		1.33
$-I_{SC}$ (962)	mA	0.61	1.34	0.61	1.34	0.535	1.30	0.61	1.30	0.61	1.30	0.535	1.25
$-I_{SC}$ (963)	mA	2.10	3.70	2.10	3.70	1.86	3.28			1.85	3.68		
I_{CEX}	μA				50.0						100.0		
I_{PDH} (962)	mA				9.75						12.0		
I_{PDH} (963)	mA				16.3						17.7		
I_{MAX} (962)	mA				8.25						12.0		
I_{MAX} (963)	mA				7.8						8.6		
$-I_{F2}$	mA		1.16		1.16		10.8						
V_{OL2}	Volts		0.4		0.4		0.4						
I_{PDL}	mA				4.41								

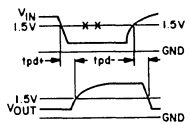
PROPAGATION DELAY

tpd TEST CIRCUIT

FIG. 83



tpd TESTS



t_{pd}— of 962 and 963 elements will be read from input at 1.5V.

All diodes 1N916 or equivalent.

C_1 and C_2 includes probe and jig capacitance.

$V_{Threshold}$= 1.5V at 25°C; at other temperatures $V_{Threshold}$ will be stated.

TABLE OF CONDITIONS & LIMITS tpd TESTS

(See Test Circuit.)

(V_{CC} = 5.0 V, T_A = 25°C)

		R ohms	C_1 pf	C_2 pf	Min. nsec	Max. nsec
$t_{pd}+$	962	3.9K	20	30	25	80
$t_{pd}-$	962	400	20	50	10	30
$t_{pd}+$	963	3.9K	20	30	15	50
$t_{pd}-$	963	400	20	50	10	30

RELIABILITY TESTS

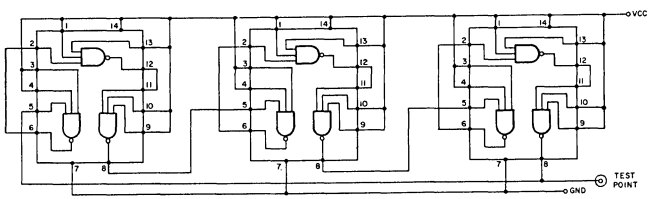
PERFORMED DURING ITT RELIABILITY PROGRAM

MEASUREMENTS OF THE FOLLOWING PARAMETERS ARE RECORDED:

Parameter	Test Sequence Number on Page 36
V_{OL}	#1
V_{OH}	#7, #8, & #9
I_F	#16, #17, & #18
I_R	#22
I_{CEX}	#41

LIFE TEST CIRCUIT

FIG. 84



NOTES: V_{CC} = +5.5 Volts Ambient Temperature = +125°C

The circuit must contain an odd number of gates connected serially in a ring.

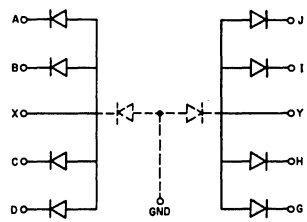
DUAL FOUR-INPUT EXTENDER MIC 933

DESCRIPTION

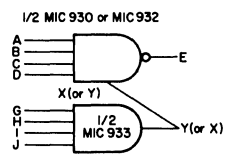
The MIC 933 element is a dual four-input extender. The MIC 933 consists of two independent diode arrays identical in every respect to the input diodes of the DTL gates and buffer elements. It can be used to extend the fan-in capability to more than 20 without adversely affecting the noise immunity or load driving capability of the elements to which they are connected. Good practice dictates that extension interconnection paths be as short as possible to minimize the effects of distributed capacitance on circuit performance. The MIC 933 has a typical input capacitance of 2pf and an output capacitance of 5 pf.

The MIC 933 can extend the fan-in of the MIC 930, 932, 944, and 961 elements.

CIRCUIT SCHEMATIC

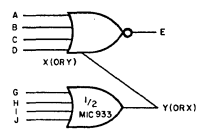


POSITIVE (NAND) LOGIC



POSITIVE LOGIC $E = \overline{ABCDGHIJ}$

NEGATIVE (NOR) LOGIC



NEGATIVE LOGIC $E = \overline{A+B+C+D+G+H+I+J}$

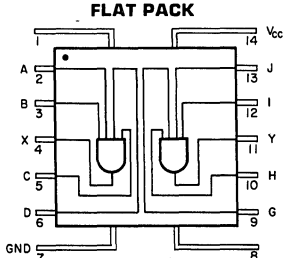
NOTE: Positive logic is used in this specification.

TRUTH TABLE

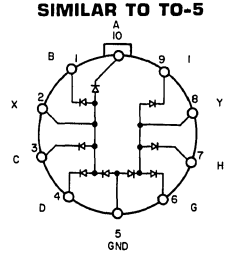
A	B	C	D	X
G	H	I	J	Y
I	I	I	I	I
O	I	I	I	O
I	O	I	I	O
I	I	O	I	O
I	I	I	O	O
O	O	O	O	O

I is High
O is Low

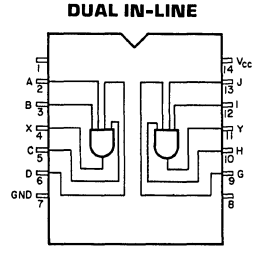
FLAT PACK



SIMILAR TO TO-5



DUAL IN-LINE



ABSOLUTE MAXIMUM RATINGS[1]

	UNITS
Supply Voltage (V_{CC}), −55°C to + 125°C, continuous ..... −.5 to +8	Volts
Supply Voltage (V_{CC}), pulsed <1.0 sec ..... +12	Volts
Input Forward Current, I_F ..... −10	mA
Input Reverse Current, I_R 1	mA
Operating Temperature Range ..... −55 to −125	°C
Storage Temperature Range ..... −65 to −150	°C
Operating Junction Temperature[2] ..... +175	°C
Input Voltage Applied to Input ..... −1.5 to +5.5	Volts
Lead Temp. (soldering, 60 sec.) 300	°C

NOTES: 1. Above which useful life may be impaired.

2. Allow 200°C/Watt θ_{J-A} for TO-5; 300°C/Watt θ_{J-A} for ¼" x ¼" flatpack and dual in-line. Allow 50°C/Watt θ_{J-C} for TO-5; 180°C/Watt θ_{J-C} for ¼" x ¼" flatpack and dual in-line. Heat removal in ¼" x ¼" flatpack is highly dependent upon contact surfaces or air flow and on lead attachment and thermal paths thru leads, as well as number of soldered leads.

TEST SEQUENCE

Test No.	Note	Pin A (G)	Pin B (H)	Pin C (I)	Pin D (J)	Pin X (Y)	Sense	Symbol
1,2,3,4, (5,6,7,8)	2,3,4	GND	GND	GND	GND	I_{FD}	$V_X(V_Y)$	V_{FD}
11,(12)	3	V_R	GND	GND	GND	—	$I_A(I_G)$	I_{R1}
13,(14)	3	GND	V_R	GND	GND	—	$I_B(I_H)$	I_{R2}
15,(16)	3	GND	GND	V_R	GND	—	$I_C(I_I)$	I_{R3}
17,(18)	3	GND	GND	GND	V_R	—	$I_D(I_J)$	I_{R4}
19,(20)	3	—	—	—	—	V_R	$I_X(I_Y)$	$5I_R$

NOTES:

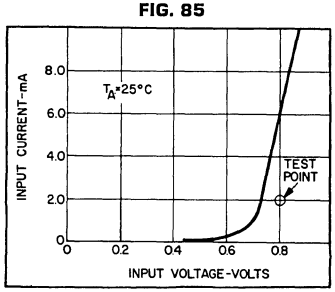
1. Forcing Conditions { V_R = 4.0 volts, I_{FD} = 2.0 mA (0 to +75°C); V_R = 4.0 volts, I_{FD} = 2.0 mA (−55 to +125°C)
2. The MIC 933 is a dual element. Tests for each side are identical. Matching tests and pin numbers are shown in parenthesis.
3. The ground pin is grounded on all tests.
4. Ground applied individually to one input, each test. Other inputs open.

TEST LIMITS

		FULL TEMPERATURE RANGE						LIMITED TEMPERATURE RANGE					
		−55°C		+25°C		+125°C		0°C		+25°C		+75°C	
Parameter	Units	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.
V_{FD}	Volts	.840	.980	.700	.820	.480	.620	.700	.900	.660	.840	.560	.760
I_R	μA		2.0		2.0		5.0		5.0		5.0		10.0
$5I_R$	μA		10.0		10.0		25.0		25.0		25.0		50.0

FORWARD VOLTAGE VERSUS FORWARD CURRENT +25°C

FIG. 85



TYPICAL CURVES

TO SHOW THE EFFECTS OF EXTENDER PIN CAPACITANCE (RESULTING FROM USE OF MIC 933) ON TIME DELAY OF MIC 930 DUAL GATE AND MIC 932 DUAL BUFFER

FIG. 86

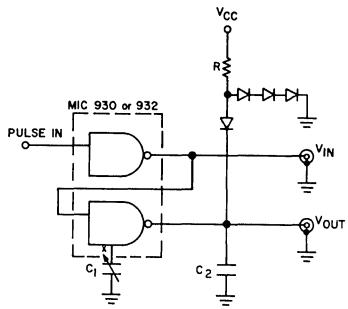


FIG. 87

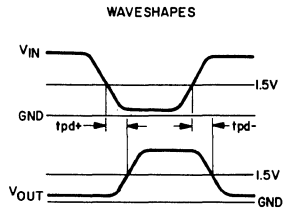


FIG. 88

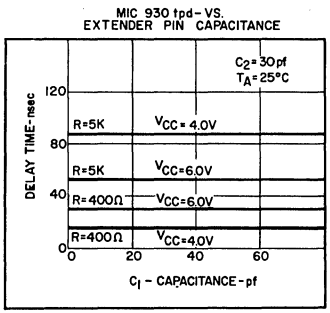


FIG. 89

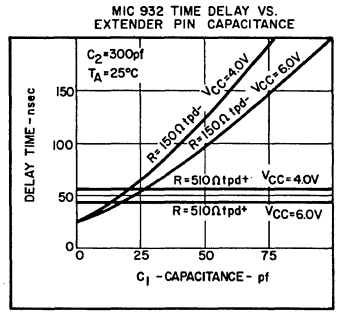
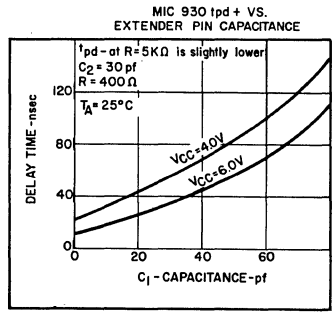


FIG. 90



NOTE:
C_1 represents the summation of the MIC 933 Dual Extender Element output capacitances (≈ 5 pf per output) and associated board, connector and wiring capacitances.

TO SHOW THE EFFECTS OF EXTENDER PIN CAPACITANCE ON NOISE THRESHOLD OF MIC 930 DUAL GATE

FIG. 91

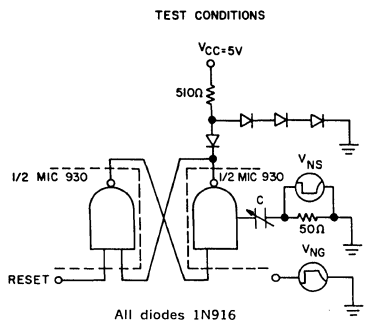


FIG. 92

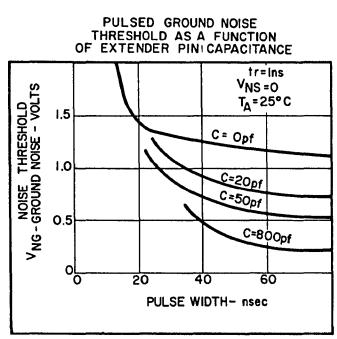
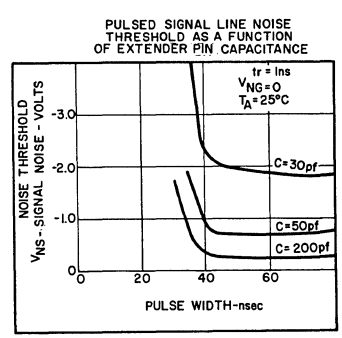


FIG. 93



ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage (V_{CC}), −55°C to +125°C, Continuous ..... −.5 to +8	Volts
Supply Voltage (V_{CC}), pulsed, <1.0 sec. ..... +12	Volts
Output Current, into Outputs, Continuous 50	mA
Output Current, into Outputs, pulsed, <30 milliseconds 100	mA
Input Forward Current, Pins 1, 4, 10, 13 (flat package) ..... −10	mA
Input Reverse Current 5.0	mA
Input Voltage, Pins 5, 6 (flat package) ..... −1.0 to +8.0	Volts
Operating Ambient Temperature ..... −55 to +125	°C
Storage Temperature ..... −65 to +150	°C
Operating Junction Temperature[2] ..... +175	°C
Input Voltage Applied to Input ..... −1.5 to +5.5	V
Lead Temp. (soldering, 60 sec.) 300	°C

NOTES: 1. Above which useful life may be impaired.

2. Allow 200°C/Watt θ_{J-A} for TO-5; 300°C/Watt θ_{J-A} for ¼" x ¼" flatpack and dual in-line. Allow 50°C/Watt θ_{J-C} for TO-5; 180°C/Watt θ_{J-C} for ¼" x ¼" flatpack and dual in-line. Heat removal in ¼" x ¼" flatpack is highly dependent upon contact surfaces or air flow and on lead attachment and thermal paths thru leads, as well as number of soldered leads.

SUMMARY OF MIC 950 CHARACTERISTICS (25° C)

Network Parameter	Note	MILITARY Min.	MILITARY Typ.	MILITARY Max.	INDUSTRIAL Min.	INDUSTRIAL Typ.	INDUSTRIAL Max.	Unit
Operating Supply Voltage	1	4.5	5.0	5.5		5.0		Volts
Network Dissipation	2			43.5			46.5	mW
Loading D.C. Fanout				8.0			10.0	DTL Unit Load
Output Logic '1' (High)		2.6			2.8			Volts
'O' (Low)				0.4			0.45	
Input D.C. Threshold '1' (High)	3	1.9			1.9			Volts
'O' (Low)				0.8			0.78	
Propagation Delay Time $t_{pd}+$	4			30.0			35.0	Nano-Second
$t_{pd}-$				30.0			35.0	

NOTES: 1. Exact specification limits for operating temperature range may be obtained by reference to the appropriate test.

2. Power supplied from V_{CC} (5V) fanout = 0.

3. Input threshold voltage is defined as the minimum (or maximum) voltage at the ciruit input to guarantee a low (or high) output.

4. Propagation delay time terms ($t_{pd}+$ and $t_{pd}-$) are described in the t_{PD} test circuit, Page 10.

FREQUENCY CHARACTERISTICS

FIG. 104

TYPICAL FREQUENCY OF OPERATION VS. LOADING CAPACITANCE

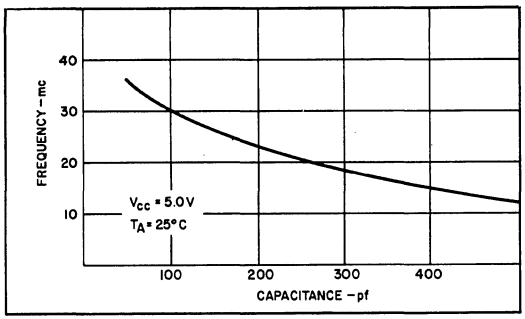
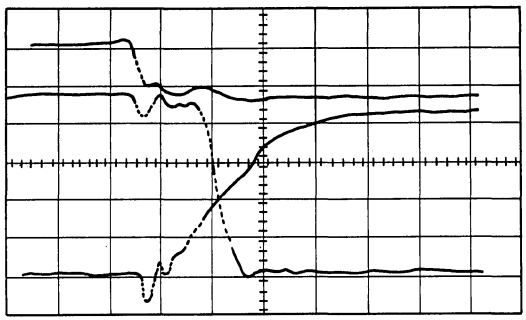


FIG. 105

MIC 950 – DIVIDING BY 2

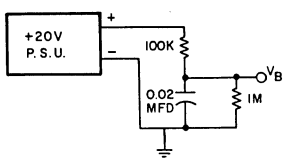


10 nsec/division
25°C V_{CC} = 5.0 V
UPPER TRACE – Input to CP (2 volts/division)
POSITIVE GOING TRACE – Output Going High (1 volt/division)
NEGATIVE GOING TRACE – Output Going Low (1 volt/division)
20 pf each output

TEST SEQUENCE

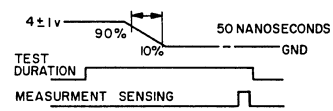
Test No.	Notes	FORCING CONDITIONS AT PINS												DIP	TEST LIMITS	
		1	2	3	4	5	6	10	11	12	13	14		DIP		
		1		2	3	4	5	7	8		9	10	TO5	Sense		
		C_D		Q	S_2	S_1	C_1	C_2	$\overline{Q}$		S_D	V_{CC}	Sense		Min.	Max.
1	1, 2				GND	V_B						V_{CCH}	V_4	V_5	2V	
2	1				GND	V_{MAX}						V_{CCH}	I_4	I_5		I_R
3	1, 2						V_B	GND				V_{CCH}	V_5	V_6	2V	
4	1						V_{MAX}	GND				V_{CCH}	I_5	I_6		I_R
5	1, 3	V_R			V_{CCH}		CP	GND				V_{CCH}	I_1	I_1		I_R
6	1, 3				GND	CP		V_{CCH}			V_R	V_{CCH}	I_9	I_{13}		I_R
7	1			V_{CEX}							GND	V_{CEX}	I_2	I_3		I_{CEX}
8	1	GND							V_{CEX}			V_{CEX}	I_8	I_{11}		I_{CEX}
9	1											V_{CCH}	V_3	V_4	V_L	
10	1											V_{CCH}	V_7	V_{10}	V_L	
11	1				GND			GND				V_{MAX}	I_{10}	I_{14}		I_{MAX}
12	1				GND							V_{PD}	I_{10}	I_{14}		I_{PD}
13	1	GND		I_{OL1}	GND						V_{IHS}	V_{CCL}	V_2	V_3		V_{OL1}
14	1	GND		I_{OL2}								V_{CCH}	V_2	V_3		V_{OL2}
15	1	V_{IHS}						GND	I_{OL1}		GND	V_{CCL}	V_8	V_{11}		V_{OL1}
16	1								I_{OL2}		GND	V_{CCH}	V_8	V_{11}		V_{OL2}
17	1, 3			$-I_{OH}$		CP	CP	GND			V_{ILS}	V_{CCL}	V_2	V_3	V_{OH}	
18	1, 3	V_{ILS}			GND	CP	CP		$-I_{OH}$			V_{CCL}	V_8	V_{11}	V_{OH}	
19	1				V_F							V_{CCH}	I_3	I_4		$-1.5I_{F_1}$
20	1							V_F				V_{CCH}	I_7	I_{10}		$-1.5I_{F_1}$
21	1	V_F									GND	V_{CCH}	I_1	I_1		$-I_{FS1}$
22	1	GND									V_F	V_{CCH}	I_9	I_{13}		$-I_{FS1}$
23	1			GND							GND	V_{CCH}	I_2	I_3	$-I_{SC}$	
24	1			GND							GND	V_{CCH}	I_2	I_3		$-I_{SC}$
25	1	GND							GND			V_{CCH}	I_8	I_{11}	$-I_{SC}$	
26	1	GND							GND			V_{CCH}	I_8	I_{11}		$-I_{SC}$
27	1		GND									V_{CCH}		I_2	I_{1K}	
28	1		GND									V_{CCH}		I_2		I_{1K}
29	1									GND		V_{CCH}		I_{12}	I_{1K}	
30	1									GND		V_{CCH}		I_{12}		I_{1K}
31	$t_{pd}+$	See Page 52 for Test Limits and Conditions.														
32	$t_{pd}-$	See Page 52 for Test Limits and Conditions.														
33	20MHZ	See Page 52 for Test Circuit.														
34	1, 4				V_F							V_{CCL}	I_3	I_4		$-1.5I_{F2}$
35	1, 4							V_F				V_{CCL}	I_7	I_{10}		$-1.5I_{F2}$
36	1, 4	V_F									GND	V_{CCL}	I_1	I_1		$-I_{FS2}$
37	1, 4	GND									V_F	V_{CCL}	I_9	I_{13}		$-I_{FS2}$

FIG. 106



NOTES:
1. GROUND PIN IS GROUNDED FOR ALL TESTS.
2. V_B FOR TESTS 1 & 3.
3. CLOCK PULSE FOR TESTS 5,6,17 & 18
4. 34/37 APPLY TO FULL TEMPERATURE RANGE.

FIG. 107



FORCING CONDITIONS

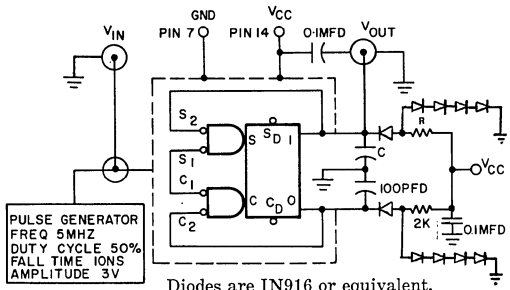
FULL TEMPERATURE RANGE					LIMITED TEMPERATURE RANGE				
Parameter	Units	−55°C	+25°C	+125°C	Parameter	Units	0°C	+25°C	+75°C
V_{CCH}	Volts	5.5	5.5	5.5	V_{CCH}	Volts	5.0	5.0	5.0
V_{CCL}	Volts	4.5	4.5	4.5	V_{CCL}	Volts	5.0	5.0	5.0
V_{MAX}	Volts	8.0	8.0	8.0	V_{MAX}	Volts	8.0	8.0	8.0
V_R	Volts	4.0	4.0	4.0	V_R	Volts	4.0	4.0	4.0
V_{CEX}	Volts	5.0	5.0	5.0	V_{CEX}	Volts	5.0	5.0	5.0
V_{PD}	Volts	5.0	5.0	5.0	V_{PD}	Volts	5.0	5.0	5.0
V_{IHS}	Volts	2.1	1.9	1.7	V_{IHS}	Volts	2.0	1.9	1.8
V_{ILS}	Volts	0.95	0.8	0.605	V_{ILS}	Volts	0.883	0.78	0.73
V_F	Volts	0.4	0.4	0.4	V_F	Volts	.45	.45	.5
I_{OL1}	mA	12.0	12.0	12.0	I_{OL1}	mA	14.0	14.0	13.3
I_{OL2}	mA	15.0	15.0	15.0	I_{OL2}	mA	14.0	14.0	14.0
$-I_{OH}$	mA	1.5	1.5	1.5	$-I_{OH}$	mA	1.5	1.5	1.5

TEST LIMITS

		FULL TEMPERATURE RANGE						LIMITED TEMPERATURE RANGE					
		−55°C		+25°C		+125°C		0°C		+25°C		+75°C	
Parameter	Units	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.
V_{OL1}	Volts		0.4		0.4		0.4		0.45		0.45		0.5
V_{OL2}	Volts		0.4		0.4		0.4		0.45		0.45		0.5
V_L	Volts	5.0		5.0		5.0		4.0		4.0		4.0	
V_{OH}	Volts	2.5		2.6		2.5		2.7		2.8		2.7	
I_R	μA		2.0		2.0		5.0		5.0		5.0		10.0
I_{CEX}	μA		50.0		50.0		100.0		100.0		100.0		100.0
I_{MAX}	mA		18.4		18.4		18.4		19.6		19.6		19.6
$-1.5\ I_{F1}$	mA		2.22		2.22		2.09		2.1		2.1		2.0
$-I_{FS1}$	mA		1.64		1.64		1.46		1.6		1.6		1.52
$-I_{SC}$	mA	12.6	27.0	15.7	27.0	14.0	26.0	13.7	29.3	13.7	29.3	12.6	29.3
$-I_{IK}$	mA	4.05			7.35	4.22	7.35	3.65	7.9	3.7	7.9	3.4	7.9
I_{PD}	mA		8.7		8.7		8.7		9.3		9.3		9.3
$-1.5\ I_{F2}$	mA		1.83		1.83		1.71						
$-I_{FS2}$	mA		1.2		1.24		1.14						

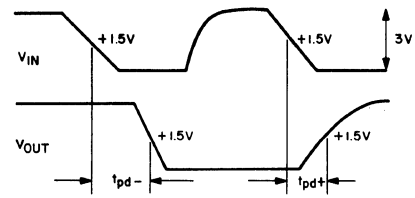
MIC 950 PROPAGATION DELAY TEST CIRCUIT AND LIMITS

FIG. 108



Diodes are IN916 or equivalent.
Capacitances include wiring and probe capacitances.

FIG. 109

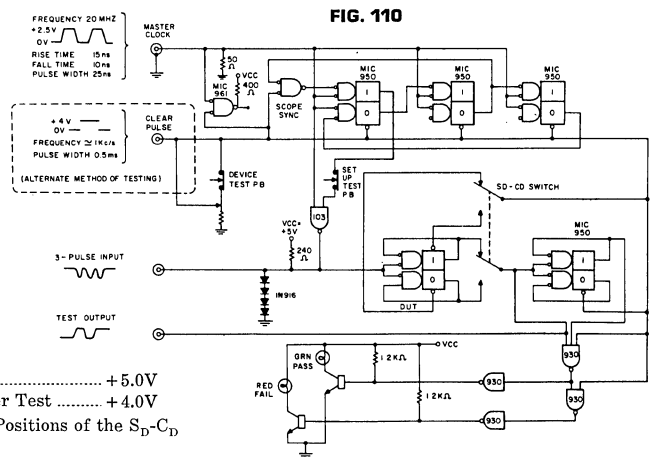


TEST CONDITIONS							FULL TEMPERATURE RANGE	LIMITED TEMPERATURE RANGE
Test No.	Device	Test	R Ohms	C Picofarad	T °C	V_{CC} Volts	Min. Max. Nanoseconds	Min. Max. Nanoseconds
31	950	$t_{pd}+$	3.9K	100	+25°C	5.0	30	35
32	950	$t_{pd}-$	390	100	+25°C	5.0	30	35

TEST CIRCUIT

20 MHZ (3 PULSE) TOGGLE TEST

FIG. 110



V_{CC} For Test Circuit ..... +5.0V
V_{CC} For MIC 950 Under Test ..... +4.0V
Test Device For Both Positions of the S_D-C_D Switch.
Suitable Precautions Must Be Used When Wiring Test Jig.

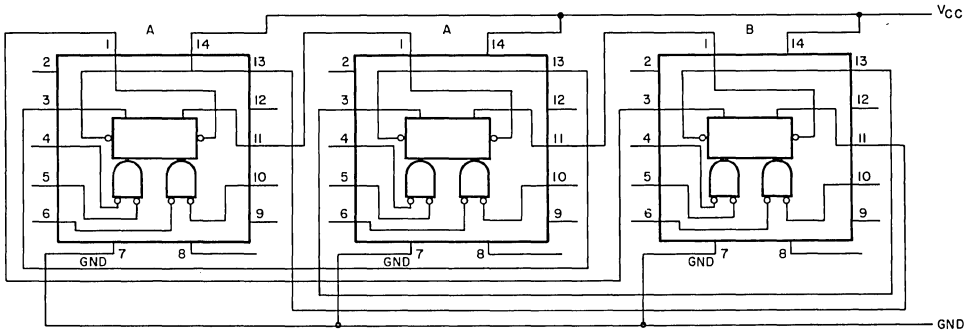
RELIABILITY TESTS

PERFORMED DURING ITT RELIABILITY PROGRAM
MEASUREMENTS OF THE FOLLOWING PARAMETERS ARE RECORDED:

Parameter	Test Sequence Number on Page 50
I_R	#2 & #6
I_{MAX}	#11
V_{OL}	#15
V_{OH}	#17
$-I_{FS}$	#21 & #22

LIFE TEST CIRCUIT

FIG. 111



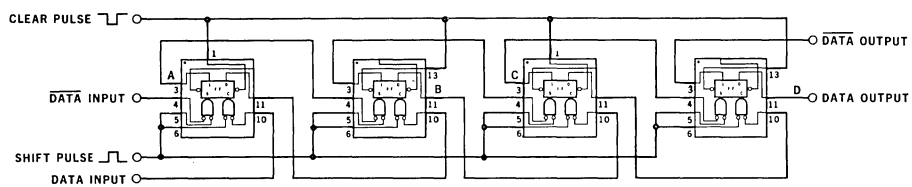
NOTE:

V_{CC} = +5.5 Volts Ambient Temperature = +125°C
Circuit may have an odd number of units connected like "A", with one connected like "B"

APPLICATIONS

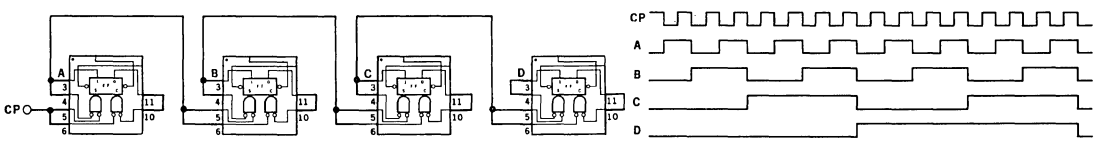
SHIFT REGISTER

FIG. 112



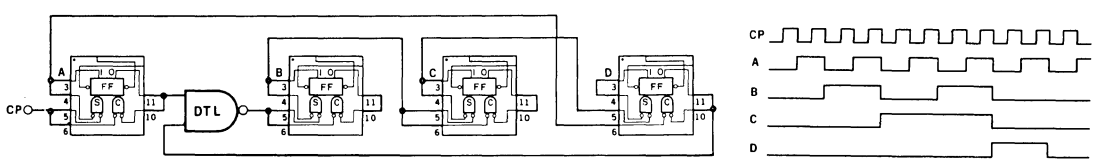
RIPPLE-CARRY BINARY COUNTER

FIG.113



RIPPLE-CARRY DECADE COUNTER

FIG. 114



DUAL FLIP-FLOPS

MIC 9093 MIC 9094 MIC 9097 MIC 9099
DUAL DTL MASTER-SLAVE J-K FLIP-FLOPS

DESCRIPTION

The MIC 9093 and MIC 9094 are single chip dual flip-flops with circuitry similar to the MIC 945 and MIC 948 respectively. They feature internal J-K connections, separate clock pins, and separate SD pins. They are useful in ripple-carry counters and many other J-K flip-flop applications.

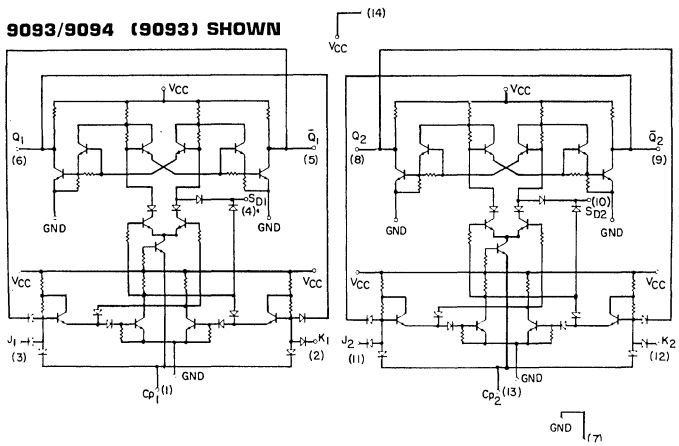
The MIC 9097 and MIC 9099 are single chip dual flip-flops with circuitry similar to the MIC 948 and MIC 945 respectively. They feature internal J-K connections, a common clock pin, a common CD pin, and separate SD pins. They are useful in shift registers, shift counters, and synchronous counters.

The MIC 9093 and MIC 9099 are usable with clock frequencies up to 5 MHZ and feature a DC level sensitive clock input for stable operation regardless of clock waveshape.

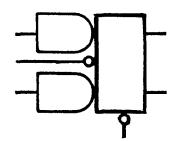
The MIC 9094 and MIC 9097 are usable with clock frequencies up to 8 MHZ.

These circuits are fully compatible with the ITT MIC 930 series DTL family and the ITT MIC 9000 series TTL family.

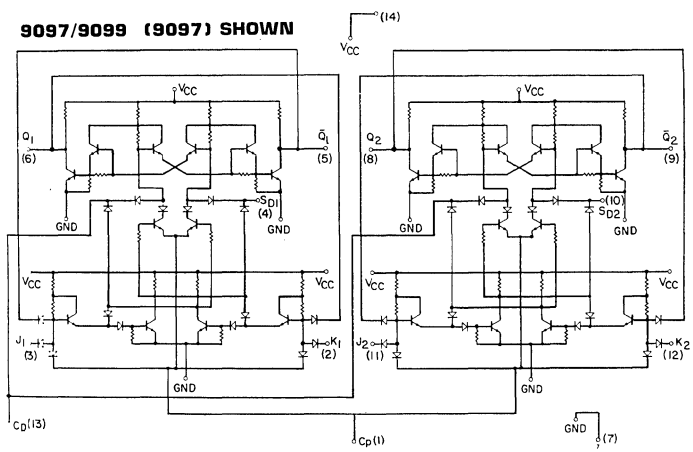
9093/9094 (9093) SHOWN



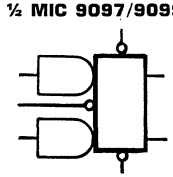
½ MIC 9093/9094



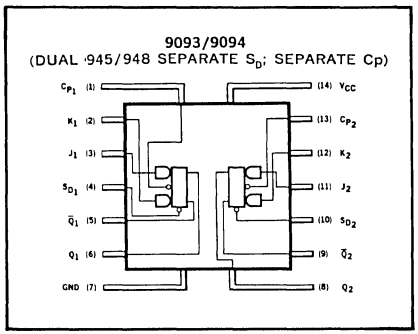
9097/9099 (9097) SHOWN

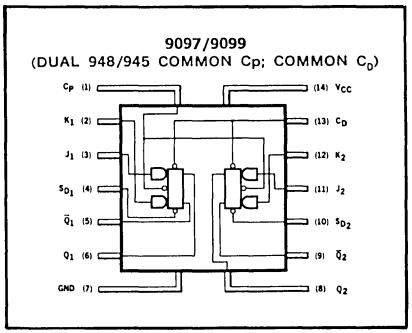


½ MIC 9097/9099



PIN CONFIGURATION (9093/9094 AND 9097/9099)





ABSOLUTE MAXIMUM RATINGS

(Above which useful life may be impaired)

Supply Voltage (V_{CC}) Continuous	−0.5 to +8.0	Volts
Supply Voltage (V_{CC}) Pulsed <1.0 second	+12.0	Volts
Power Dissipation 25°C Ambient (Note 1)	500	mw
Operating Temperature Range	−55 to +125	°C
Storage Temperature Range	−65 to +150	°C
Lead Temperature (soldering 60 second)	+300	°C
Input Voltage Applied to Input	−1.5 to +5.5	Volts

NOTE 1: Degradation by 3.3 mw per degree C for ambient temperatures above 25°C.

TRUTH TABLES

SYNCHRONOUS ENTRY

Inputs		Output
J	K	Qn+1
0	0	Qn
0	1	0
1	0	1
1	1	$\overline{Qn}$

ASYNCHRONOUS ENTRY

Inputs		Outputs	
S_D	C_D	Q	$\bar{Q}$
0	0	1	1
0	1	1	0
1	0	0	1
1	1	No Change	

NOTES:

1. Positive logic: O=L, 1=H is shown.
2. With synchronous entry, output changes occur as clock level changes from High to Low. For operation in accordance with the table, J and K inputs should normally be changed while the clock is low, and maintained while the clock is high.
3. Asynchronous entry overrides synchronous entry, regardless of clock level. If S_D and C_D are both low, then both go high simultaneously, final condition cannot be predicted. For proper operation, the S_D or C_D terminals must be held in the low state for at least 50 nanoseconds.
4. From circuit symmetry, the S_D and C_D pin designations may be interchanged by interchanging the J and K, and also the Q and $\bar{Q}$ pin designations. Thus, the 9093–9094 may be used as a dual flip-flop having C_D terminals available, and the 9097–9099 may be used as a dual flip-flop having separate C_D terminals and a common S_D terminal.
   All rules for MIC 945 apply to MIC 9093 and 9099
   All rules for MIC 948 apply to MIC 9094 and 9097
5. Refer to the MIC 945/948 section of ITT's New Unabridged DTL Design Data Book for typical operating characteristics.

SUMMARY OF MIC 9093/9094 AND 9097/9099 CHARACTERISTICS (25°C)

Network Parameter		Note	FULL TEMPERATURE RANGE Min.	Typ.	Max.	LIMITED TEMPERATURE RANGE Min.	Typ.	Max.	Unit
Operating Supply Voltage		1	4.5	5.0	5.5		5.0		Volts
Network Dissipation		9093/9099 2			70.0			75.0	mW
		9094/9097			81.0			87.5	
Loading D.C. Fanout		9093/9099			10.0			12.0	DTL Unit
		9094/9097			9.0			11.0	Load
Output Logic	'1' (High)	9093/9099	2.5			2.5			Volts
		9094/9097	2.5			4.2			
	'O' (Low)	9093/9099			0.4			0.45	
		9094/9097			0.4			0.45	
Input Threshold	'1' (High)	3	1.9			1.9			Volts
	'O' (Low)				1.1			1.1	
Propagation	$t_{pd}+$	9093/9099 4	35.0		75.0	35.0		75.0	Nano-
Delay Time		9094/9097	30.0		65.0	30.0		65.0	Second
	$t_{pd}-$	9093/9099	30.0		75.0	30.0		75.0	
		9094/9097	30.0		75.0	30.0		75.0	
Noise Immunity			0.35	>0.5		0.35	>0.5		Volts

NOTES: 1. Exact specification limits for operating temperature range may be obtained by reference to the appropriate test.
2. Power supplied from V_{CC}(5V) during "ON" state, Fanout = 0.
3. Input threshold voltage is defined as the minimum (or maximum) voltage at the circuit input to guarantee a low (or high) output.
4. Propagation delay time terms ($t_{pd}+$ and $t_{pd}-$) are described in the t_{pd} test circuit, Page 8.

9093/9094 TEST SEQUENCE

Test No.	Notes	FORCING CONDITIONS AT PINS C_P 1(13)	K 2(12)	J 3(11)	S_D 4(10)	$\overline{Q}$ 5(9)	Q 6(8)	V_{CC} 14	Sense	TEST LIMITS Min.	Max.
1	1,2	GND	GND	GND	GND			V_{MAX}	I_{14}		I_{MAX}
2	1,2				GND			V_{PD}	I_{14}		I_{PDH}
3 (4)	1	V_R		GND				V_R	$I_1(I_{13})$		I_{RCP}
5 (6)	1	V_R	GND		GND			V_R	$I_1(I_{13})$		I_{RCP}
7 (8)	1	GND		V_R		GND		V_{CCH}	$I_3(I_{11})$		I_R
9(10)	1	GND	V_R				GND	V_{CCH}	$I_2(I_{12})$		I_R
11(12)	1	C_{P2}	GND		V_R			V_{CCH}	$I_4(I_{10})$		$2I_R$
13(14)	1				GND		V_{CEX}	V_{CEX}	$I_6(I_8)$		I_{CEX}
15(16)	1	C_{P2}	V_R	GND	V_R	V_{CEX}		V_{CEX}	$I_5(I_9)$		I_{CEX}
17(18)	1	C_{P2}	V_R	GND	V_{IL}		$-I_{OH}$	V_{CCL}	$V_6(V_8)$	V_{OH}	
19(20)	1	C_{P2}	V_R	GND	V_R	$-I_{OH}$		V_{CCL}	$V_5(V_9)$	V_{OH}	
21(22)	1,3	C_{P1}	V_R	GND	V_R		I_{OL1}	V_{CCL}	$V_6(V_8)$		$V_{OL}1$
23(24)	1,3	C_{P1}	V_R	GND	V_R		I_{OL2}	V_{CCH}	$V_6(V_8)$		$V_{OL}2$
25(26)	1,3				GND	I_{OL1}		V_{CCL}	$V_5(V_9)$		$V_{OL}1$
27(28)	1,3				GND	I_{OL2}		V_{CCH}	$V_5(V_9)$		$V_{OL}2$
29(30)	1,3	C_{P4}	V_{IH}	GND	C_{P1}			V_{CCH}	$V_6(V_8)$		$V_{OL}2$
31(32)	1	V_F			V_{IL}			V_{CCH}	$-V_1(V_{13})$		$-I_{FCP1}$
33(34)	1	C_{P3}	V_R	V_F	C_{P1}			V_{CCH}	$-I_3(I_{11})$		$-2/3I_{F1}$
35(36)	1		V_F		GND			V_{CCH}	$-I_2(I_{12})$		$-2/3I_{F1}$
37(38)	1			GND	V_F			V_{CCH}	$I_4(I_{10})$		$-I_{FS1}$
39(40)	1	C_{P2}	V_R	$-V_S$	V_R	GND		V_{CCH}	$-I_5(I_9)$	$-I_{SC}$ (Min.)	$-I_{SC}$ (Max.)
41(42)	1		$-V_S$		GND		GND	V_{CCH}	$-I_6(I_8)$	$-I_{SC}$ (Min.)	$-I_{SC}$ (Max.)
43(44)		TPD+ See Test Figure and Table									
45(46)		TPD− See Test Figure and Table									
47(48)	1,4	V_F			V_{IL}			V_{CCL}	$-V_1(V_{13})$		$-I_{FCP2}$
49(50)	1,4	C_{P3}	V_R	V_F	C_{P1}			V_{CCL}	$-I_3(I_{11})$		$-2/3\ I_{F2}$
51(52)	1,4		V_F		GND			V_{CCL}	$-I_2(I_{12})$		$-2/3\ I_{F2}$
53(54)	1,4			GND	V_F			V_{CCL}	$I_4(I_{10})$		$-I_{FS2}$

NOTES: 1. Pin 7 is grounded for all tests. 2. Tests 1 and 2 only; forcing conditions applied to both flip-flops simultaneously. 3. Tests 21 through 30 only; ground Q, S_D, and C_P of opposite flip-flop. 4. Tests 47/54 apply to full temperature range only.

RELIABILITY TESTS

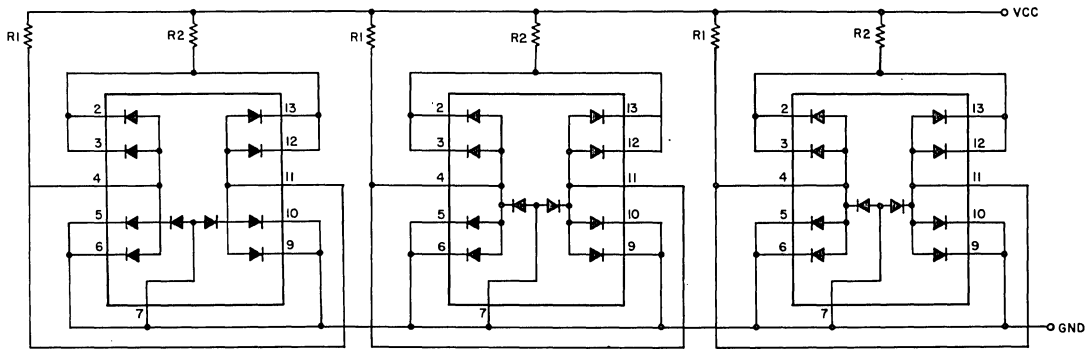
PERFORMED DURING ITT RELIABILITY PROGRAM

MEASUREMENTS OF THE FOLLOWING PARAMETERS ARE RECORDED:

Parameter	Test Sequence Number on Page 39
V_F	#1
V_F	#5
$5I_R$	#19
$5I_R$	#20

LIFE TEST CIRCUIT

FIG. 94



NOTE: V_{CC} = +5.5 Volts Ambient Temperature = +125°C
R_1 = 220Ω, 10%, ½ watt. R_2 = 390Ω, 10%, ½ watt.

CLOCKED FLIP-FLOP MIC 945
CLOCKED FLIP-FLOP MIC 948

DESCRIPTION

The MIC 945 and MIC 948 elements are clocked flip-flops.

Both the MIC 945 and MIC 948 flip-flops operate on the "master-slave" principle. Information enters the "master" flip-flop when trigger clock input voltage is high and transfers to the "slave" flip-flop when trigger clock input voltage goes low. Since operation depends only on voltage levels any sort of waveshape having the proper voltage levels may be used as a trigger signal. (The rise and fall times are irrelevant.)

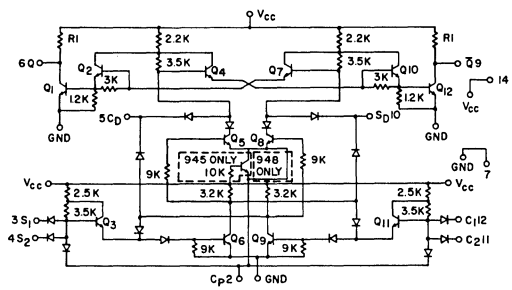
Both the MIC 945 and MIC 948 have an improved direct set and direct clear design which allows unhampered asynchronous entry irrespective of signals applied to any other inputs. The direct inputs always take precedence, thus simplifying the design of arbitrarily preset counters or control flip-flops.

Both flip-flops incorporate output buffers which provide isolation between the "slave" flip-flop and the output load, thereby enhancing immunity to signal line noise.

The MIC 945 incorporates a 6K ohm output pull up resistor which allows for a fan-out of up to 12 DTL loads.

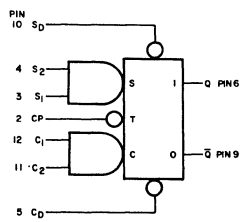
The MIC 948 incorporates a 2K ohm output pull up resistor which allows for typically 30% faster rise times for capacitive loads at a fan-out of up to 11 DTL loads.

CIRCUIT SCHEMATIC



NOTES: Pins 1, 8, 13 not used
945, R_1 = 6K
948, R_1 = 2K
PIN NUMBERS REFER TO FLAT PACKAGE AND DIP

POSITIVE LOGIC SYMBOLS



NOTES:
1. Pin numbers refer to flat package.
2. Abbreviations used in the body of tables:
NC = no change, the trigger-pulse has equal effect.
0 = low, the more negative voltage level.
1 = high, the more positive voltage level
(In all cases, unused pins have the same effect as high.)
Φ = immaterial, either 1 or 0 has no effect on outputs.

SYNCHRONOUS ENTRY

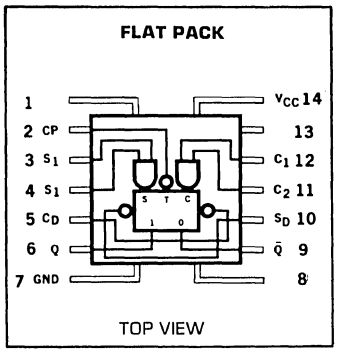
Inputs t_n				Output t_{n+1}
3	4	11	12	6
0	Φ	0	Φ	NC
0	Φ	Φ	0	NC
Φ	0	0	Φ	NC
Φ	0	Φ	0	NC
0	Φ	1	1	0
Φ	0	1	1	0
1	1	0	Φ	1
1	1	Φ	0	1
1	1	1	1	Undetermined

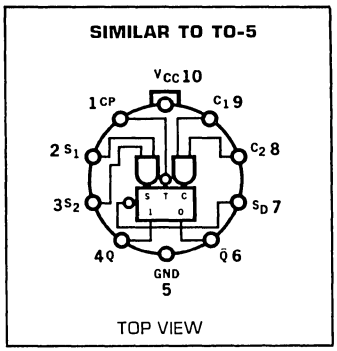
For J-K Mode Operation:
Connect 4 to 9 and 11 to 6

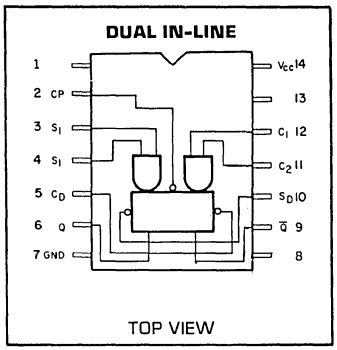
ASYNCHRONOUS ENTRY

Inputs		Outputs	
5	10	6	9
1	1	NC	NC
1	0	1	0
0	1	0	1
0	0	1	1

Asynchronous entry is independent of all other inputs and overrides synchronous entry.







ABSOLUTE MAXIMUM RATINGS[1]

		UNITS
Supply Voltage (V_{CC}), −55°C to +125°C, continuous	−0.5 to +8	Volts
Supply Voltage (V_{CC}), pulsed, <1 sec	+12	Volts
Output Current, into outputs	30	mA
Input Forward Current	−10	mA
Input Reverse Current	1	mA
Operating Temperature	−55 to +125	°C
Storage Temperature	−65 to +150	°C
Operating Junction Temperature[2]	+175	°C
Input Voltage Applied to Input	−1.5 to +5.5	V
Lead Temp. (soldering, 60 sec.)	300	°C

NOTES: 1. Above which useful life may be impaired.
2. Allow 200°C/Watt θ_{J-A} for TO-5; 300°C/Watt θ_{J-A} for ¼" x ¼" flatpack and dual in-line. Allow 50°C/Watt θ_{J-C} for TO-5; 180°C/Watt θ_{J-C} for ¼" x ¼" flatpack and dual in-line. Heat removal in ¼" x ¼" flatpack is highly dependent upon contact surfaces or air flow and on lead attachment and thermal paths thru leads, as well as number of soldered leads.

SUMMARY OF MIC 945 AND 948 CHARACTERISTICS (25°C)

			FULL TEMPERATURE RANGE			LIMITED TEMPERATURE RANGE			
Network Parameter		Note	Min.	Typ.	Max.	Min.	Typ.	Max.	Unit
Operating Supply Voltage		1	4.5	5.0	5.5		5.0		Volts
Network Dissipation	945	2			70.0			75.0	mW
	948				81.0			87.5	
Loading D.C. Fanout	945				10.0			12.0	DTL Unit
	948				9.0			11.0	Load
Output Logic '1' (High)	945		2.5			3.1			Volts
	948		2.5			4.3			
'0' (Low)	945				0.4			0.45	
	948				0.4			0.45	
Input Threshold '1' (High)		3	1.9			1.9			Volts
'0' (Low)					1.1			1.1	
Propagation t_{pd}+	945	4	35.0		75.0	35.0		75.0	Nano-
Delay Time	948		30.0		65.0	30.0		65.0	Second
t_{pd}−	945		30.0		75.0	30.0		75.0	
	948		30.0		75.0	30.0		75.0	
Noise Immunity			0.35	>0.5		0.35	>0.5		Volts

NOTES: 1. Exact specification limits for operating temperature range may be obtained by reference to the appropriate test.
2. Power supplied from V_{CC}(5V) during "ON" state, Fanout = 0.
3. Input threshold voltage is defined as the minimum (or maximum) voltage at the circuit input to guarantee a low (or high) output.
4. Propagation delay time terms (t_{pd}+ and t_{pd}−) are described in the t_{pd} test circuit, Page 46

TEST SEQUENCE

NOTE: Pin numbers refer to flat package and dual in line package.

Test No.	Notes	C_P Pin 2	S_1 3	FORCING CONDITIONS AT PINS S_2 4	C_D 5	Q 6	$\overline{Q}$ 9	S_D 10	C_2 11	C_1 12	V_{CC} 14	Sense	TEST LIMITS Min.	Max.
1	1	V_R	GND	GND	GND						V_R	I_2		I_{RCP}
2	1	V_R						GND	GND	GND	V_R	I_2		I_{RCP}
3	1	GND	V_R	GND							V_{CCH}	I_3		I_R
4	1	GND	GND	V_R							V_{CCH}	I_4		I_R
5	1	GND							GND	V_R	V_{CCH}	I_{12}		I_R
6	1	GND							V_R	GND	V_{CCH}	I_{11}		I_R
7	1	CP	GND	GND	V_R			V_{CCH}			V_{CCH}	I_5		I_R
8	1	CP			V_{CCH}			V_R	GND	GND	V_{CCH}	I_{10}		I_R
9	1				GND	V_{CEX}		GND			V_{CEX}	I_6		I_{CEX}
10	1				GND		V_{CEX}	GND			V_{CEX}	I_9		I_{CEX}
11	1	GND	GND	GND	GND			GND	GND	GND	V_{MAX}	I_{14}		I_{MAX}
12	1	CP	GND	GND	V_{CCL}	$-I_{OH}$		V_{ILS}			V_{CCL}	V_6	V_{OH}	
13	1	CP			V_{ILS}		$-I_{OH}$	V_{CCL}	GND	GND	V_{CCL}	V_9	V_{OH}	
14	1, 2	CP	V_{IL}		V_{CCL}	I_{OL1}		V_{IH}	V_{IH}	V_{IH}	V_{CCL}	V_6		V_{OL1}
15	1, 2	CP		V_{IL}	V_{CCH}	I_{OL2}		V_{IH}	V_{IH}	V_{IH}	V_{CCH}	V_6		V_{OL2}
16	1, 2	CP	V_{IH}	V_{IH}	V_{IH}		I_{OL1}	V_{CCL}	V_{IL}		V_{CCL}	V_9		V_{OL1}
17	1, 2	CP	V_{IH}	V_{IH}	V_{IH}		I_{OL2}	V_{CCH}		V_{IL}	V_{CCH}	V_9		V_{OL2}
18	1	V_R	V_F	V_R							V_{CCH}	$-I_3$		$-2/3\ I_{F1}$
19	1	V_R	V_R	V_F							V_{CCH}	$-I_4$		$-2/3\ I_{F1}$
20	1	V_R							V_R	V_F	V_{CCH}	$-I_{12}$		$-2/3\ I_{F1}$
21	1	V_R							V_F	V_R	V_{CCH}	$-I_{11}$		$-2/3\ I_{F1}$
22	1	GND			V_F			GND			V_{CCH}	$-I_5$		$-I_{FSI1}$
23	1	GND			GND			V_F			V_{CCH}	$-I_{10}$		$-I_{FSI1}$
24	1				V_F				GND	GND	V_{CCH}	$-I_5$		$-I_{FS}$
25	1		GND	GND				V_F			V_{CCH}	$-I_{10}$		$-I_{FS}$
26	1	V_F			V_{ILS}						V_{CCH}	$-I_2$		$-I_{FCP1}$
27	1	V_F						V_{ILS}			V_{CCH}	$-I_2$		$-I_{FCP1}$
28	1	CP			V_{CCH}	GND		V_{CCH}	GND	GND	V_{CCH}	$-I_6$	$-I_{SC}$	
29	1	CP			V_{CCH}	GND		V_{CCH}	GND	GND	V_{CCH}	$-I_6$		$-I_{SC}$
30	1	CP	GND	GND	V_{CCH}		GND	V_{CCH}			V_{CCH}	$-I_9$	$-I_{SC}$	
31	1	CP	GND	GND	V_{CCH}		GND	V_{CCH}			V_{CCH}	$-I_9$		$-I_{SC}$
32	1										V_{PD}	I_{14}		I_{PDH}
33	$t_{pd}+$, 945	See Page 45 for Test Limits and Conditions.												
34	$t_{pd}-$, 945	See Page 45 for Test Limits and Conditions.												
35	$t_{pd}+$, 948	See Page 45 for Test Limits and Conditions.												
36	$t_{pd}-$, 948	See Page 45 for Test Limits and Conditions.												
37	1,3	V_R	V_F	V_R							V_{CCL}	$-I_3$		$-2/3\ I_{F2}$
38	1,3	V_R	V_R	V_F							V_{CCL}	$-I_4$		$-2/3\ I_{F2}$
39	1,3	V_R							V_R	V_F	V_{CCL}	$-I_{12}$		$-2/3\ I_{F2}$
40	1,3	V_R							V_F	V_R	V_{CCL}	$-I_{11}$		$-2/3\ I_{F2}$
41	1,3	GND			V_F			GND			V_{CCL}	$-I_5$		$-I_{FSI2}$
42	1,3	GND			GND			V_F			V_{CCL}	$-I_{10}$		$-I_{FSI2}$
43	1,3	V_F			V_{ILS}						V_{CCL}	$-I_2$		$-I_{FCP2}$
44	1,3	V_F						V_{ILS}			V_{CCL}	$-I_2$		$-I_{FCP2}$

NOTES: 1. Ground pin is grounded.
2. Delay application of I_{OL} current source until after completion of clock pulse. Alternatively clamp current source compliance voltage below V_{CEX}.
3. Tests 37/44 apply to full temperature range only.

FORCING CONDITIONS

FULL -TEMPERATURE RANGE					LIMITED TEMPERATURE RANGE				
Parameter	Units	−55°C	+25°C	+125°C	Parameter	Units	0°C	+25°C	+75°C
V_{CCH}	Volts	5.5	5.5	5.5	V_{CCH}	Volts	5.0	5.0	5.0
V_{CCL}	Volts	4.5	4.5	4.5	V_{CCL}	Volts	5.0	5.0	5.0
V_{MAX}	Volts		8.0		V_{MAX}	Volts		8.0	
V_{PD}	Volts		5.0		V_{PD}	Volts		5.0	
V_R	Volts	4.0	4.0	4.0	V_R	Volts	4.0	4.0	4.0
V_F	Volts	0.4	0.4	0.4	V_F	Volts	0.45	0.45	0.5
V_{CEX}	Volts		5.5		V_{CEX}	Volts		4.5	
V_{IL}	Volts	1.4	1.1	0.8	V_{IL}	Volts	1.2	1.1	0.95
V_{ILS}	Volts	1.4	1.1	0.8	V_{ILS}	Volts	1.2	1.1	0.95
V_{IH}	Volts	2.1	1.9	1.7	V_{IH}	Volts	2.0	1.9	1.8
I_{OL1} 945	mA	12.0	12.0	12.0	I_{OL1} 945	mA	16.8	16.8	16.0
I_{OL1} 948	mA	13.0	13.0	13.0	I_{OL1} 948	mA	15.4	15.4	14.6
I_{OL2} 945	mA	15.0	15.0	15.0	I_{OL2} 945	mA	16.8	16.8	16.0
I_{OL2} 948	mA	13.6	13.6	13.6	I_{OL2} 948	mA	15.4	15.4	14.6
$-I_{OH}$ 945	μA	180.0	180.0	180.0	$-I_{OH}$	μA	120.0	120.0	120.0
$-I_{OH}$ 948	μA	540.0	540.0	540.0					

TEST LIMITS

		FULL TEMPERATURE RANGE						LIMITED TEMPERATURE RANGE					
		−55°C		+25°C		+125°C		0°C		+25°C		+75°C	
Parameter	Units	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.
V_{OL1}	Volts		0.4		0.4		0.4		0.45		0.45		0.5
V_{OL2} 945	Volts		0.4		0.4		0.4		0.45		0.45		0.45
V_{OL2} 948	Volts		0.4		0.4		0.4		0.45		0.45		0.5
V_{OH} 945	Volts	2.5		2.5		2.5		2.6		2.6		2.5	
V_{OH} 948	Volts	2.5		2.5		2.5		4.3		4.3		4.2	
I_{RCP}	μA		10.0		10.0		20.0		20.0		20.0		30.0
I_R	μA		2.0		2.0		5.0		5.0		5.0		10.0
I_{CEX}	μA				50.0						100.0		
I_{MAX} 945 Flat Pack	mA				16.0						17.0		
I_{MAX} 948 Flat Pack	mA				16.0						17.5		
I_{MAX} 945 TO-5	mA				20.0						21.0		
I_{MAX} 948 TO-5	mA				23.0						25.0		
$-2/3\ I_{F1}$	mA		.98		.98		.92		0.95		0.95		0.9
$-I_{FSI1}$	mA		2.93		2.93		2.57		2.8		2.8		2.66
$-I_{FS}$	mA		2.4		2.4		2.1		2.1		2.1		2.0
$-I_{FCP1}$ 945	mA		2.93		2.93		2.57		2.8		2.8		2.66
$-I_{FCP1}$ 948	mA		2.35		2.35		2.03		2.24		2.24		2.13
$-I_{SC}$ 945	mA	0.7	1.33	0.7	1.33	0.625	1.3	0.59	1.41	0.59	1.41	0.55	1.38
$-I_{SC}$ 948	mA	2.1	3.96	2.1	3.96	1.86	3.54	1.77	4.2	1.77	4.2	1.6	4.0
I_{PDH} 945					14.0						15.0		
I_{PDH} 948					16.2						17.5		
$-2/3\ I_{F2}$	mA		.76		.76		.72						
$-I_{FSI2}$	mA		2.26		2.26		2.20						
$-I_{FCP2}$ 945	mA		2.26		2.26		2.02						
$-I_{FCP2}$ 948	mA		1.83		1.83		1.59						

FIG. 95

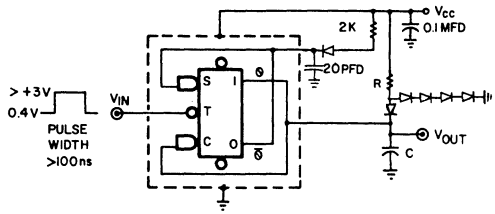
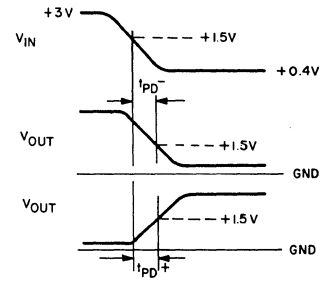


FIG. 96

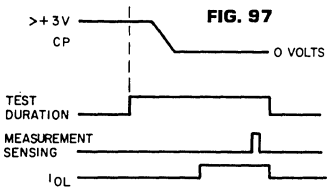


All diodes 1N916

All capacitances include wiring and probe capacitances.

PROPAGATION DELAY CONDITIONS AND LIMITS

FIG. 97



TEST CONDITIONS							LIMITS	
Test No.	Device	Test	R Ohms	C Picofarad	T °C	V_{CC} Volts	Min. Nanosecond	Max. Nanosecond
33	945	$t_{pd}+$	2.0K	30	+25	5.0	35	75
34	945	$t_{pd}-$	330	50	+25	5.0	30	75
35	948	$t_{pd}+$	2.0K	30	+25	5.0	30	65
36	948	$t_{pd}-$	330	50	+25	5.0	30	75

ELECTRICAL CHARACTERISTICS

FIG. 98
TYPICAL POWER DISSIPATION VS. Vcc

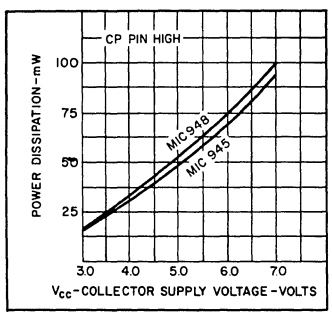


FIG. 99
TYPICAL Tpd VS. CAPACITANCE*

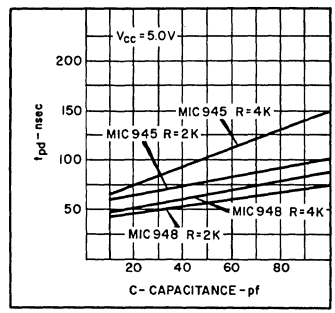


FIG. 100
TYPICAL Tpd VS. CAPACITANCE*

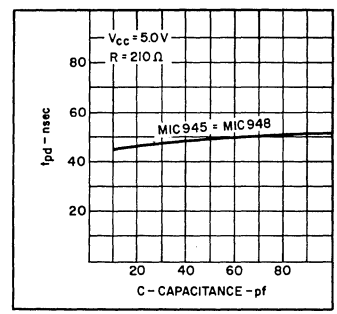


FIG. 101
TYPICAL MAXIMUM BINARY COUNTING RATE VS. CAPACITY

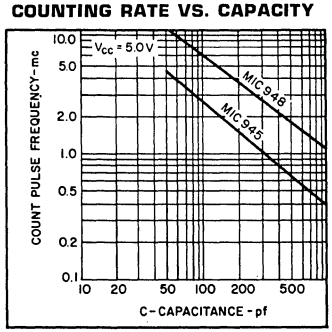
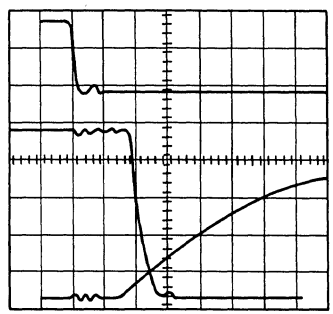


FIG. 102
948 DIVIDE BY TWO WAVEFORM



MIC 948 as a binary counter.

Upper Trace: Input, 2 volts per division.

Lower Traces: Outputs, 1 volt per division.

Falling output loaded by 50 pf and 330Ω to V_{CC}.

Rising output loaded by 50 pf.
25 nsec per division.

V_{CC} = 5V.

*SEE TEST CIRCUIT.

RELIABILITY TESTS

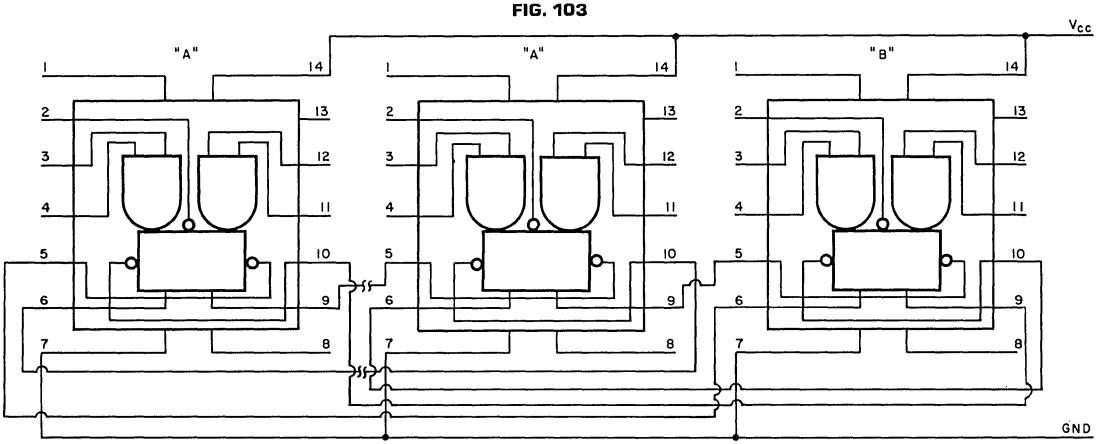
PERFORMED DURING ITT RELIABILITY PROGRAM

MEASUREMENTS OF THE FOLLOWING PARAMETERS ARE RECORDED:

Parameter	Test Sequence Number on Page 44
I_{RCP}	#1
I_R	#4 & #5
V_{OH}	#13
V_{OL}	#14
$-2/3I_F$	#18 & #20
I_{PDH}	#32

LIFE TEST CIRCUIT

FIG. 103



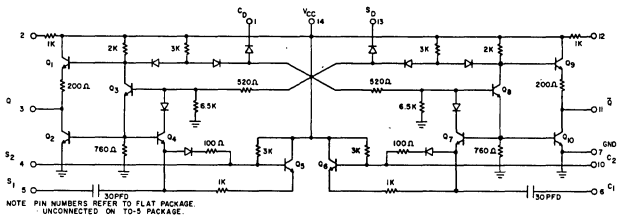
NOTE:
V_{CC}= +5.5 Volts, Ambient Temperature= +125° C
Circuit may have an odd number of units connected like "A", with one connected like "B".

PULSE-TRIGGERED BINARY FLIP-FLOP MIC 950

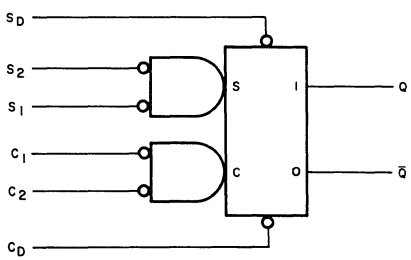
DESCRIPTION

The MIC 950 element is a pulse-triggered, high-speed gated flip-flop and can be used either as an R-S or J-K flip-flop. It will operate in a binary counter application in excess of 20 MHz over the full temperature range and it dissipates typically less than 30 milliwatts. The pulse-triggered set and clear inputs are capacitively coupled while the corresponding steering inputs are directly coupled. The direct set and clear inputs which respond to voltage levels take precedence over the pulse triggered inputs, thus simplifying the design of arbitrarily preset counters or control flip-flops.

CIRCUIT SCHEMATIC



POSITIVE LOGIC SYMBOLS

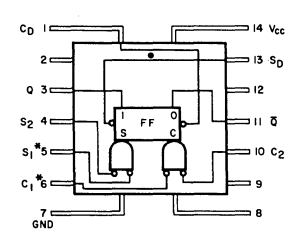


TRUTH TABLE

RESPONSE TO									
PULSE INPUTS						DIRECT INPUTS			
Inputs				Outputs		Inputs		Outputs	
4	5	6	10	3	11	1	13	3	11
S_2	S_1	C_1	C_2	Q	$\bar{Q}$	C_D	S_D	Q	$\bar{Q}$
1	Φ	1	Φ	NC	NC	1	1	NC	NC
Φ	1	Φ	1	NC	NC	0	1	0	1
0	0	Φ	1	1	0	1	0	1	0
0	0	1	Φ	1	0	0	0	1	1
1	Φ	0	0	0	1				
Φ	1	0	0	0	1				
0	0	0	0	Ambiguous					

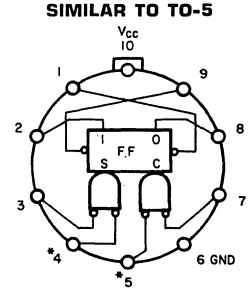
NOTES: 1. Pin numbers refer to flat package.
2. Abbreviations used in the body of tables:
0 = low, the more negative voltage level.
1 = high, the more positive voltage level (In all cases, unused pins have the same effect as high.)
Φ = immaterial, either 1 or 0 has equal effect.
NC = no change, the trigger-pulse has no effect on outputs.
3. 1 or 0 for pins 5 and 6 represent voltage transitions to the level indicated rather than the levels themselves.
4. The tables assume independent use of pulsed inputs and direct inputs. Otherwise, direct inputs will predominate.

FLAT PACK



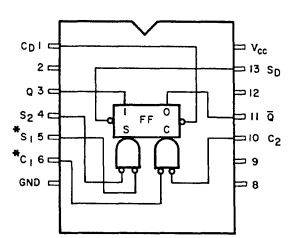
TOP VIEW
*These inputs are capacitively coupled.

SIMILAR TO TO-5



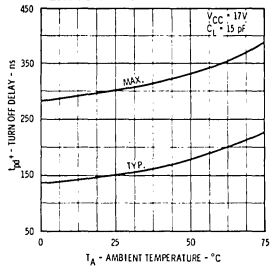
TOP VIEW
*These inputs are capacitively coupled.

DUAL IN-LINE

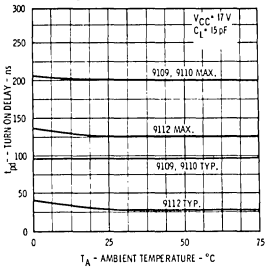


TOP VIEW
*These inputs are capacitively coupled.

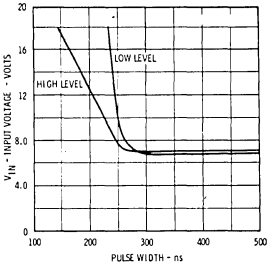
TURN OFF DELAY VERSUS AMBIENT TEMPERATURE



TURN ON DELAY VERSUS AMBIENT TEMPERATURE



TYPICAL A.C. NOISE IMMUNITY INPUT VOLTAGE VERSUS PULSE WIDTH

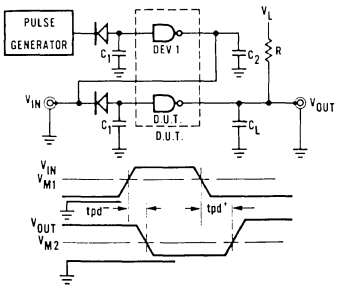


SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

$C_1 = 5.0$ pF Includes all probe
$C_2 = 10$ pF and jig capacitance
$C_L = 15$ pF

TEST CONDITIONS

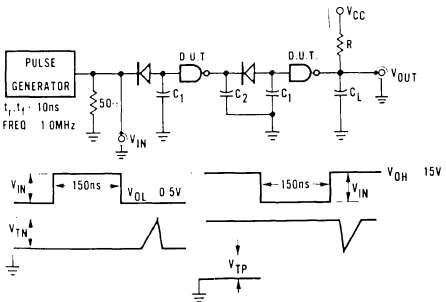
D.U.T.	DEV. 1	V_{m1}(V)	V_{m2}(V)	V_L(V)	R_{tpd-}	R_{tpd+}
9109	9110	7.5	1.5	5.0	510 Ω	3.6 k
9110	9110	7.5	7.5	17.0	2.4 k	24 k
9112	932	1.5	7.5	17.0	2.4 k	24 k



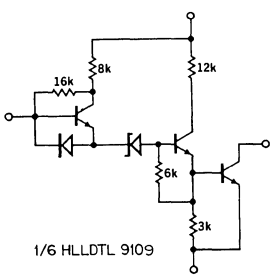
A. C. NOISE IMMUNITY TEST CIRCUIT

$C_1 = 5.0$ pF Includes jig and
$C_2 = 10$ pF all probe capacitance
$C_L = 15$ pF

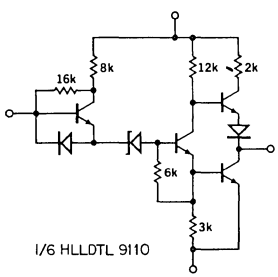
TEST CONDITIONS AND LIMITS						
TEST	LIMIT		V_{CC}	R	T_A	V_{IN}
	MIN.	MAX.	(Volts)	(kΩ)	(°C)	(Volts)
V_{TP}	8.5 V		17	24	25	10
V_{TN}		7.0 V	17	2.4	25	10



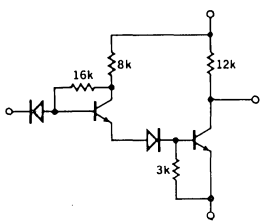
CIRCUIT SCHEMATICS



1/6 HLLDTL 9109



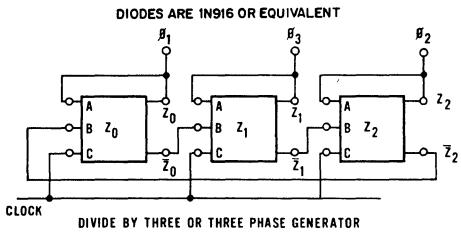
1/6 HLLDTL 9110



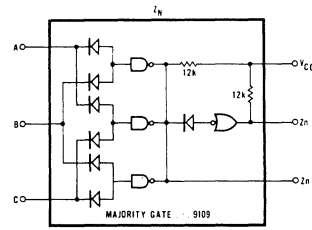
1/6 HLLDTL 9112

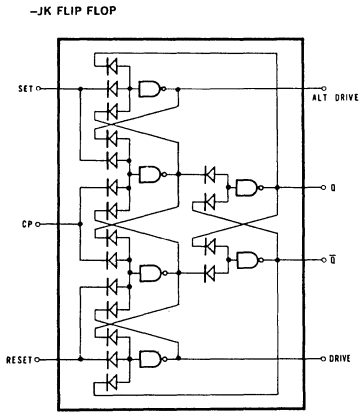
HIGH LEVEL LOGIC

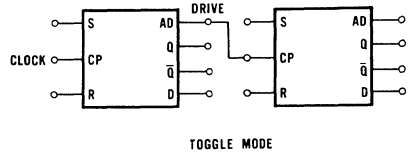
APPLICATIONS SEQUENTIAL COUNTER



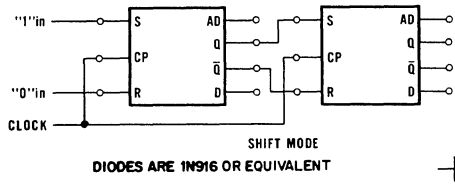
ϕ_1	ϕ_3	ϕ_2	Clock
1	0	0	0
1	0	1	1
0	0	1	0
0	1	1	1
0	1	0	0
1	1	0	1

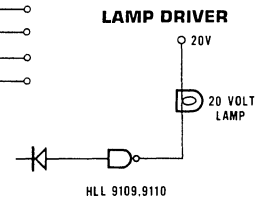


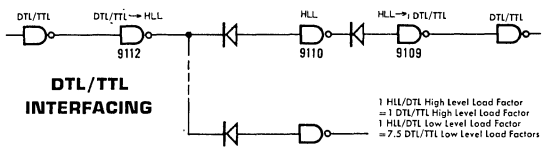


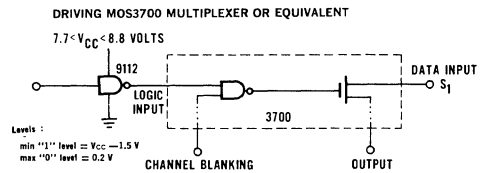


J	K	Qn+1
L	H	L
L	L	Qn
H	H	$\bar{Q}n$
H	L	H









FORCING CONDITIONS

Parameter	Units	FULL TEMPERATURE RANGE			LIMITED TEMPERATURE RANGE		
		−55°C	+25°C	+125°C	0°C	+25°C	+75°C
V_{MAX}	Volts		20.0			25.0	
V_{CCH}	Volts	16.5	16.5	16.5	20.0	20.0	20.0
V_{CCL}	Volts	13.5	13.5	13.5	12.0	12.0	12.0
V_{CEX}	Volts	16.5	16.5	16.5	20.0	20.0	20.0
V_F	Volts	0.0	0.0	0.0	0.0	0.0	0.0
V_{IL} (9109, 9110)	Volts	7.9	7.6	7.15	7.65	7.6	7.4
V_{IH} (9109, 9110)	Volts	9.3	9.1	8.8	9.2	9.1	9.0
I_{OLI}	mA	10.0	10.0	10.0	10.0	10.0	10.0
I_{OLZ}	mA	12.0	12.0	12.0	20.0	20.0	20.0
I_{OH}	μA	−100	−100	−100	−100	−100	−100
V_R	Volts	4.0	4.0	4.0	4.0	4.0	4.0
V_{IL} (9112)	Volts	1.3	1.0	0.5	1.05	1.0	0.8
V_{IH} (9112)	Volts	2.1	2.0	1.4	2.1	2.0	1.9
V_{OH} (9109)	Volts	16.5	16.5	16.5	18.0	18.0	18.0

TEST SEQUENCE* 9109

Test No.	Notes	FORCING CONDITIONS AT PINS							Sense	TEST LIMITS	
		Pin A (L)	Pin B (K)	Pin C (J)	Pin D (I)	Pin E (H)	Pin F (G)	V_{CC}		Min.	Max.
1								V_{CCH}	I_{VCC}		I_{PDH}
2	1	GND	V_{MAX}	GND	V_{MAX}	GND	V_{MAX}	V_{MAX}	I_{VCC}		I_{MAX}
3, (4)		V_{IL}	V_{OH}	GND		GND		V_{CCH}	$I_B(I_K)$		I_{OH}
5, (6)		GND		V_{IL}	V_{OH}	GND		V_{CCH}	$I_D(I_I)$		I_{OH}
7, (8)		GND		GND		V_{IL}	V_{OH}	V_{CCH}	$I_F(I_G)$		I_{OH}
9, (10)		V_F		GND		GND		V_{CCH}	$I_A(I_L)$		$-I_F$
11, (12)		GND		V_F		GND		V_{CCH}	$I_C(I_J)$		$-I_F$
13, (14)		GND		GND		V_F		V_{CCH}	$(I_E)(I_H)$		$-I_F$
15, (16)		V_{IH}	I_{OL1}	GND		GND		V_{CCL}	$V_B(V_K)$		V_{OL1}
17, (18)		GND		V_{IH}	I_{OL1}	GND		V_{CCL}	$V_D(V_I)$		V_{OL1}
19, (20)		GND		GND		V_{IH}	I_{OL1}	V_{CCL}	$V_F(V_G)$		V_{OL1}
21, (22)		V_{IH}	I_{OL2}	GND		GND		V_{CCH}	$V_B(V_K)$		V_{OL2}
23, (24)		GND		V_{IH}	I_{OL2}	GND		V_{CCH}	$V_D(V_I)$		V_{OL2}
25, (26)		GND		GND		V_{IH}	I_{OL2}	V_{CCH}	$V_F(V_G)$		V_{OL2}

*Ground Pin is grounded for all tests. Inputs of all unused gates are grounded.
Note 1. Test all gates simultaneously.

TEST SEQUENCE* 9110

Test No.	Notes	FORCING CONDITIONS AT PINS							Sense	TEST LIMITS	
		Pin A (L)	Pin B (K)	Pin C (J)	Pin D (I)	Pin E (H)	Pin F (G)	V_{CC}		Min.	Max.
1								V_{CCH}	I_{VCC}		I_{PDH}
2	1	GND	V_{MAX}	GND	V_{MAX}	GND	V_{MAX}	V_{MAX}	I_{GND}		I_{MAX}
3, (4)		V_{IL}	I_{OH}	GND		GND		V_{CCL}	$V_B(V_K)$	V_{OH}	
5, (6)		GND		V_{IL}	I_{OH}	GND		V_{CCL}	$V_D(V_F)$	V_{OH}	
7, (8)		GND		GND		V_{IL}	I_{OH}	V_{CCL}	$V_F(V_G)$	V_{OH}	
9, (10)		V_F		GND		GND		V_{CCH}	$I_A(I_L)$		$-I_F$
11, (12)		GND		V_F		GND		V_{CCH}	$I_C(I_J)$		$-I_F$
13, (14)		GND		GND		V_F		V_{CCH}	$I_E(I_H)$		$-I_F$
15, (16)		GND	V_{CEX}	GND		GND		V_{CEX}	$I_B(I_K)$		I_{CEX}
17, (18)		GND		GND	V_{CEX}	GND		V_{CEX}	$I_D(I_I)$		I_{CEX}
19, (20)		GND		GND		GND	V_{CEX}	V_{CEX}	$I_F(I_C)$		I_{CEX}
21, (22)		V_{IH}	I_{OL1}	GND		GND		V_{CCL}	$V_B(V_K)$		V_{OL1}
23, (24)		GND		V_{IH}	I_{OL1}	GND		V_{CCL}	$V_D(V_I)$		V_{OL1}
25, (26)		GND		GND		V_{IH}	I_{OL1}	V_{CCL}	$V_F(V_G)$		V_{OL1}
27, (28)		V_{IH}	I_{OL2}	GND		GND		V_{CCH}	$V_B(V_K)$		V_{OL2}
29, (30)		GND		V_{IH}	I_{OL2}	GND		V_{CCH}	$V_D(V_J)$		V_{OL2}
31, (32)		GND		GND		V_{IH}	I_{OL2}	V_{CCH}	$V_F(V_G)$		V_{OL2}
33, (34)		GND	GND	GND		GND		V_{CCH}	$I_B(I_K)$	I_{SC}	I_{SC}
35, (36)		GND		GND	GND	GND		V_{CCH}	$I_D(I_I)$	I_{SC}	I_{SC}
37, (38)		GND		GND		GND	GND	V_{CCH}	$I_F(I_G)$	I_{SC}	I_{SC}

HIGH LEVEL LOGIC

TEST SEQUENCE* 9112

Test No.	Notes	FORCING CONDITIONS AT PINS							Sense	TEST LIMITS	
		Pin A (L)	Pin B (K)	Pin C (J)	Pin D (I)	Pin E (H)	Pin F (G)	V_{CC}		Min.	Max.
1								V_{CCL}	I_{VCC}		I_{PDH}
2	1	GND	V_{MAX}	GND	V_{MAX}	GND	V_{MAX}	V_{MAX}	I_{CND}		I_{MAX}
3, (4)		V_R		GND		GND		V_{CCH}	$I_A(I_L)$		I_R
5, (6)		GND		V_R		GND		V_{CCH}	$I_C(I_J)$		I_R
7, (8)		GND		GND		V_R		V_{CCH}	$I_E(I_H)$		I_R
9, (10)		GND	V_{CEX}	GND		GND		V_{CCH}	$I_B(I_K)$		I_{CEX}
11, (12)		GND		GND	V_{CEX}	GND		V_{CCH}	$I_O(I_I)$		I_{CEX}
13, (14)		GND		GND		GND	V_{CEX}	V_{CCH}	$I_F(I_G)$		I_{CEX}
15, (16)		V_F		GND		GND		V_{CCH}	$I_A(I_L)$		$-I_F$
17, (18)		GND		V_F		GND		V_{CCH}	$I_C(I_J)$		$-I_F$
19, (20)		GND		GND		V_F		V_{CCH}	$I_E(I_H)$		$-I_F$
21, (22)		V_{IH}	I_{OL1}	GND		GND		V_{CCL}	$V_B(V_K)$		V_{OL1}
23, (24)		GND		V_{IH}	I_{OL1}	GND		V_{CCL}	$V_N(V_I)$		V_{OL1}
25, (26)		GND		GND		V_{IH}	I_{OL1}	V_{CCL}	$V_F(V_G)$		V_{OL1}
27, (28)		V_{IH}	I_{OL2}	GND		GND		V_{CCH}	$V_B(V_K)$		V_{OL2}
29, (30)		GND		V_{IH}	I_{OL2}	GND		V_{CCH}	$V_D(V_I)$		V_{OL2}
31, (32)		GND		GND		V_{IH}	I_{OL2}	V_{CCH}	$V_F(V_G)$		V_{OL2}
33, (34)		V_{IL}	I_{OH}	GND		GND		V_{CCH}	$V_B(V_K)$	V_{OH}	
35, (36)		GND		V_{IL}	I_{OH}	GND		V_{CCH}	$V_O(V_I)$	V_{OH}	
37, (38)		GND		GND		V_{IL}	I_{OH}	V_{CCH}	$V_F(V_G)$	V_{OH}	
39, (40)		GND	GND	GND		GND		V_{CCH}	$I_B(I_K)$	$-I_{SC}$	$-I_{SC}$
41, (42)		GND		GND	GND	GND		V_{CCH}	$I_O(I_I)$	$-I_{SC}$	$-I_{SC}$
43, (44)		GND		GND		GND	GND	V_{CCH}	$I_F(I_G)$	$-I_{SC}$	$-I_{SC}$

TEST LIMITS

Parameter	Units	FULL TEMPERATURE RANGE						LIMITED TEMPERATURE RANGE					
		−55°C		+25°C		+125°C		0°C		+25°C		+75°C	
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.
I_{POH} (9109, 9110)	mA										28.0		
I_{POH} (9112)	mA										34.0		
I_{MAX}	mA				10						15.0		
I_{ON} (9109)	μA		75.0		75.0		75.0		75.0		75.0		75.0
$-I_F$ (9109, 9110)	mA		0.860		0.860		0.810		1.31		1.31		1.25
$-I_F$ (9112)	mA		0.825		0.825		0.800		1.15		1.15		1.10
V_{OL1}	Volts		0.5		0.5		0.5		0.5		0.5		0.5
V_{OL2}	Volts		1.0		1.0		1.0		1.0		1.0		1.0
V_{OH} (9110, 9112)	Volts	14.5		14.5		14.5		18.0		18.0		18.0	
I_R	μA		2.0		2.0		5.0		5.0		5.0		10.0
I_{CEX}	μA		50.0		50.0		50.0		75.0		75.0		75.0
I_{SC} (9110)	mA		−12.0	5.2	11.0		−11.0		−17.0	5.0	16.3		15.6
I_{SC} (9112)	mA		−1.90	1.1	1.83		−1.83		−2.4	−1.25	−2.3		−2.3

MOS COUNTER DECODER DRIVER

- **Direct drive for low voltage seven segment display tubes***
- **Counts up or down**
- **Sample and hold capability**
- **Operation to 1 MHz**
- **Dot storage and drive**
- **Packaged in a 24 pin metalized ceramic DIP**

General — The ITT 1056 MOS circuit performs the functions of up/down decade counting, binary storage, binary to decimal decoding, decimal to seven segment decoding and direct drive for low voltage seven segment display tubes.* The 1056 and the display tube share the same −27v supply.

Up/Down Count Control — The ITT 1056 counts up when a logic "0" (negative logic convention is employed here making logic zero the high voltage level) is applied to the count up/down command input (pin 24). Conversely, a logic "1" on pin 24 causes the ITT1056 to count down.

Preset Count Control — The counter is preset to any predetermined number by applying the BCD equivalent of the number on the preset inputs (pins 5, 6, 7 and 8) and a logic "1" on the preset command input (pin 4).

Count Disable Control — Accumulation of input clock pulses by the decade counter is interrupted by a logic "1" on the count disable pin 2.

Clock Input — The decade counter advances by one count for each low to high voltage transition (logic "1" to logic "0") of the clock input (pin 3) when the count disable control is in the logic "0" state.

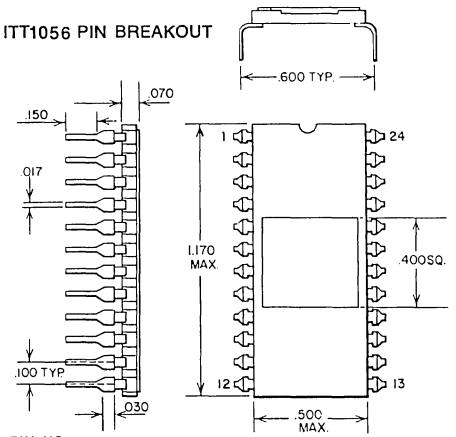
Storage Entry Command — A logic "1" on the storage entry command pin 13 causes the BCD numbers in the decade counter to enter an intermediate storage. A logic "0" on pin 13 prevents data entering this buffer. Only BCD data currently in the buffer is converted to the seven segment display drive. Data displayed by the 1056 then corresponds to the count present in the decade counter when the storage entry pin logic level was last changed from a "1" to "0". The blanking and dot inputs are also stored in this buffer.

Blanking Input — All output drivers are turned off by a logic "1" on the blanking input pin 10 and when a logic "1" is placed on the storage entry input. This control is provided for blanking out any digit not required for display. Blanking of leading zeros is one application utilizing this input.

*Tung-Sol DT1705D and G.E. Y1938

DIMENSIONS

ITT1056 PIN BREAKOUT



PIN NO.

1 — Ground	13 — Storage Entry Command
2 — Count Disable Command	14 — Dot Output
3 — Clock Input	15 — Bar E Output
4 — Preset Command	16 — Bar F Output
5 — P1 Input (2^0)	17 — Bar C Output
6 — P2 Input (2^1)	18 — Bar D Output
7 — P3 Input (2^2)	19 — Bar G Output
8 — P4 Input (2^3)	20 — Bar B Output
9 — Count Zero Output	21 — Bar A Output
10 — Blanking Input	22 — V_{GG}
11 — Carry Propagate Output	23 — V_{DD}
12 — Dot Input	24 — Count Up/Down Command

Dot Input Control — The dot output driver at pin 14 is controlled by the input on the dot input pin 12. A logic "1" on pin 12 and a logic "1" on the storage input pin 13 switches on the dot driver and stores it until pin 13 is again brought to a "1" level.

Forbidden Count Display — The 1056 BCD to seven segment decode circuitry detects forbidden BCD counts (10 to 15) which could inadvertently appear in the decade counter and excites the corresponding outputs to display the character "F" on the display tube.

Carry Propagate Output — The carry propagate output on pin 11 provides the necessary signal to cascade the 1056 for high frequency synchronous counting. A logic "0" appears at the carry propagate output on the nine count when counting up and on the zero count when counting down. For synchronous counting, the carry propagate signal from the nth digit must be fed to the count disable control pin 2 of the (n+1)st digit as illustrated in Figure 1. With this arrangement, the logic "0" carry propagate signal from the nth digit permits the (n+1)st digit

to advance or decrease only once for every ten clock pulses input to the nth digit. Connected as shown in Figure 2, the 1107C will count asynchronously up or down.

Count Zero Output — The count zero output on pin 9 also provides a signal to cascade 1107C units. A logic "0" appears at the count zero output when there is a decimal zero in the counter counting up or down. This output connected as shown in Figure 3 will give asynchronous up counting only.

ABSOLUTE MAXIMUM RATINGS

CHARACTERISTICS		UNITS
Maximum Positive Voltage Any Pin	+0.3	Volts
Maximum Negative Voltage Any Pin	−30.0	Volts
Storage Temperature	−55 to 150	°C
Ambient Operating Temperature	−55 to 85	°C

ELECTRICAL CHARACTERISTICS — Standard Conditions (unless otherwise specified)

Load = 1.0 MΩ and 25 pF, V_{GG} = −27 V ± 1 V, V_{DD} = −13 V ± 1 V, T_A = −55°C to +85°C, V_{SS} = Ground

PARAMETER		MINIMUM	TYPICAL	MAXIMUM	UNITS	CONDITIONS
INPUTS (Any)	Logic "0"	—	—	−2.0	Volts	
	Logic "1"	−10	—	—	Volts	
	Capacitance	—	2.0	5.0	pF	
	Leakage	—	—	5.0	uA	V_{in} = −25 Volts
Pulse Duration at Logic "0" or Logic "1" Clock (t_{pwl})		0.5	—	Continuous	uS	See Figure 5
Other Inputs		1.0	—	Continuous	uS	See Figure 5
Clock Rise (t_r) and Fall Times (t_f)		—	—	20	uS	See Figure 5
Clock Frequency		dc	—	1.0	MHz	
LOGIC OUTPUTS	Impedance	—	2.0	3.5	KΩ	I_{out} less than 0.3 mA
	Logic "0"	—	−0.5	−1.0	Volt	I_{out} less than 0.3 mA
	Logic "1"	−11	−12	V_{DD}	Volts	I_{out} less than 0.3 mA
Propagation Delay Plus Rise (t_{so}) or Fall Time (t_{sf})		—	0.7	1.0	uS	
Display Drive Outputs Output On		—	−1.3	−2.0	Volts	1.0 mA to a negative supply
Output Off		—	0.01	5.0	uA	−26 Volts on Output Terminal
Propagation Delay Plus Rise or Fall Time to (TD)		—	2.5	4.0	uS	
Supply Current Drain						
I_{GG}		—	4.0	7.5	mA	T_A = 25°C
I_{DD}		—	4.0	7.5	mA	T_A = 25°C, Excluding external load current

FIGURE 1 — SYNCHRONOUS COUNTING

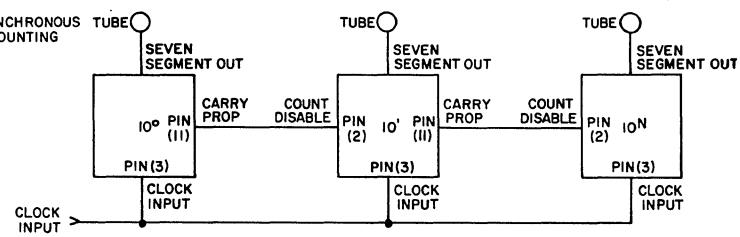


FIGURE 2 —— ASYCHRONOUS COUNTING

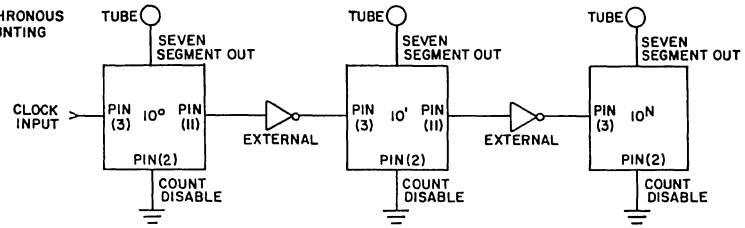


FIGURE 3 —— ASYCHRONOUS COUNTING (UP ONLY)

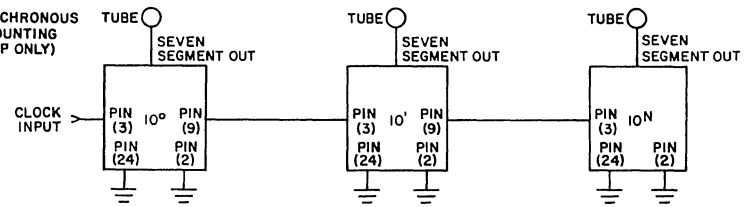


FIGURE 4 —— BLOCK DIAGRAM OF ITT1056

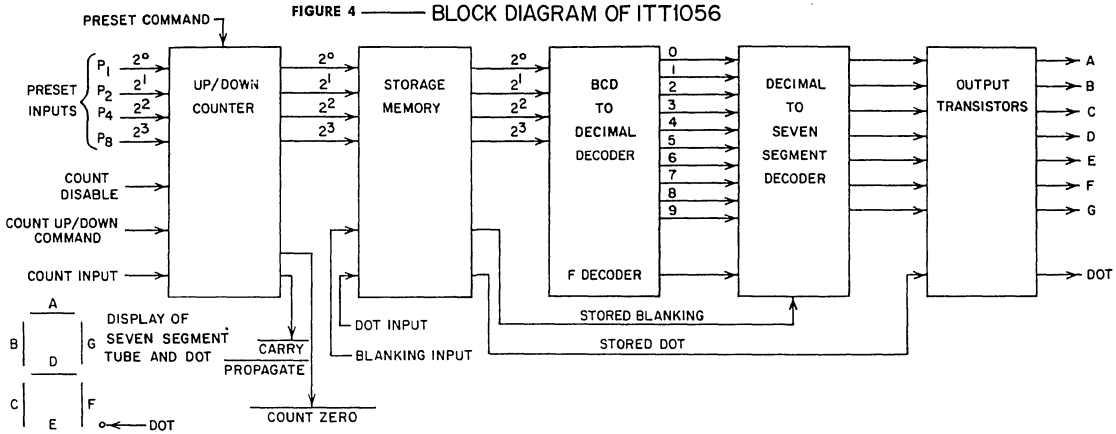
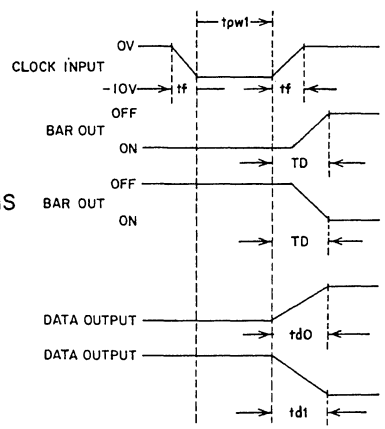


FIGURE 5 —— BAR AND DATA WAVEFORMS



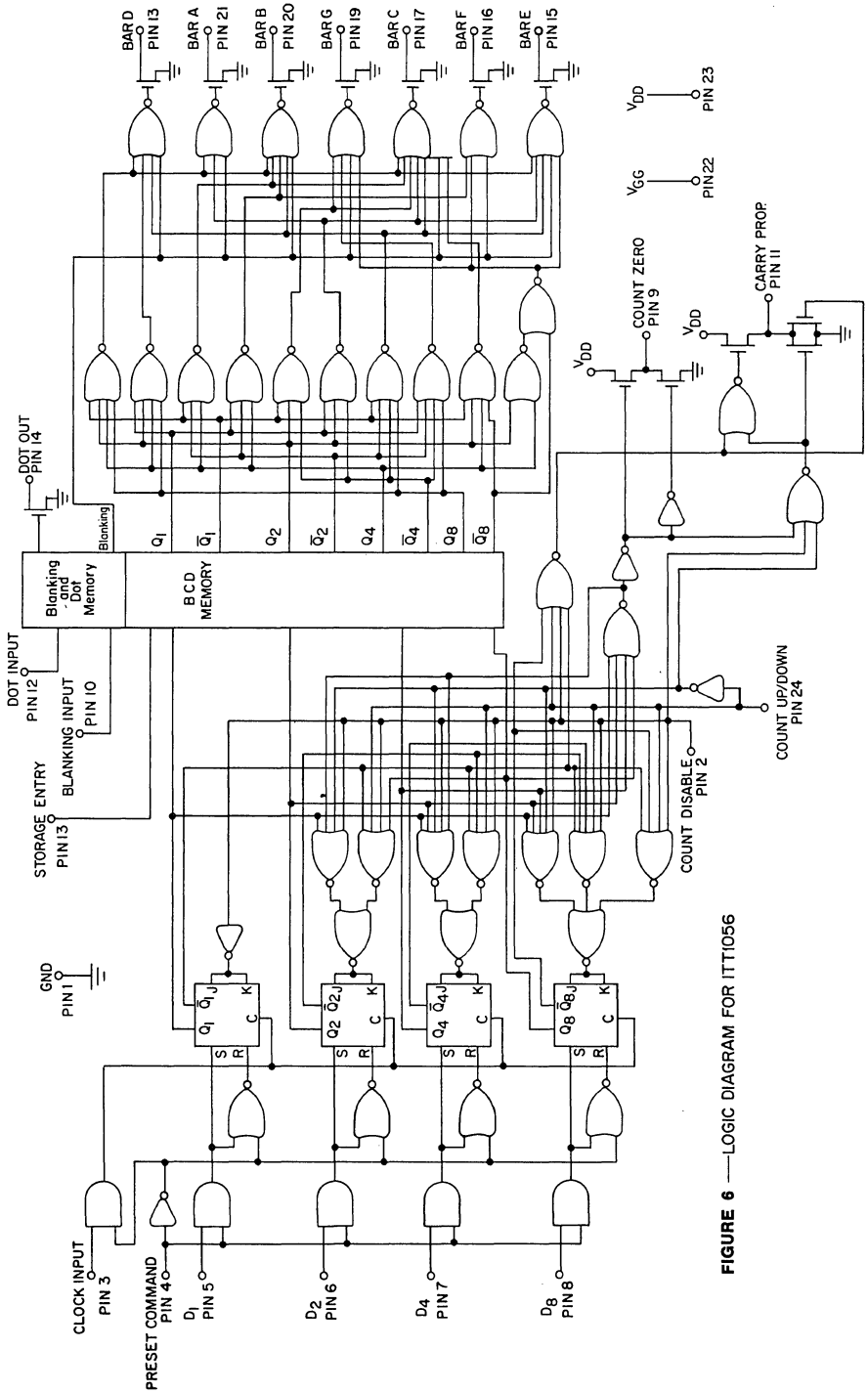


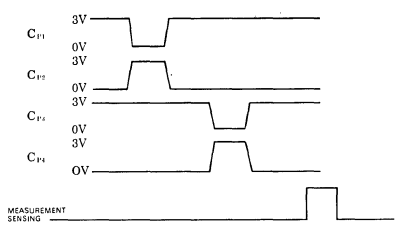
FIGURE 6 —LOGIC DIAGRAM FOR ITT1056

9097/9099 TEST SEQUENCE

Test No.	Notes	FORCING CONDITIONS AT PINS								Sense	TEST LIMITS	
		C_P 1	K 2(12)	J 3(11)	S_D 4(10)	$\overline{Q}$ 5(9)	Q 6(8)	C_D 13	V_{CC} 14		Min.	Max.
1	1,2	GND	GND	GND	GND			GND	V_{MAX}	I_{14}		I_{MAX}
2	1,2							GND.	V_{PD}	I_{14}		I_{PDH}
3(4)	1	V_R		GND				GND	V_R	I_1		$2I_{RCP}$
5(6)	1	V_R	GND		GND				V_R	I_1		$2I_{RCP}$
7(8)	1	GND		V_R		GND			V_{CCH}	$I_3(I_{11})$		I_R
9(10)	1	GND	V_R				GND		V_{CCH}	$I_2(I_{12})$		I_R
11(12)	1	C_{P2}	GND		V_R				V_{CCH}	$I_4(I_{10})$		I_R
13	1,2	C_{P2}		GND				V_R	V_{CCH}	I_{13}		$2I_R$
14(15)	1				GND		V_{CEX}	GND	V_{CEX}	$I_6(I_8)$		I_{CEX}
16(17)	1				GND	V_{CEX}		GND	V_{CEX}	$I_5(I_9)$		I_{CEX}
18(19)	1	C_{P2}	V_R	GND	V_{IL}		$-I_{OH}$	V_R	V_{CCL}	$V_6(V_8)$	V_{OH}	
20(21)	1	C_{P2}	GND	V_R	V_R	$-I_{OH}$		V_{IL}	V_{CCL}	$V_5(V_9)$	V_{OH}	
22(23)	1	GND			V_R		I_{OL}	GND	V_{CCL}	$V_6(V_8)$		$V_{OL}1$
24(25)	1	GND			V_R		I_{OL}	GND	V_{CCH}	$V_6(V_8)$		$V_{OL}2$
26(27)	1	GND			GND	I_{OL}		V_R	V_{CCL}	$V_5(V_9)$		$V_{OL}1$
28(29)	1	GND			GND	I_{OL}		V_R	V_{CCH}	$V_5(V_9)$		$V_{OL}2$
30(31)	1	C_{P4}	V_{IH}	GND	C_{P1}			V_R	V_{CCH}	$V_6(V_8)$		$V_{OL}2$
32(33)	1	C_{P4}	GND	V_{IH}	V_R			C_{P1}	V_{CCH}	$V_5(V_9)$		$V_{OL}2$
34(35)	1			V_F				GRD	V_{CCH}	$-I_3(I_{11})$		$-2/3I_{F1}$
36(37)	1		V_F		GND				V_{CCH}	$-I_2(I_{12})$		$-2/3I_{F1}$
38(39)	1	GND			V_F			GND	V_{CCH}	$-I_4(I_{10})$		$-I_{FSI1}$
40	1,2	GND			GND			V_F	V_{CCH}	$-I_{13}$		$-2I_{FSI1}$
41(42)	1			GND	V_F				V_{CCH}	$-I_4(I_{10})$		$-I_{FS1}$
43	1,2		GND					V_F	V_{CCH}	$-I_{13}$		$-2I_{FS1}$
44	1,2	V_F			V_{IL}				V_{CCH}	$-I_1$		$-2I_{FCP1}$
45	1	V_F						V_{IL}	V_{CCH}	$-I_1$		$-2I_{FCP1}$
46(47)	1		$-V_S$		GND		GND	GND	V_{CCH}	$-I_6(I_8)$	$-I_{SC}$ (min.)	$-I_{SC}$ (max.)
48(49)	1			$-V_S$	GND	GND		GND	V_{CCH}	$-I_5(I_9)$	$-I_{SC}$ (min.)	$-I_{SC}$ (max.)
50(51)	TPD+			See Test Figure and Table								
52(53)	TPD−			See Test Figure and Table								
54(55)	1,3			V_F				GRD	V_{CCL}	$-I_3(I_{11})$		$-2/3I_{F2}$
56(57)	1,3		V_F		GND				V_{CCL}	$-I_2(I_{12})$		$-2/3I_{F2}$
58(59)	1,3	GND			V_F			GND	V_{CCL}	$-I_4(I_{10})$		$-I_{FSI2}$
60	1,2,3	GND			GND			V_F	V_{CCL}	$-I_{13}$		$-2I_{FSI2}$
61(62)	1,3			GND	V_F				V_{CCL}	$-I_4(I_{10})$		$-I_{FS2}$
63	1,2,3		GND					V_F	V_{CCL}	$-I_{13}$		$-2I_{FS2}$
64	1,2,3	V_F			V_{IL}				V_{CCL}	$-I_1$		$-2I_{FCP2}$
65	1,2,3	V_F						V_{IL}	V_{CCL}	$-I_1$		$-2I_{FCP}$

NOTES: 1. Pin 7 is grounded for all tests. 2. Tests 1, 2, 13, 40, 43, 44, 60, 63, 64 and 65 only; forcing conditions applied to both flip-flops simultaneously. 3. Tests 54/65 apply to full temperature range only.

PROPAGATION DELAY CONDITIONS AND LIMITS



(T_A= +25°C)

TEST CONDITIONS				LIMITS	
		R ohms	C PF	Min. nsec.	Max. nsec.
TPD+	9093,9099	2K	30	35.	75
TPD−	9093,9099	330	50	30	75
TPD+	9094,9097	2K	30	30	65
TPD−	9094,9097	330	50	30	75

TEST LIMITS

Parameter	Units	FULL TEMPERATURE RANGE						LIMITED TEMPERATURE RANGE					
		−55°C		+25°C		+125°C		0°C		+25°C		+75°C	
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.
V_{OH} 9093/9099	Volts	2.5		2.5		2.5		2.6		2.6		3.1	
V_{OH} 9094/9097	Volts	2.5		2.5		2.5		4.3		4.3		4.3	
V_{OL}	Volts		0.4		0.4		0.4		0.45		0.45		0.45
$V_{OL}2$ 9093/9099	Volts		0.4		0.4		0.4		0.45		0.45		0.45
$V_{OL}2$ 9094/9097	Volts		0.4		0.4		0.4		0.45		0.45		0.45
I_{MAX} 9093	mA				40						42		
I_{MAX} 9094	mA				43						48		
I_{MAX} 9097	mA				32						35		
I_{MAX} 9099	mA				36						38		
I_{PDH} 9093/9099	mA				28						30		
I_{PDH} 9094/9097	mA				32.4						35		
$-I_{SC}$ 9093/9099	mA	0.7	1.33	0.7	1.33	.625	1.30	.59	1.41	.59	1.41	.55	1.38
$-I_{SC}$ 9094/9097	mA	2.1	3.96	2.1	3.96	1.86	3.54	1.77	4.2	1.77	4.2	1.6	4.0
$-2/3\ I_F$	mA		.98		.98		.92		.95		.95		.90
I_{FSI}	mA		2.93		2.93		2.57		2.8		2.8		2.66
$2I_{FSI}$	mA		5.86		5.86		5.86		5.6		5.6		5.32
I_{FS}	mA		2.2		2.2		1.93		2.1		2.1		2.0
$2I_{FS}$	mA		4.4		4.4		3.86		4.2		4.2		4.0
I_{FCP} 9093	mA		2.93		2.93		2.57		2.8		2.8		2.66
I_{FCP} 9094	mA		2.35		2.35		2.03		2.24		2.24		2.13
$2I_{FCP}$ 9097	mA		4.68		4.68		4.04		4.48		4.48		4.26
$2I_{FCP}$ 9099	mA		5.86		5.86		5.14		5.6		5.6		5.32
I_{CEX}	uA				52						105		
I_{RCP}	uA		10		10		20		20		20		30
$2I_{RCP}$	uA		20		20		40		40		40		60
I_R	uA		2		2		5		5		5		10
$2I_R$	uA		4		4		10		10		10		20
$-2/3\ I_{F2}$	mA		.76		.76		.72						
I_{FSI2}	mA		2.26		2.26		2.20						
$2\ I_{FSI2}$	mA		4.52		4.52		4.40						
I_{FS2}	mA		1.7		1.7		1.5						
$2\ I_{FS2}$	mA		3.4		3.4		3.0						
I_{FCP2} (9093)	mA		2.26		2.26		2.02						
I_{FCP2} (9094)	mA		1.83		1.83		1.59						
$2\ I_{FCP2}$ (9097)	mA		3.66		3.66		3.18						
$2\ I_{FCP2}$ (9099)	mA		4.52		4.52		4.04						

RELIABILITY TESTS

PERFORMED DURING ITT RELIABILITY PROGRAM

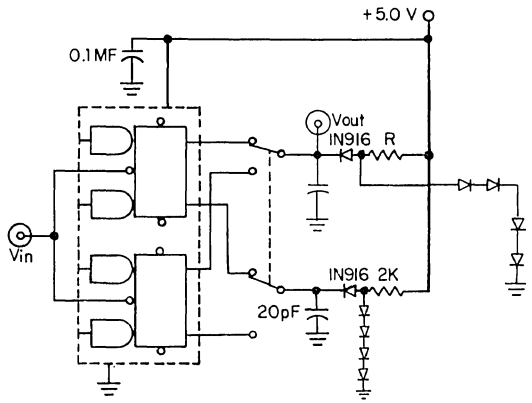
MEASUREMENTS OF THE FOLLOWING PARAMETERS ARE RECORDED:

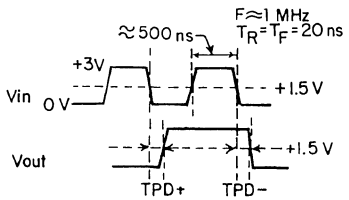
Parameter	Test Sequence Number on Pages 56, 57	
	9093/9094	9097/9099
$2I_{RCP}$	#3	#3(4)
I_{RCP}	#3(4)	
I_R	#7(8)	#7(8)
V_{OH}	#17	#18
V_{OL}	#21	#22
$-2/3I_F$	#33	#34
I_{PDH}	#2	#2

FORCING CONDITIONS

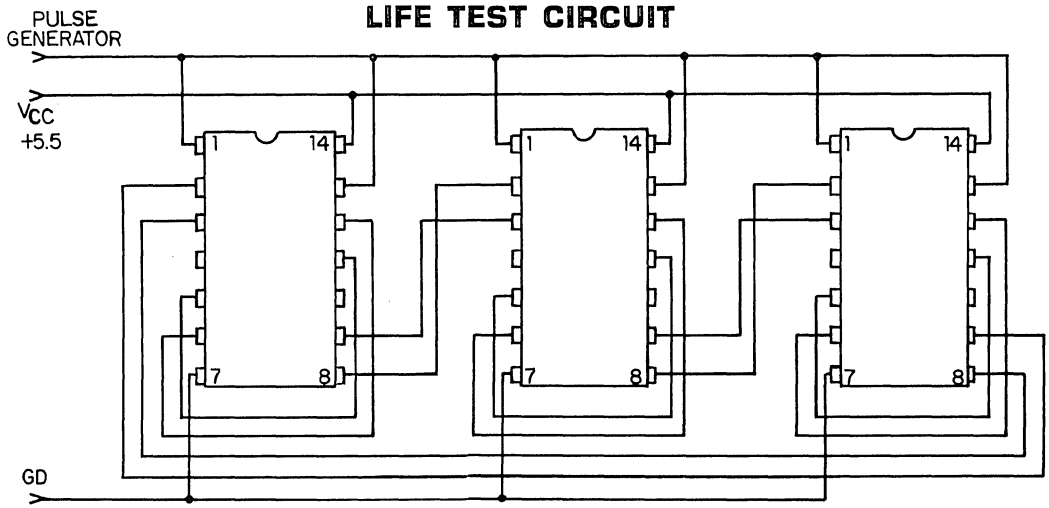
Parameter	Units	−55°C	+25°C	+125°C
V_{CCH}	Volts	5.5	5.5	5.5
V_{CCL}	Volts	4.5	4.5	4.5
V_{CEX}	Volts		4.5	
V_{MAX}	Volts		8.0	
V_{PD}	Volts		5.0	
V_{IH}	Volts	2.1	1.9	1.7
V_{IL}	Volts	1.4	1.1	0.8
V_F	Volts	0.4	0.4	0.4.
V_R	Volts	4.0	4.0	4.0
$-I_{OH}$	uA	115	115	115
I_{OH} 9093/9099	μA	180	180	180
I_{OH} 9094/9097	μA	540	540	540
I_{OL1} 9093/9099	mA	12.0	12.0	12.0
I_{OL2} 9093/9099	mA	15.0	15.0	15.0
I_{OL1} 9094/9097	mA	13.0	13.0	13.0
I_{OL2} 9094/9099	mA	13.6	13.6	13.6

Parameter	Units	0°C	+25°C	+75°C
V_{CCH}	Volts	5.0	5.0	5.0
V_{CCL}	Volts	5.0	5.0	5.0
V_{CEX}	Volts		5.0	
V_{MAX}	Volts		8.0	
V_{PD}	Volts		5.0	
V_{IH}	Volts	2.0	1.9	1.8
V_{IL}	Volts	1.2	1.1	0.95
V_F	Volts	0.45	0.45	0.45
V_R	Volts	4.0	4.0	4.0
$-I_{OH}$	uA	110	110	110
I_{OL} 9093/9099	mA	15.8	15.8	15.1
I_{OL} 9094/9097	mA	14.4	14.4	13.7
$-V_S$	Volts	−1.0	−1.0	−1.0





LIFE TEST CIRCUIT



MONOSTABLE MULTIVIBRATOR MIC 941/951

DESCRIPTION

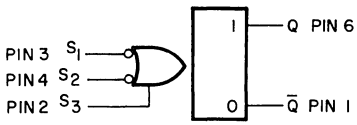
The MIC 941/951 is a monostable multivibrator.

The 941/951 provides a pair of complementary output pulses which are typically 100 nsec wide when it is triggered with an external pulse. The width of the output pulse is adjustable to greater than 100ns by the addition of an external resistor and/or capacitor.

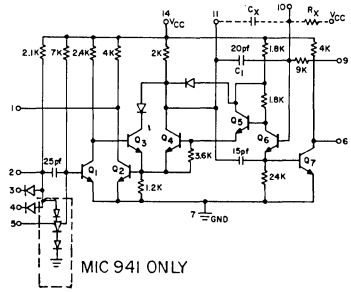
The output pulse width is very stable as either power supply voltage or temperature are varied when an external timing resistor is used instead of the internal diffused resistor.

This circuit is very useful in providing DTL compatible pulses from other sources.

POSTIVE LOGIC SYMBOLS

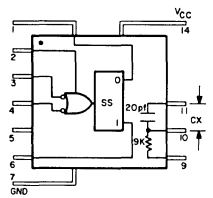


CIRCUIT SCHEMATIC

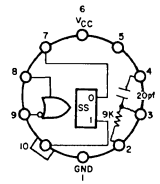


All data in this specification refers to 14-pin package numbers except TO-5 outline and the 10-pin reference numbers in the test sequence on Page 61.

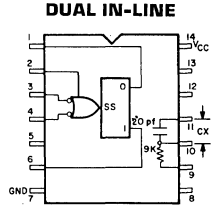
FLAT PACK



SIMILAR TO TO-5



DUAL IN-LINE



ABSOLUTE MAXIMUM RATINGS[1]

	UNITS
Supply Voltage (V_{CC}), −55°C to +125°C, continuous ..... −0.5 to +8	Volts
Supply Voltage (V_{CC}), pulsed, <1 sec ..... +12	Volts
Output Current, into outputs 50	mA
Current into Pin 10 5	mA
Input Forward Current ..... −10	mA
Input Reverse Current 1	mA
Operating Temperature ..... −55 to +125	°C
Storage Temperature ..... −65 to +150	°C
Operating Junction Temperature[2] ..... +175	°C
Lead Temp. (soldering, 60 sec.) ..... +300	°C
Input Voltage Applied to Input ..... −1.5 to +5.5	Volts

NOTES: 1. Above which useful life may be impaired.

2. Allow 200°C/Watt θ_{J-A} for TO-5; 300°C/Watt θ_{J-A} for ¼" x ¼" flatpack and dual in-line. Allow 50°C/Watt θ_{J-C} for TO-5; 180°C/Watt θ_{J-C} for ¼" x ¼" flatpack and dual in-line. Heat removal in ¼" x ¼" flatpack is highly dependent upon contact surfaces or air flow and on lead attachment and thermal paths thru leads, as well as number of soldered leads.

TEST SEQUENCE

Test	Pin no.:	5	1	2	3	4	6	7	9	10	11	14	LIMITS		
No.	TO-5 Pin no.:		7	8	9	—	10	1	2	3	4	6	Sense	Min.	Max.
1				V_F				GND				V_{CCH}	I_2	$-.5I_F$	
2					V_F	V_R		GND				V_{CCH}	I_3	$-.5I_F$	$-2I_{F1}$
3	Note 1				V_R	V_F		GND				V_{CCH}	I_4	$-.5I_F$	$-2I_{F1}$
4	Note 2							GND			V_F	V_{CCH}	I_{11}	$-.5I_F$	
5				GND	V_R			GND				V_{CCH}	I_3		I_R
6	Note 1			GND		V_R		GND				V_{CCH}	I_4		I_R
7			I_{OL1}					GND		GND		V_{CCL}	V_1		V_{OL1}
8		GND	I_{OL1}					GND				V_{CCL}	V_1		V_{OL1}
9							I_{OL1}	GND	V_{CCL}			V_{CCL}	V_6		V_{OL1}
10			$-I_{OH}$	GND				GND	V_{CCL}			V_{CCL}	V_1	V_{OH}	
11							I_{OH}	GND		GND		V_{CCL}	V_6	V_{OH}	
12								GND	V_{CCH}	GND		V_{CCH}	I_9	I_{9K}	I_{9K}
13					GND	GND		GND	V_{PD}			V_{PD}	I_9+I_{14}		I_{PDL}
14					GND	GND		GND				V_{MAX}	I_{14}		I_{MAX}
15								GND	V_{CCH}			V_{CCH}	V_2	V_{2L}	V_{2H}
16	t_{pd}— Pin 1	See Test Circuit Page 59													
17	t_{pd}+ Pin 6	See Test Circuit Page 59													
18	Pulse width Pin 1	See Test Circuit Page 59													
19	Pulse width Pin 6	See Test Circuit Page 59													
20	Note 3		I_{OL2}					GND		GND		V_{CCH}	V_1		V_{OL2}
21	Note 3	GND	I_{OL2}					GND				V_{CCH}	V_1		V_{OL2}
22	Note 3						I_{OL2}	GND	V_{CCH}			V_{CCH}	V_6		V_{OL2}
23	Note 3				V_F	V_R		GND				V_{CCL}	I_3		$-2\ I_{F2}$
24	Note 3				V_R	V_F		GND				V_{CCL}	I_4		$-2\ I_{F2}$

NOTE: 1. These tests do not apply to 10-pin TO-5 packages. 2. Applies to limited temperature range only.
3. Tests 20/24 apply to full temperature range only.

FORCING CONDITIONS

		FULL TEMPERATURE RANGE			LIMITED TEMPERATURE RANGE				
Parameter	Units	−55°C	+25°C	+125°C	Parameter	Units	0°C	+25°C	+75°C
V_{CCH}	Volts	5.5	5.5	5.5	V_{CCH}	Volts	5.0	5.0	5.0
V_{CCL}	Volts	4.5	4.5	4.5	V_{CCL}	Volts	5.0	5.0	5.0
V_{PD}	Volts		5.0		V_{PD}	Volts		5.0	
V_{MAX}	Volts		8.0		V_{MAX}	Volts		8.0	
V_R	Volts	4.0	4.0	4.0	V_R	Volts	4.0	4.0	4.0
V_F	Volts	0.4	0.4	0.4	V_F	Volts	.45	.45	.5
$I_{OL1,2}$	mA	15.0	15.0	15.0	I_{OL}	mA	14.8	14.8	14.0
$-I_{OH}$	mA	.18	.18	.18	$-I_{OH}$	mA	.15	.15	.15

TEST LIMITS

		FULL TEMPERATURE RANGE						LIMITED TEMPERATURE RANGE					
		−55°C		+25°C		+125°C		0°C		+25°C		+75°C	
Parameter	Units	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.
$-.5I_F$	mA	0.8		0.8		0.75		.65		.6		.65	
$-2I_{F1}$	mA		2.93		2.93		2.75		2.6		2.8		2.66
I_R	μA		5.0		5.0		10.0		5.0		5.0		10.0
V_{OL1}	Volts		.4		.4		.4		.5		.45		.5
V_{OH}	Volts	2.5		2.5		2.5		3.2		3.2		3.2	
I_{9K}	mA			.5	.75					.4	.95		
I_{PDL}	mA				9.0						11.8		
I_{MAX}	mA				21.4						23.1		
V_{2L} 941	Volts			1.8	2.5					1.7	2.6		
V_{2H} 951	Volts			5.0						4.5			
V_{OL2}	Volts		.4		.4		.4						
$-2\ I_{F2}$	mA		2.26		2.26		2.22						

MIC 951 SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

TEST LIMITS

	Limited Temp. Range		Full Temp. Range	
	Min. Nano-seconds	Max. Nano-seconds	Min. Nano-seconds	Max. Nano-seconds
$t_{pd}-$		40		40
$t_{pd}+$		40		40
Pin 1	90	330	90	220
Pin 6	70	270	70	160

FIG. 115

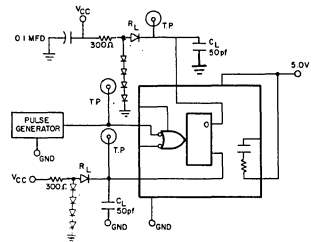
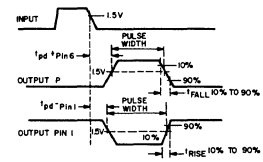


FIG. 116



Suitable precautions must be used when wiring test jig.

TYPICAL DC CHARACTERISTICS

FIG. 117

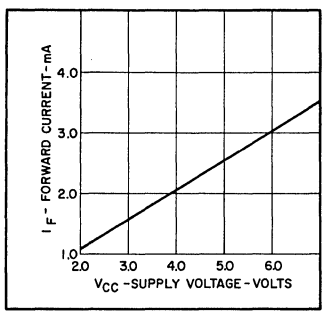


FIG. 118

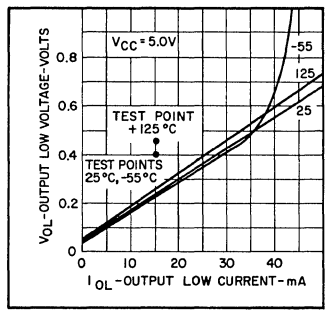
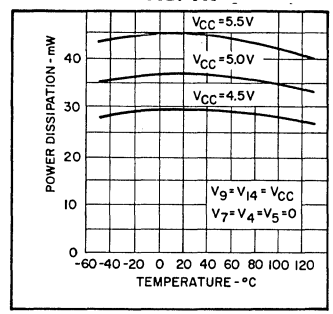


FIG. 119



TIMING CHARACTERISTICS

FIG. 120

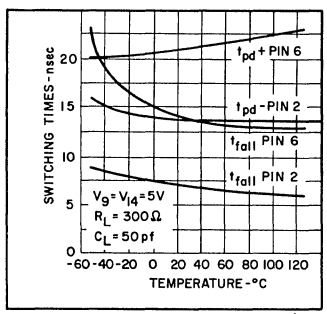


FIG. 121

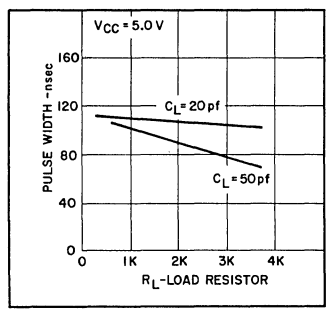


FIG. 122

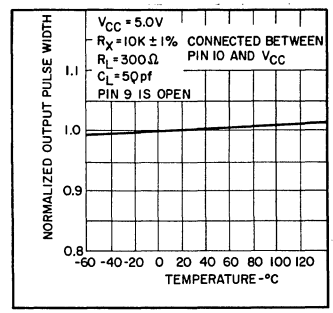


FIG. 123

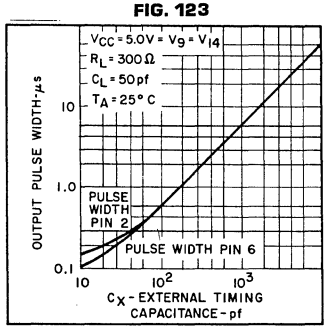


FIG. 124

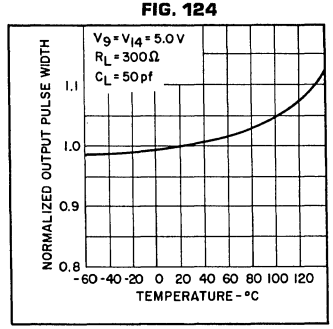
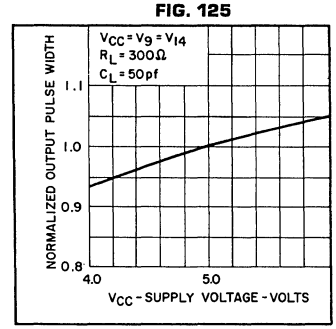


FIG. 125



INPUT-OUTPUT LOAD FACTORS

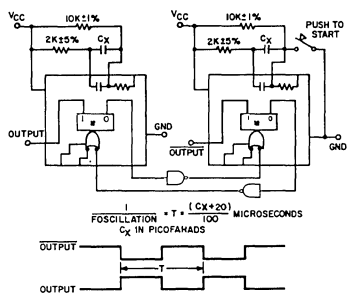
1. Each MIC 951 input should be rated at 2 loads.
2. Each MIC 951 output may drive 10 DTL loads.
3. For input-output load factors of other DTL elements, please refer to the individual DTL element specifications.

APPLICATIONS

RULES FOR USE OF MIC 951

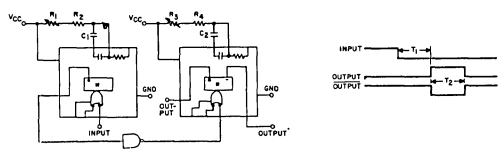
1. With Pin 9 connected to V_{CC} and no external capacitor (C_X), the output pulse width is approximately 100 nsec.
2. With Pin 9 connected to V_{CC} and an external capacitor (C_X) connected between Pins 10 and 11, the output pulse width (T) is: $T \approx 4.5\ (C_X+20)$ with C_X in pf and T in nsec.
3. For improved pulse width control, Pin 9 is left open and a stable external resistor (R_X) of 9 KΩ minimum to 15 KΩ maximum is connected from Pin 10 to V_{CC}. The output pulse width is given by the expression: $T \approx 0.5\ R_X\ (C_X+20)$ with R_X in KΩ, C_X in pf and T in nsec. (See Fig. 126)

FIG. 126



4. The output duty cycle (pulse width/period) should not exceed 40%. It may be increased to 50% by adding a 2-KΩ resistor between Pin 11 and V_{CC}. Higher duty cycles are obtainable but the output pulse width and performance are less predictable.
5. The maximum input fall time to trigger: 25 nsec for a 1.0-volt swing; 50 nsec for a 2.0-volt swing; 100 nsec for a 4.0-volt swing.
6. The AC sensitivity of the inputs may be decreased by connecting a capacitor between Pin 5 and ground.
7. The minimum pulse width at output Pin 1 is approximately 100 nsec. This pulse width may be decreased to 50 nsec by connecting a 10-KΩ resistor between Pin 5 and V_{CC}.

FIG. 127



Explanation

The input 951 determines T_1, the time before the initiation of the output pulse. The second or output 951 determines T_2, the output pulse width.

With R_2 = 10KΩ and R_1 a 5-KΩ potentiometer, T_1 is variable over a range of 2 to 3 and is given by $T_1 \approx 0.5\ (R_1+R_2)\ (C_1+20\ pf)$.

Similarly, with R_4 = 10KΩ and R_3 a 5-KΩ potentiometer, T_2 is $\approx 0.5(R_3+R_4)\ (C_2+20\ pf)$ and T_2 can be controlled by the potentiometer over a range of 2 to 3 since $10K\Omega \leq (R_3+R_4) \leq 15K\Omega$.

A much greater range in T_1 and T_2 is available by varying C_1 and C_2.

RELIABILITY TESTS

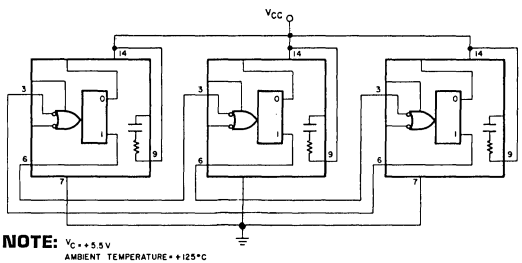
PERFORMED DURING ITT RELIABILITY PROGRAM

MEASUREMENTS OF THE FOLLOWING PARAMETERS ARE RECORDED:

Parameter	Test Sequence Number on Page 57
I_F	#2
I_R	#6
V_{OL}	#8
V_{OH}	#11
I_{MAX}	#14

LIFE TEST CIRCUIT

FIG. 128



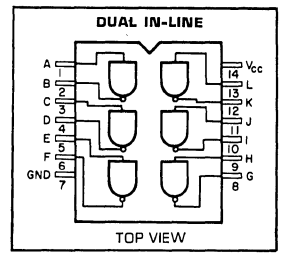
NOTE: V_{CC} = 5.5 V
AMBIENT TEMPERATURE = +125°C

HIGH LEVEL HEX INVERTER 9109, 9110, 9112

The ITT High Level Logic DTL family consists of three high voltage, high threshold hex inverters which offer extremely good D.C. and A.C. noise immunity. These circuits are useful in applications involving a high noise environment or high voltage supply which prohibits the use of current sinking logic.

Interfacing from current sinking logic to HLL is accomplished with the 9112, shifting from HLL to current sinking logic is accomplished with the 9109, and inverting HLL is done with the 9110.

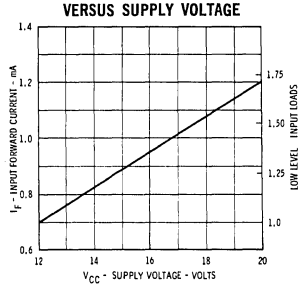
- DTL compatibility
- High Voltage Operation 12 to 20V.
- Fan Out=7 CSL.
- D.C. noise immunity 6.5V
- External input diodes to facilitate high density building block approach.



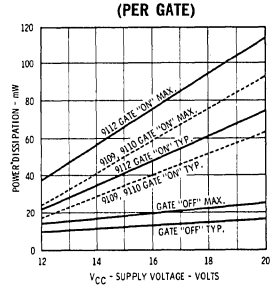
ABSOLUTE MAXIMUM RATINGS[1]

Storage Temperature	−65°C to +150°C
Operating Temperature	0°C to +75°C
Vcc Pin Potential to GND Pin	−5V to +25V
Output Current When Output is Low	40mA
Input Current (9109, 9110)	10mA
Output Voltage	25V
Input Voltage (9112)	5.5V

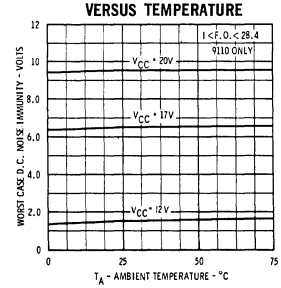
WORST CASE INPUT FORWARD CURRENT AND INPUT LOADS VERSUS SUPPLY VOLTAGE



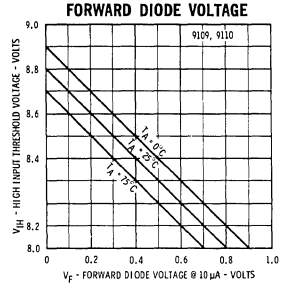
WORST CASE POWER DISSIPATION VERSUS SUPPLY VOLTAGE (PER GATE)



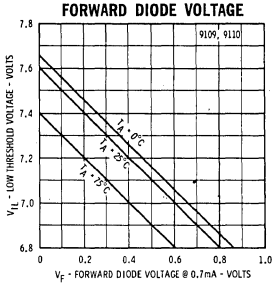
WORST CASE HIGH LEVEL D.C. NOISE IMMUNITY VERSUS TEMPERATURE



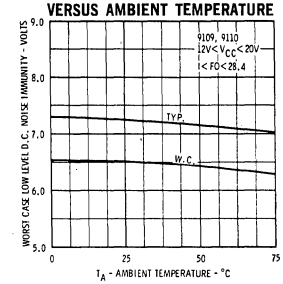
WORST CASE HIGH INPUT THRESHOLD VOLTAGE VERSUS FORWARD DIODE VOLTAGE



WORST CASE LOW THRESHOLD VOLTAGE VERSUS FORWARD DIODE VOLTAGE



WORST CASE LOW LEVEL D.C. NOISE IMMUNITY VERSUS AMBIENT TEMPERATURE



SILICON GATE MOS STATIC SHIFT REGISTER

- **Direct Bipolar Compatibility**
- **3MHz Operation Guaranteed (Typically 5MHz,-55 c to +125 c)**
- **22pF Clockline Capacitance (Max.)**
- **1.0mW/Bit Power Dissipation (Max.) including Internal clock Generator**
- **Input Overvoltage Protection**
- **10 Lead TO-100 Package**
- **Length Selectable to 144,138 or 125 Bits**

The ITT1144 is a single selectable 125,138 or 144 bit single-phase static shift register. It is a monolithic integrated circuit utilizing P-channel enhancement mode SILICON GATE MOS technology. The output buffer is capable of driving both low level MOS and bipolar loads directly.

FUNCTIONAL DESCRIPTION – The 1144 is a straight "pipe line" single phase static shift register. Data is accepted at the input when the clock is negative and data is available at the output after the positive going clock transition. The output stage is push-pull, and can sink one TTL load to VDD (1.6mA at 0.4V). Bipolar compatible operation is achieved by connecting VSS to +5.0V, VDD to OV, and VGG to -12V. Register length of 144, 138, or 125 BITS is determined by the state of control inputs S1 and S2, as defined by the following truth table.

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

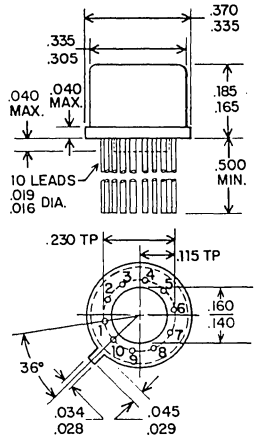
CHARACTERISTICS	UNITS
All inputs including Ø,S1 and S2 (Note 2) . . . –24V to +0.3	V
V_{GG} (Note 2) . . . . . –20V to +0.3	V
V_{DD} and Output (Note 2) . . . . . –7.0V to +0.3	V
Output Current when Output is low (Note 1) 10	mA
Storage Temperature . . . . . –55 C to +150	°C
Operating Temperature . . . . . –55 to +125	°C

Note 1: Low logic level is most negative level and high logic level is most positive level.
Note 2: All voltages with respect to V_{SS}.

TRUTH TABLE

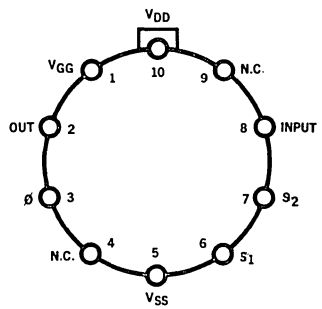
REGISTER LENGTH	S_1	S_2
144	V_{SS}	V_{GG}
138	V_{GG}	V_{GG}
125	V_{SS} or V_{GG}	V_{SS}

PHYSICAL DIMENSIONS

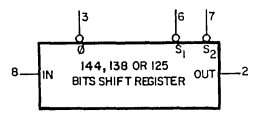


NOTES: LEADS ARE GOLD-PLATED KOVAR
PACKAGE WEIGHT IS 1.32 GRAMS

CONNECTION DIAGRAM
(TOP VIEW)



LOGIC SYMBOL



ORDERING CODE:
ITT1144–5C 0 to 70°C
ITT1144–1C –55 to 125°C

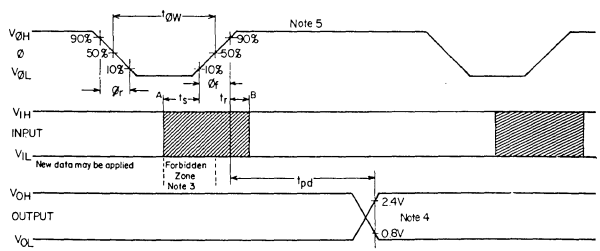
D.C. CHARACTERISTICS (T_A = −55°C to 125°C, V_{SS} = 5.0V±10%, V_{DD}=0V, V_{GG} = −12V±10%)

SYMBOL	CHARACTERISTICS	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
V_{OH}	Output High Voltage	V_{SS}−.5		V_{SS}	Volts	I_{OH} = −200uA
V_{OL}	Output Low Voltage			0.4	Volts	I_{OL} = 1.6mA note 1
V_{1H}	Input High Voltage	V_{SS}−1.0		V_{SS}+0.3	Volts	
V_{1L}	Input Low Voltage	V_{GG}		0.80	Volts	
I_{IL6},I_{IL7}	Control Input Low Current			10	uA	V_{6L},V_{7L}=V_{GG},T_A=25°C
I_{IH6},I_{IH7}	Control Input High Current		50	100	uA	V_{6H},V_{7H}=V_{SS},T_A=25°C
I_{1L}	Input Low Load Current			10	uA	V_1=−15.0V,T_A=25°C
$V\emptyset_H$	Clock Input High Voltage	V_{SS}−1.0		V_{SS}+0.3	Volts	
$V\emptyset_L$	Clock Input Low Voltage	−15.0		−10.0	Volts	
$I\emptyset_L$	Clock Input Leakage			10	uA	V$\emptyset$= −15V, T_A=25°C
R_{OH}	Impedance of Output High		1.0	2.5	kohms	I_{out} =200uA
R_{OL}	Impedance of Output Low		180	250	ohms	I_{out}= −1.6mA
I_{GG}	V_{GG} Current		−3.0	−4.5	mA	V_{SS}=5.5V,V_{GG}=−13.2V
I_{DD}	V_{DD} Current		−9	−11.5	mA	V$\emptyset_L$=−13.2
I_{SS}	V_{SS} Current		12	15	mA	T_A=25°C
P_D	Power Dissipation		110	150	mW	Clock Duty Cycle=30%

A.C. CHARACTERISTICS (T_A=−55°C to 125°C,V_{SS}=5.0V ± 10%,V_{DD}=0V,V_{GG}=−12V ± 10%) (See Fig. 1)

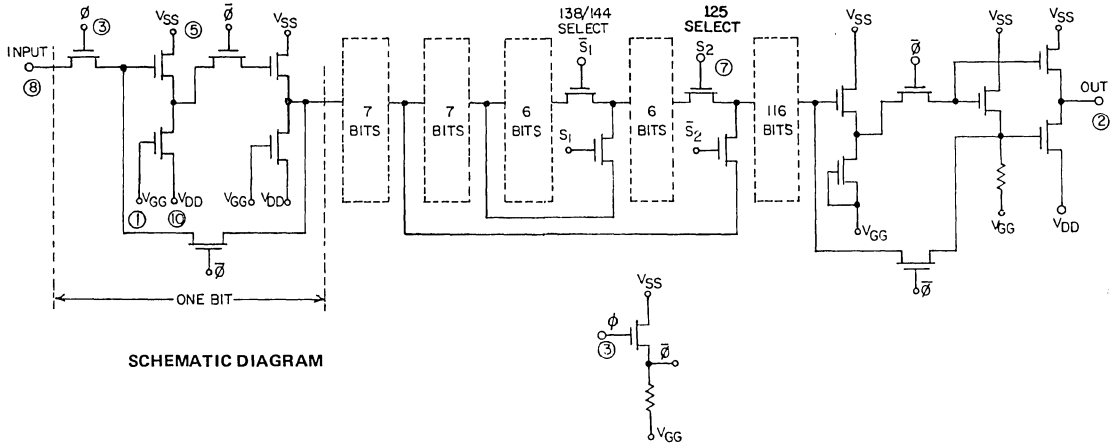
SYMBOL	CHARACTERISTICS	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
$t_{\emptyset W}$	Clock Pulse Width	0.1		20	uS	T_A = 70°C
				2	uS	70°C<T_A ≤125°C
$\emptyset_r$,$\emptyset_f$	Clock Rise & Fall Times (10% − 90%)			1.0	uS	
C$\emptyset$	Clock Capacitance		16	22	pF	V_{IN},V$\emptyset$=V_{SS} f=1.0 MHz
CIN	Input Capacitance		4	5		
f	Operating Frequency	D.C.		3.0	MHz	
t_s	Input Set Up Time			50	ns	
t_r	Input Release Time	0			ns	
t_{pd+}	Delay from Ø High to High Level at Output (V_{OH} = 2.4V)			150	ns	C_L = 10pF, Load = 1 DTL Input
t_{pd-}	Delay from Ø High to Low Level at Output (V_{OL} = .8V)			150	ns	C_L = 10pF, Load = 1 DTL Input

Fig. 1
TIMING DIAGRAM
See Test Circut.



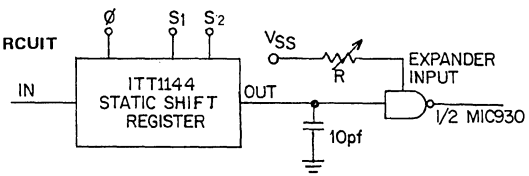
Note 3: A and B define a window during which the input to the shift register is setting up. If the input data changes during this window, the change may or may not be detected. To avoid this ambiguous operation, the input data must remain good between A and B.

Note 4: The outputs remain good until a new output appears.
Note 5: Data is stored indefinitely only when Ø is high.



SCHEMATIC DIAGRAM

PROPAGATION DELAY TEST CIRCUIT



V_{SS} = +4.5V
V_{GG} = −10.8V
V_{DD} = 0V

Propagation delay is measured with register output loaded with one DTL gate and a discrete 10pf capacitor. The DTL gate input current is adjusted to 1.6mA by means of a resistor tied between V_{SS} and the gate expander terminal.

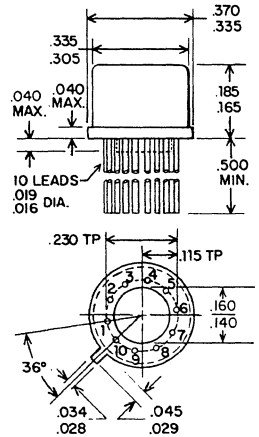
ITT3329

512 BIT DYNAMIC SHIFT REGISTER

SILICON GATE MOS SHIFT REGISTER

- **Direct Bipolar Compatibility**
- **2 MHz Operation Guaranteed (Typically from 1 kHz to 4 MHz)**
- **45 pF Clockline Capacitance (Max.)**
- **0.5 mW/Bit Power Dissipation (Max) at 2 MHz**
- **Input Overvoltage Protection**
- **10 Lead to-100 Package**

PHYSICAL DIMENSIONS

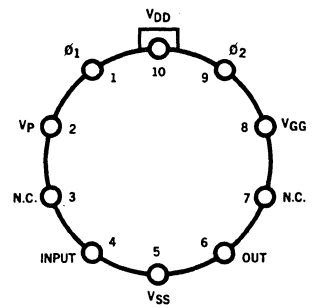


NOTES: LEADS ARE GOLD-PLATED KOVAR
PACKAGE WEIGHT IS 1.32 GRAMS

The ITT 3329 is a single 512 bit, two-phase dynamic shift register. It is a monolithic integrated circuit utilizing P-channel enhancement mode SILICON GATE MOS technology. An on-chip input resistor allows direct bipolar compatibility by tying the V_P pin to V_{DD}. The output buffer is capable of driving both low level MOS and bipolar loads directly without addition of an external resistor.

FUNCTIONAL DESCRIPTION – The 3329 is a straight "pipe line" two phase dynamic shift register. The functions ϕ_1 and ϕ_2 are non-overlapping and negative as illustrated in Figure 1. Data is accepted at the input when ϕ_1 is negative and data is available at the output after negative going transition of ϕ_2. The input is connected by a MOS transistor to V_{SS}; this transistor acts as an externally controlled pull-up resistor allowing complete TTL compatibility. The output stage is push-pull, and can sink one TTL load to V_{DD} (1.6 mA at 0.4 V). Bipolar compatible operation is achieved by connecting V_{SS} to +5.0 V, V_{DD} to 0 V, and V_{GG} to −12 V, with V_P, the control pin to the input pull-up resistor tied to V_{DD}.

CONNECTION DIAGRAM
(TOP VIEW)

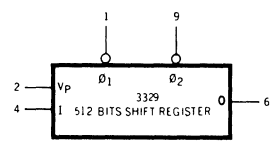


ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

CHARACTERISTICS	UNITS
All Inputs including ϕ_1, ϕ_2 and V_P (Notes 1 & 3) . . . . . −24 V to +0.3	V
V_{GG} (Note 3) . . . . . −24 V to +0.3	V
V_{DD} and Output (Note 3) . . . . . −7.0 V to +0.3	V
Output Current when Output is low (Note 2) 10	mA
Storage Temperature . . . . . −55°C to +150	°C
Operating Temperature . . . . . 0°C to +70	°C

Note 1: V_P must be tied to V_{SS} if data input is between −7 V and −24 V.
Note 2: Low logic level is most negative level and high logic level is most positive level.
Note 3: All voltages with respect to V_{SS}.

LOGIC SYMBOL



V_{SS} = PIN 5
V_{DD} = PIN 10
V_{GG} = PIN 8

ORDERING CODE: ITT3329-5C

D.C. CHARACTERISTICS ($T_A = 0°C$ to $+70°C$, $V_{SS} = 5.0\ V \pm 10\%$, $V_{DD} = 0\ V$, $V_{GG} = -12\ V \pm 10\%$)

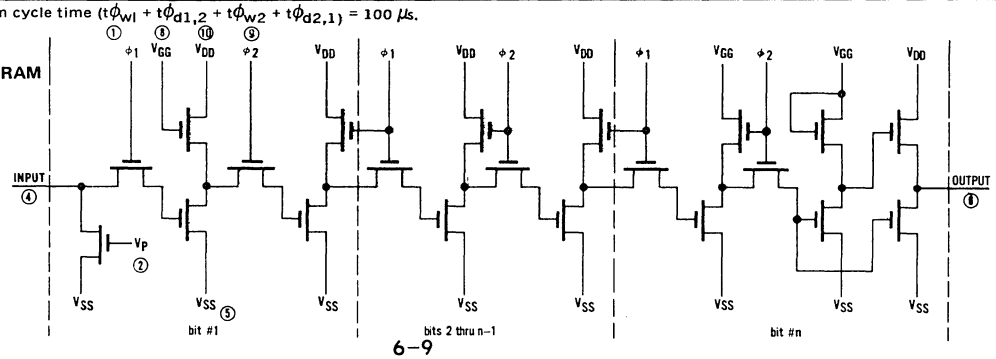
SYMBOL	CHARACTERISTICS	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
V_{OH}	Output High Voltage	$V_{SS}-0.6$		V_{SS}	Volts	$I_{OH} = -0.5$ mA
V_{OL}	Output Low Voltage	0	0.24	0.4	Volts	$I_{OL} = 1.6$ mA
V_{IH}	Input High Voltage	$V_{SS}-1.0$			Volts	
V_{IL}	Input Low Voltage	V_{GG}		0.85	Volts	$V_P = V_{SS}$ if V_1 is negative
I_{IH}	Input High Load Current	0.17			mA	$V_1 = V_{SS}-1$, $V_P = V_{DD}$
I_{IL}	Input Low Load Current		1.0	1.60	mA	$V_1 = 0.4$ V, $V_P = V_{DD}$
I_{IL}	Input Low Load Current			1.0	μA	$V_1 = -5.0$ V, $V_P = V_{SS}$, $T_A = 25°C$
$V\phi_H$	Clock Input High Voltage	$V_{SS}-1.0$		V_{SS}	Volts	
$V\phi_L$	Clock Input Low Voltage	−6.5		−4.5	Volts	
$I\phi_L$	Clock Input Leakage			1.0	μA	$V\phi = -10$ V, $T_A = 25°C$
R_{OH}	Impedance of Output High		0.7	1.0	kohms	$V_{OUT} = V_{SS}-0.5$ V
R_{OL}	Impedance of Output Low		150	250	ohms	$V_{OUT} = V_{OL}$
I_{GG}	V_{GG} Current		−2.4	−3.0	mA	$V_{SS} = 5.5$ V, $V_{GG} = -13.2$ V
I_{DD}	V_{DD} Current		−28	−35	mA	$V\phi_L = -6.5$ V, $T_A = 25°C$, f = 2.0 MHz, $t\phi_w = 200$ ns
I_{SS}	V_{SS} Current		30.4	38	mA	
P_D	Power Dissipation		200	250	mW	

A.C. CHARACTERISTICS ($T_A = 0°C$ to $+70°C$, $V_{SS} = 5.0\ V \pm 10\%$, $V_{DD} = 0\ V$, $V_{GG} = -12\ V \pm 10\%$) (See Fig. 1)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
$t\phi_w$	Clock Pulse Width	0.2		100	μs	Note 4
$t\phi_d$	Time Between Clocks	0		100	μs	Note 4
ϕ_r, ϕ_f	Clock Rise & Fall Times (10% - 90%)			1.0	μs	
$C\phi$	Clock Capacitance (Each clockline)			45	pF	$V\phi = V_{SS}$, f = 1.0 MHz
f	Operating Frequency	0.01		2.0	MHz	
t_s	Input Set Up Time			100	ns	
t_r	Input Release Time	0			ns	
t_{pd+}	Delay from ϕ_2 to High Level at Output			150	ns	$C_L = 10$ pF, Load = 1 TTL Input
t_{pd-}	Delay from ϕ_2 to Low Level at Output			150	ns	$C_L = 10$ pF, Load = 1 TTL Input

Note 4: Maximum cycle time ($t\phi_{w1} + t\phi_{d1,2} + t\phi_{w2} + t\phi_{d2,1}$) = 100 μs.

SCHEMATIC DIAGRAM



○ = Pin Number

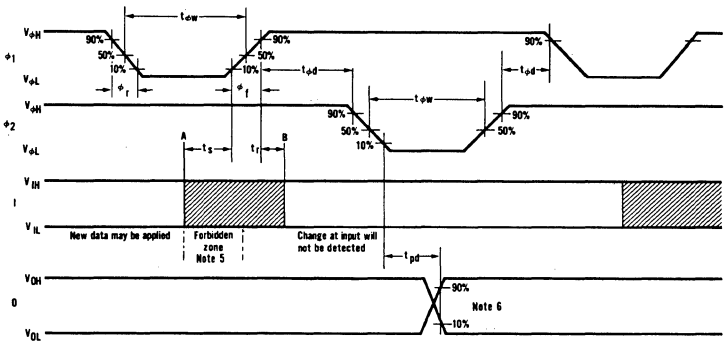


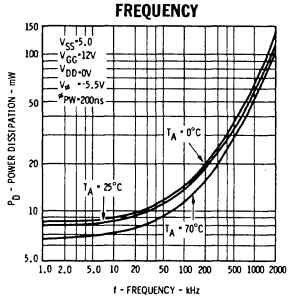
Fig. 1 - TIMING DIAGRAM

Note 5: A and B define a window during which the input to the shift register is setting up. If the input data changes during this window, the change may or may not be detected. To avoid this ambiguous operation, the input data must remain good between A and B.

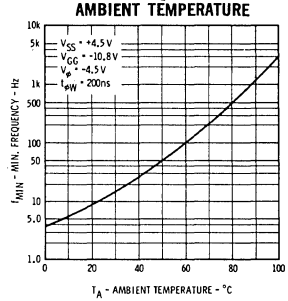
Note 6: The outputs remain good until a new output appears.

TYPICAL ELECTRICAL CHARACTERISTICS

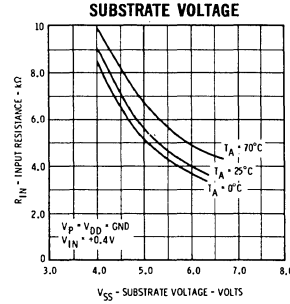
POWER DISSIPATION VERSUS FREQUENCY



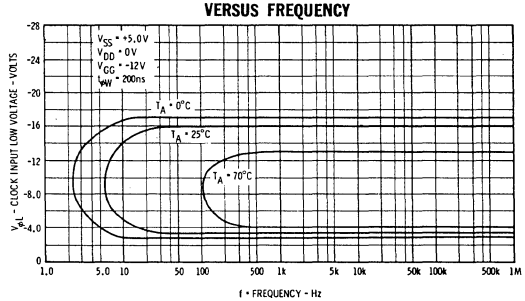
MINIMUM FREQUENCY VERSUS AMBIENT TEMPERATURE



INPUT RESISTANCE VERSUS SUBSTRATE VOLTAGE



CLOCK INPUT LOW VOLTAGE VERSUS FREQUENCY



APPLICATIONS

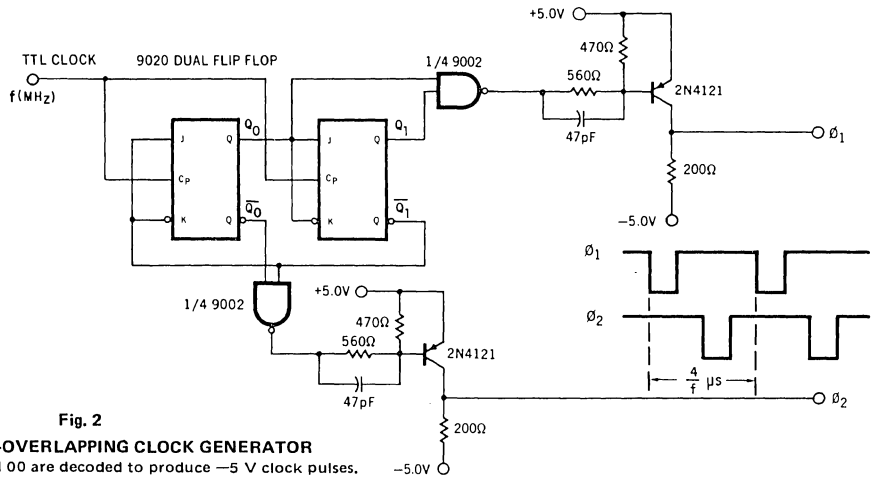


Fig. 2

TWO-PHASE NON-OVERLAPPING CLOCK GENERATOR

The counter states 11 and 00 are decoded to produce —5 V clock pulses.

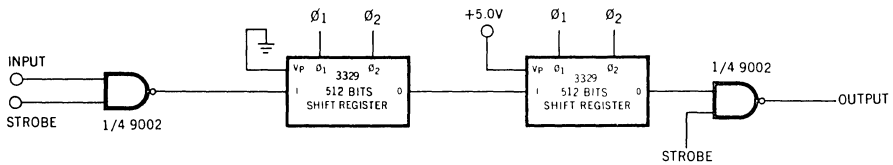


Fig. 3– SHIFT REGISTER INTERFACE

The shift register inputs may be connected directly to a TTL or DTL output if V_P is tied to ground. If the input is to be driven by a MOS output, V_P is tied to V_{SS}. The output can drive TTL or DTL directly. No external components are required.

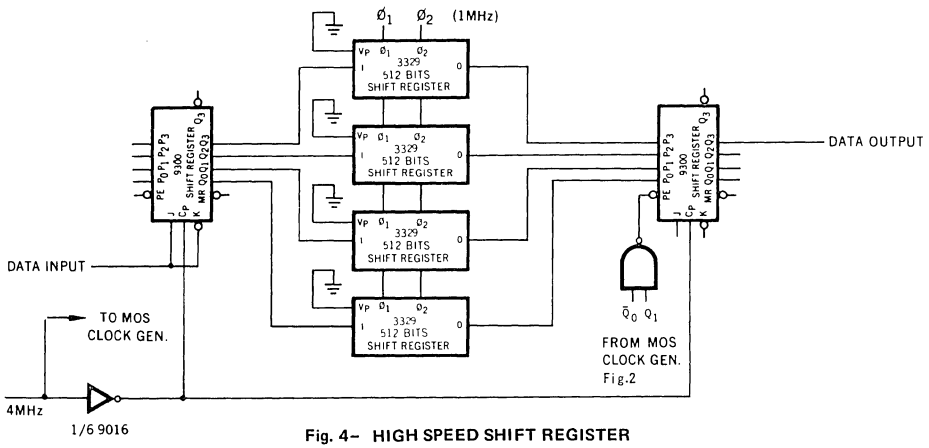


Fig. 4– HIGH SPEED SHIFT REGISTER

Four shift registers may be connected as shown in the figure above to simulate one long high speed shift register. The 9300 MSI shift register on the left is used as a serial to parallel converter. Data is clocked into the 9300 at four times the clock rate of the silicon-gate shift registers. When four bits have been clocked in, they are loaded into the four long shift registers. At the output of the silicon-gate registers, another 9300 is used to re-serialize the data at the higher clock rate. Because the 9300's add several bits of delay, the system illustrated looks like a high speed 4x512+5 bit register.

Note that the clock period of the 9300's must be greater than the input set up time on the silicon-gate registers.

MOS 8 CHANNEL MULTIPLEX SWITCH

- **Input Logic Levels Compatible with TTL and DTL**
- **One-Out-Of-Eight Decoder on the Chip**
- **High On/Off Ratio**
- **Output Enable Control**
- **Input Gate Protection**
- **Low Leakage Current**
- **Zero Offset Voltage**
- **Fast Switching Time 0.8 μs (TYP) AT T_A = +85°C**

The ITT 3708 is an eight-channel multiplex switch with output enable control and one-out-of-eight decoder included on the chip. It is a monolithic integrated circuit utilizing P-channel enhancement mode silicon gate technology. The logic input lines of the 3708 are NPN bipolar compatible and can be used directly with TTL and DTL 5.0 volt logic levels with no level-shifting interface required. This device is intended for use in A/D converters, multiplexing in analog or digital data transmission systems, and other airborne or ground instrumentation signal routing applications.

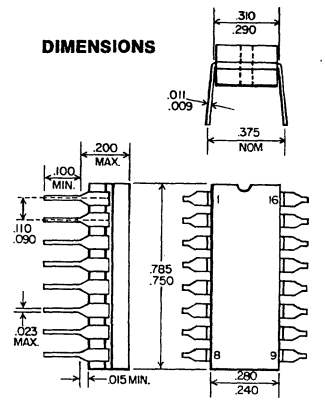
ABSOLUTE MAXIMUM RATINGS (Notes 1 and 2)

CHARACTERISTICS	UNITS
Storage Temperature . . . . . −65°C to +150	°C
Operating Temperature . . . . . −55°C to +85	°C
Positive Voltage on any pin . . . . . +0.3	V
Negative Voltage on digital and analog input pins . . . . . −30	V
and analog output pins . . . . . −30	V
Negative Voltage on V_{DD} pin . . . . . −30	V
Total power dissipation in package (T_A = 25°C) 200	mW

NOTES:

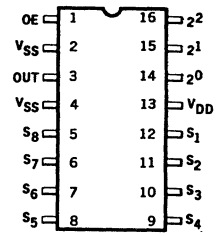
(1) These ratings are limiting values above which the serviceability of the device may be impaired.
(2) Voltage ratings are all referenced to pins 2 and 4 (V_{SS}).

DIMENSIONS



NOTES: All dimensions in inches.
Leads are intended for insertion in hole rows on .300" centers. They are purposely shipped with "positive" misalignment to facilitate insertion.

PIN CONFIGURATION
(16 Lead DIP)



TRUTH TABLE

LOGIC INPUTS				CHANNEL
2^0	2^1	2^2	OE	'ON'
L	L	L	H	S_1
H	L	L	H	S_2
L	H	L	H	S_3
H	H	L	H	S_4
L	L	H	H	S_5
H	L	H	H	S_6
L	H	H	H	S_7
H	H	H	H	S_8
X	X	X	L	OFF

ELECTRICAL CHARACTERISTICS

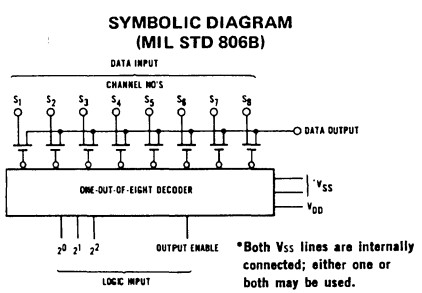
For ITT3708-2D2 $-5.0V<V_{OUT}<+5.0V$, $T_A = 25°C$, $-18\ V<V_{DD}<-20\ V$, $5.0\ V<V_{SS}<6.0\ V$ unless otherwise specified

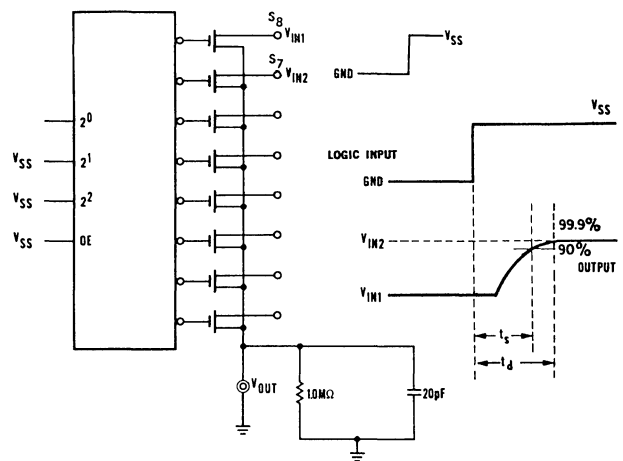
For ITT3708-2D3 $0\ V<V_{OUT}<+5.0\ V$, $T_A = 25°C$, $-18\ V<V_{DD}<-20\ V$, $5.0\ V<V_{SS}<6.0\ V$ unless otherwise specified

SYMBOL	CHARACTERISTICS	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
R_{ON}	Data Channel "ON" Resistance					
	2D2		250	400	Ω	$V_{OUT} = -5.0\ V$, $I_{OUT} = -100\ \mu A$
	2D3		190	350	Ω	$V_{OUT} = 0\ V$, $I_{OUT} = -100\ \mu A$
R_{ON}	Data Channel "ON" Resistance		125		Ω	$V_{DD} = -20\ V$, $V_{SS} = +5.0\ V$, $I_{OUT} = -100\ \mu A$
R_{OFF}	Data Channel "OFF" Resistance	1.5	5.0		GΩ	$V_{SS}-V_{OUT} = 15\ V$
I_{LO}	Output Leakage Current		2.0	10	nA	$V_{SS}-V_{OUT} = 15\ V$
I_{LO} (85°)	Output Leakage Current		100	500	nA	$V_{SS}-V_{OUT} = 15\ V$
I_{LDI}	Data Input Leakage Current					
	2D2			3.0	nA	$V_{SS}-V_{IN} = 15\ V$
	2D3			2.0	nA	$V_{SS}-V_{IN} = 10\ V$
I_{LI}	Logic Input Leakage Current			1.0	μA	$V_{SS}-V_{LOGIC\text{-}IN} = 15\ V$
*V_{IL}	Logic Gate Input "Low" Level	V_{DD}		+0.2	V	
*V_{IH}	Logic Gate Input "High" Level	$V_{SS}-1.5$		V_{SS}	V	
t_s	Channel Switching Time (See Fig. 1)		0.45		μs	
t_s (85°C)	Channel Switching Time (See Fig. 1)		0.8	1.5	μs	
t_d	Channel Switching Time (See Fig. 1)		1.0	2.5	μs	
C_{db}	Output Capacitance		25		pF	$V_{SS}-V_{OUT} = 0\ V$, f = 1.0 MHz
C_{is}	Data Input Capacitance		4.5		pF	$V_{SS}-V_{IN} = 0\ V$, f = 1.0 MHz
C_{ig}	Logic Input Capacitance		3.0	175	pF	$V_{SS}-V_{LOGIC\text{-}IN} = 0\ V$, f = 1.0 MHz
P_D	Power Dissipation		130		mW	$V_{DD} = -26\ V$, $V_{SS} = 0\ V$

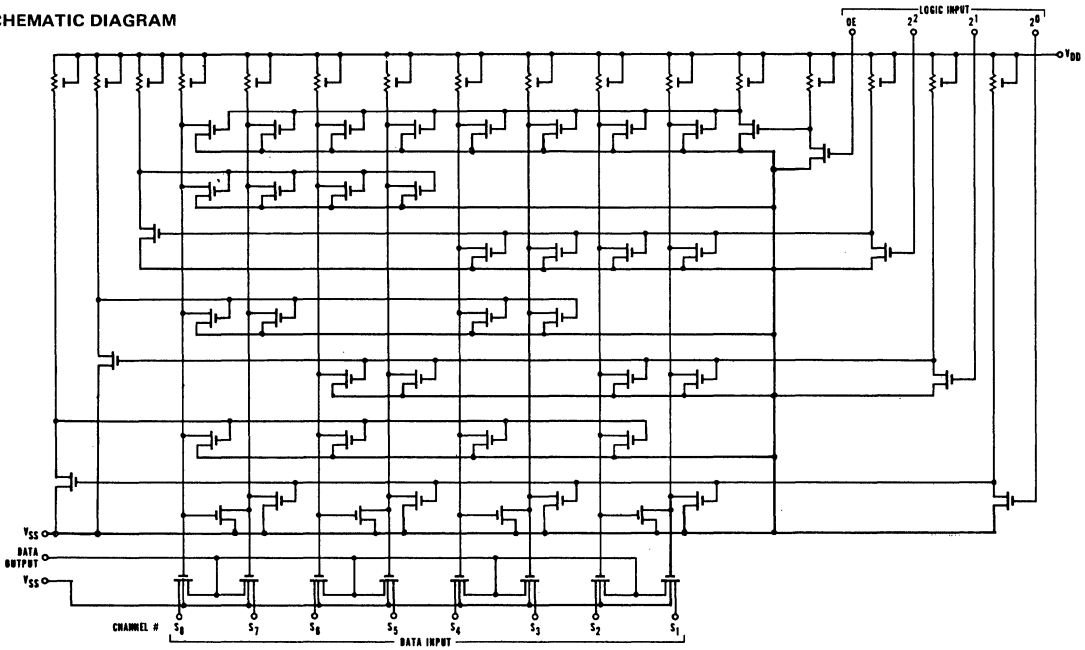
*When driven by DTL and TTL elements, avoid excessive D.C. loading of DTL and TTL elements to insure 3708 logic levels under maximum fan-out conditions. Analog input signal swing should not exceed V_{SS} (= V_{CC}).

Fig. 1— SWITCHING TIME TEST CIRCUIT



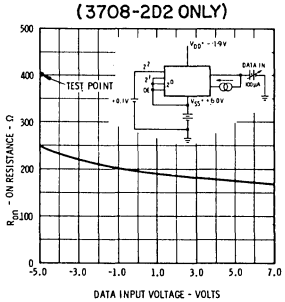


SCHEMATIC DIAGRAM

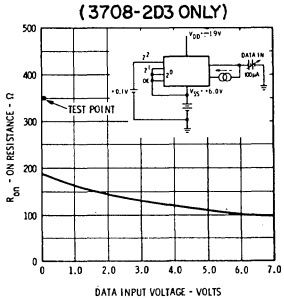


TYPICAL DEVICE CHARACTERISTICS

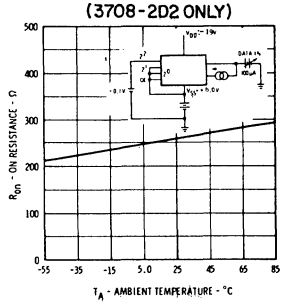
ON RESISTANCE VERSUS DATA INPUT VOLTAGE (3708-2D2 ONLY)



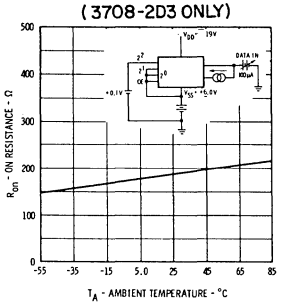
ON RESISTANCE VERSUS DATA INPUT VOLTAGE (3708-2D3 ONLY)



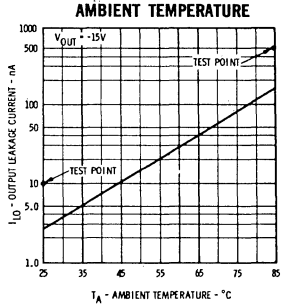
ON RESISTANCE VERSUS AMBIENT TEMPERATURE (3708-2D2 ONLY)



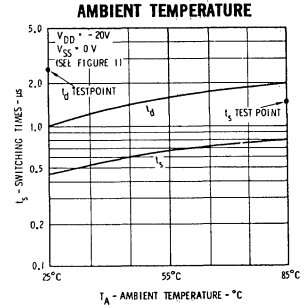
ON RESISTANCE VERSUS AMBIENT TEMPERATURE (3708-2D3 ONLY)

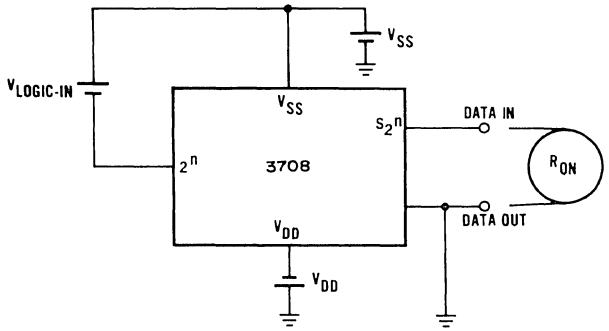


OUTPUT LEAKAGE CURRENT VERSUS AMBIENT TEMPERATURE



SWITCHING TIME VERSUS AMBIENT TEMPERATURE

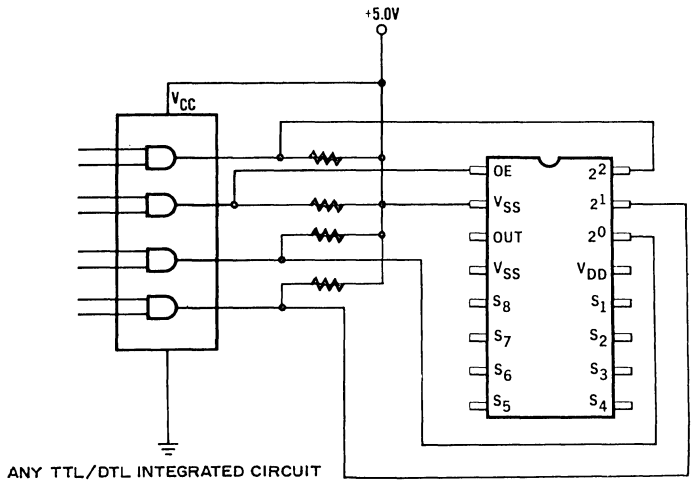




The following sets of power supplies are equivalent:

	CONDITION 1	CONDITION 2
DATA IN	+5.0 V	0 V
V_{SS}	+6.0 V	+1.0 V
V_{DD}	−18 V	−23 V
LOGIC IN		
"Low" Level	+0.2 V	−4.8 V
"High" Level	+5.5 V	+0.5 V

Voltage levels between semiconductor electrodes are normally referenced to one of the electrodes. In MOS, this electrode is the substrate (body or V_{SS}). The voltages can be translated to an equivalent level and referenced to another electrode. In order to measure the 'ON' resistance of the data channel accurately, the data output is at ground potential and all other terminals are changed correspondingly to test worst case conditions.



SPECIAL ORDERING CODE

3708-2D2
Temp. Range: -55°C to +85°C
Input Signal: -5.0to +5.0 Volts

3708-2D3
Temp. Range: -55°C to +85°C
Input Signal: 0 to +5 Volts

3708-5D2
Temp. Range: 0°C to +70°C
Input Signal: -5.0to +5.0 Volts

3708-5D3
Temp. Range: 0°C to +70°C
Input Signal: 0 to +5.0 Volts

ENTERTAINMENT TYPE SELENIUM RECTIFIERS

- Low Cost
- Small Size
- Easy Mounting
- Long Life
- High Voltage

The ITT selenium rectifiers in this catalog cover a wide range of applications. High voltage types lend themselves to compact power supply designs for mobile equipment. The "off-the-line" types are ideal for low-cost half wave and voltage doubler applications in a variety of equipment. Low power applications are especially appropriate for the clip-in types and miniature diodes.

ITT selenium rectifiers are available in several mounting and terminal styles. Miniature diodes and tubular type rectifiers are provided with tinned wire leads and are self-supporting. Open type rectifiers are available in stud and eyelet mounting styles, many can be supplied with clip-in mountings. These rectifiers can be supplied with conventional solder terminals, printed wiring board terminals or plug-in terminals.

ITT's vacuum disposition technique produces selenium rectifiers with extremely long life and minimum change in initial characteristics.

APPLICATIONS

- Horizontal phase discriminator
- Diode matrix assemblies
- Oscilloscopes
- Gate circuits
- Wave shaping networks
- Modulators and demodulators
- Power supplies
- Hi-fi equipment
- DC motor control
- Electric appliances

CLIP TYPE 6H65F
(actual size)

CARTRIDGE TYPE 676H100BCIT
(half size)

OPEN PLATE TYPE 1263B
(actual size)

MINIATURE TYPE 1215
(actual size)

MINIATURE TYPE K1615C
(actual size)

HIGH VOLTAGE CARTRIDGE TYPE SELENIUM RECTIFIERS

CHARACTERISTICS

PIV	Rating (mA)	DIMENSIONS (inches)					ITT Part No.
		Rectifier Dim.		Cell Dia.	Lead Dim.(1)		
		Dia.	Length		Dia.	Length	
4650	2	7/32	3-9/32	1/8	.031(2)	1½	665H100ABI
4650	2	7/32	2-1/8	1/8	.031(2)	1½	665H100ABIT
4650	4	9/32	3-9/32	3/16	.031(2)	1½	676H100ABI
4650	4	9/32	2-1/8	3/16	.031(2)	1½	676H100ABIT
4650	6.5	13/32	3-9/32	9/32	.040(2)	1½	647H100ABI
4650	6.5	13/32	2-1/8	9/32	.040(2)	1½	647H100ABIT
4650	2	15/64	3-1/2	1/8	.031	1½	665H100BCI
4650	2	15/64	2-11/32	1/8	.031	1½	665H100BCIT
4650	4	19/64	3-1/2	3/16	.031	1½	676H100BCI
4650	4	19/64	2-11/32	3/16	.031	1½	676H100BCIT
4650	6.5	3/8	3-1/2	9/32	.031	1½	647H100BCI
4650	6.5	3/8	2-11/32	9/32	.031	1½	647H100BCIT
4650	15	39/64	3-23/32	1/2	.031	1½	629H100BCI
4650	15	39/64	2-9/16	1/2	.031	1½	629H100BCI
4650	25	15/16	3-23/32	3/4	.031	1½	630H100BCI
4650	25	15/16	2-9/16	3/4	.031	1½	630H100BCIT

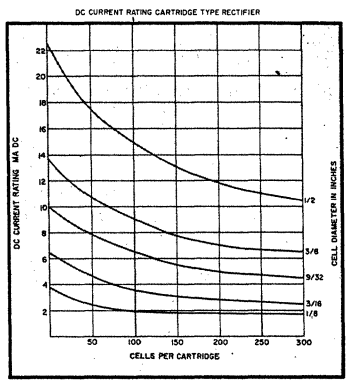
NOTES: 1. Solder type terminals or radial leads also available.
2. Silver plated metal end ferrules.

HOW TO ORDER HIGHER VOLTAGE TYPES

Voltage ratings are available in 46.5 volt increments up to many thousands of volts. Contact ITT Semiconductors for applications assistance.

HOW TO CALCULATE CURRENT RATINGS

Current rating depends upon cell area and the number of cells in series. The curves at the right give the necessary information. The AB series of rectifiers in the characteristics table above have a maximum current rating of 10 mA in a half wave circuit. The BC series has a maximum current rating of 45 mA in a half wave circuit.



OFF-THE-LINE HALF WAVE SELENIUM RECTIFIERS

SPECIFICATIONS

Rated Input Voltage ..... 117 Volts RMS
Maximum Input Voltage ..... 130 Volts RMS
Maximum Inverse Voltage ..... 380 Volts Peak
Maximum Output Current ..... As Listed
Maximum RMS Current ..... 2.7 Times DC Rating
Maximum Peak Current ..... 10 Times DC Rating
Minimum Series Resistance ..... As Listed
Maximum Cell Operating Temperature ..... 85°C

DIMENSIONS

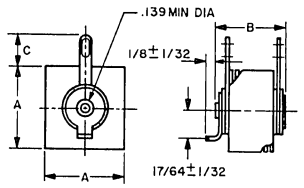


FIGURE 1

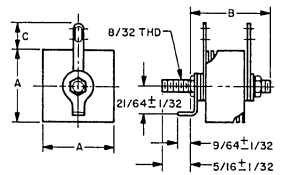


FIGURE 2

CHARACTERISTICS

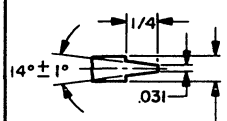
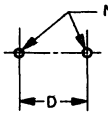
Max. Output (mA) DC	Dimensions (inches) Fig. No.	Cell Size (A)	Mtg Dim. (B) Max.	Term. Hgt (C) Max.	Series Resist. (Min.)	ITT Part No.
10		3/8 Dia. x 11/16 long, with axial wire leads 1-5/16 long			47	1158
15		3/8 Dia. x 11/16 long, with axial wire leads 1-5/16 long			47	5152
20		1/2 Dia. x 11/16 long, with axial wire leads 1-5/16 long			47	1159
30		1/2 Dia. x 11/16 long, with axial wire leads 1-5/16 long			47	5153
65	1	1	9/16	21/64	22	1002A
	1	1	9/16	13/32	22	1444(1)
	1	11/16	23/32	31/64	22	1263A
	1	11/16	21/32	9/16	22	1526(1)
	—	11/16	BKT MTD	31/64	22	1263B
75	1	1	3/4	21/64	22	1003A
	1	1	3/4	13/32	22	1445(1)
	1	11/16	21/32	31/64	22	6H75AE
100	1	1-1/4	3/4	25/64	22	1004A
	1	1	1-1/8	21/64	22	1101A
	1	1	1-1/8	13/32	22	1504(1)
	1	1	3/4	21/64	7.5	6H100AE
150	1	1-1/4	1	25/64	15	1005A
	1	1	1-1/8	21/64	7.5	6H150AE
200	1	1-1/2	1	31/64	4.7	1006A
	2	1	2	21/64	4.7	6H200A
250	1	1-1/2	1-1/8	31/64	4.7	1028A
	1	1-1/4	1-1/4	25/64	4.7	6H250AE
300	2	1-1/2	2-7/32	19/32	4.7	1090A
	1	1-1/4	1-13/32	25/64	4.7	6H300AE
350	2	1-3/4	2-7/32	19/32	4.7	1023A
	2	1-5/8	2-7/32	17/32	4.7	1356A
	2	1-1/4	2	25/64	4.7	6H350A
400	2	1-3/4	2-1/4	19/32	4.7	1277A
	1	1-1/2	1-1/2	31/64	4.7	6H400AE
450	2	2	2-7/32	15/32	4.7	1021A
	2	1-1/2	2-7/32	31/64	3.3	6H450A
500	2	2	2-7/32	15/32	4.7	1179A
	2	1-3/4	1-13/16	19/32	3.3	6H500A
600	2	2	2-1/2	15/32	4.7	1289A
	2	1-3/4	2	19/32	3.3	6H600A
750	2	2	2	15/32	3.3	6H750A

NOTE: Rectifier terminals designed for mounting in a printed circuit board. The "B" dimension listed here is the overall length; see page 4 for mounting information.

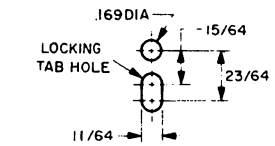
OFF-THE-LINE HALF WAVE SELENIUM RECTIFIERS, continued

MOUNTING DETAILS

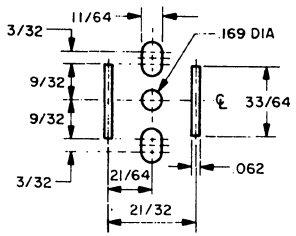
Taper Tip Design . . . for maximum ease of insertion in heavy-gauge printed circuit boards up to ⅛" thick. The tapered terminal may be inserted into round, diamond-shaped, or rectangular holes. Taper design keeps the rectifier plates off the board. As a result, the flow of cooling air through the cells is improved, and extra board area is freed beneath the rectifier for additional printing.

Mounting Detail	Terminal Detail	Rectifier Code No.	Dimension "D"
		1444	5/16
		1445	15/32
		1504	7/8
		1526	13/32

MOUNTING HOLES

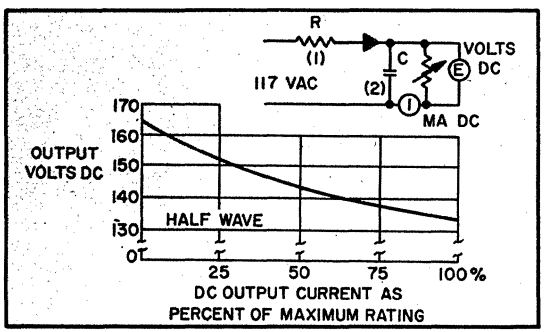


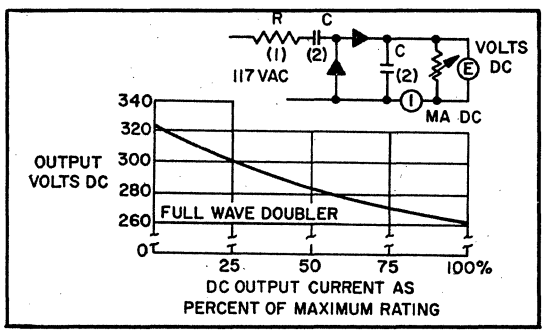
Mounting hole layout for stud and eyelet rectifiers.

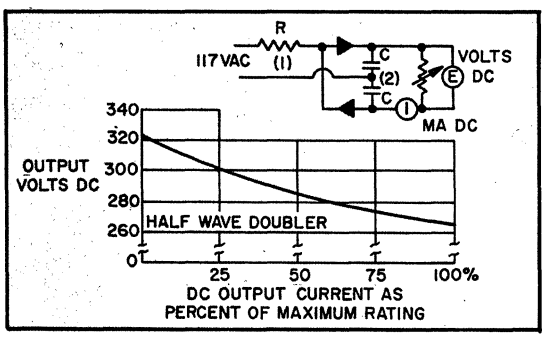


Mounting hole layout for clip mounted rectifiers; will also permit mounting of stud type rectifiers.

CIRCUIT DIAGRAMS and TYPICAL VOLTAGE REGULATION CURVES







NOTES:

1. Minimum series resistance specified in characteristics table.
2. Minimum filter capacitance in MFD to be ½ rectifier rating in milliamperes.

CLIP TYPE SELENIUM RECTIFIERS

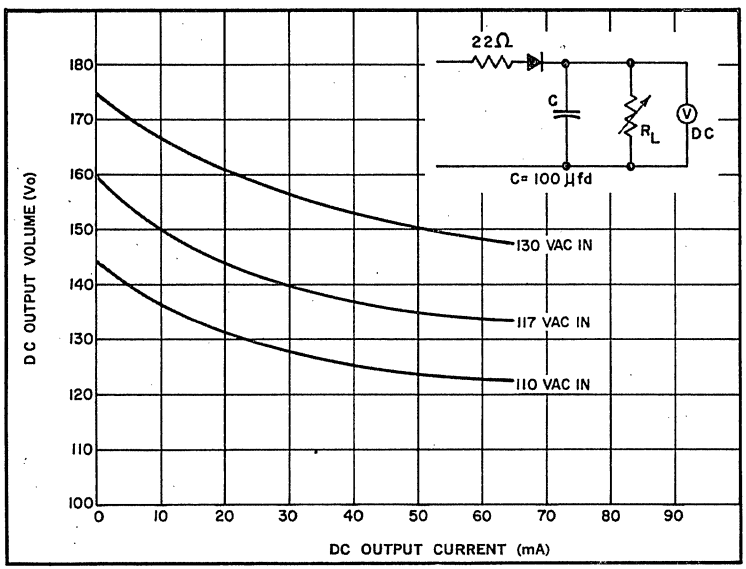
CHARACTERISTICS FOR CAPACITIVE LOAD

Nominal RMS Input Voltage	117
Maximum RMS Input Voltage	130
Maximum Peak Reverse Voltage	380
Maximum Peak Current (mA)	650
Maximum RMS Current (mA)	175
Maximum DC Output Current (mA)	65
Minimum Recommended Series Resistance (Ohms)	22
Maximum Cell Operating Temperature (°C)	85
Maximum Forward Voltage Drop (dc)	10
Dielectric Strength (Volts for 1 Min.)	900
Output Voltage with 117 Volts Input and 100 μf Capacitor and 65 mA dc (Volts)	130

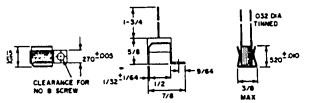
ENVIRONMENTAL CHARACTERISTICS

Humidity—Withstands 120 hours in 95% +RH at 65°C.

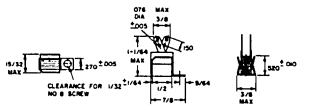
Vibration—Withstands 10 to 55 cps., .060" displacement for 2 hours in each plane.



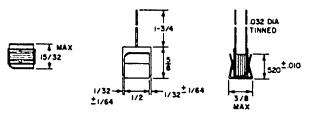
DIMENSIONS



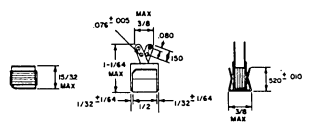
6H65HW



6H65F



6H65FW



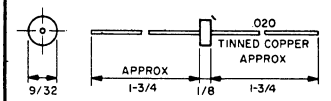
6H65H

MINIATURE SELENIUM DIODES

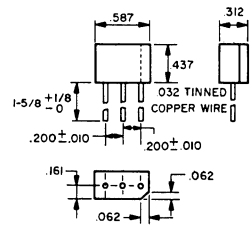
CHARACTERISTICS

	ITT Part No.	
AC APPLICATIONS	1215	K1615AC K1616AC K1617AC
Max. DC forward current (mA)	.25	—
Max. peak forward current (mA)	2.5	—
Max. RMS input volts, resistive load	40	—
Max. peak reverse volts, resistive load	56	—
Max. peak reverse volts, capacitive load	68	—
*Max. shunt capacitance in $\mu\mu$f at 1 kc and −10 volts bias	—	50
Max. shunt capacitance unbalance ($\mu\mu$f)	—	5
Max. shunt capacitance in $\mu\mu$f at 200 kc	22	—
Max. ambient temperature	55°C	85°C
DC APPLICATIONS		
Max pure DC forward current (mA)	.37	.15
Max. continuous reverse volts	30	20
Max. reverse current at 40 volts (μA)	6	—
Max. reverse current at 20 volts (μA)	—	4

DIMENSIONS



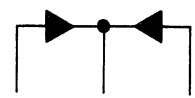
ITT Part Nos.
K1615AC, K1616AC, K1617AC



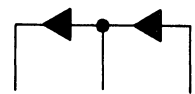
ITT Part No. 1215

ELECTRICAL CONNECTIONS

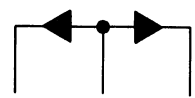
K1615
COMMON
CATHODE



K1616
DOUBLER



K1617
COMMON
ANODE



SELENIUM CONTACT PROTECTOR RECTIFIERS

- AC or DC Applications
- Low Cost
- Easy to Install
- Small Size
- Rugged Construction

These ITT selenium cells have been specifically processed for contact protector applications. Their long life, low leakage current and reliable operation provide a low-cost solution to arcing problems in switched inductive devices.

These circuit protectors prevent arcing by effectively suppressing the voltage surges which normally occur during switching. This eliminates the undesirable by-products of arcing, such as contact pitting and erosion, undesirable electrical noise, false triggering of adjacent control circuits or possible insulation breakdown.

ITT selenium cells may be used in a back-to-back arrangement on devices breaking either AC or DC circuits. In AC applications, each arm normally contains the same number of cells; for DC use, a different number of cells is generally specified for each arm.

TYPICAL APPLICATIONS

- Relays
- Stepping Switches
- Electromagnets
- Solenoids
- Small Motors
- Electric Clutches
- Telephone Switching Equipment
- Automobile Clocks & Horns
- Telemetering Equipment
- Magnetic Chucks
- Thermostats
- Electric Brakes
- Solenoid Valves
- Computers

ORDERING INFORMATION

Explanation of part number codes

8A4 P S 1

- 1 — No. of cells in position "A"
- S — "S" indicates DC suppressor
- A — "A" indicates AC suppressor
- P — "P" indicates paper tube
- H — "H" indicates hermetic seal

102 S 2 E X 1

- 1 — No. of cells in position "B"
- X — Finish
- 2 — No. of cells in position "A"
- S — "S" indicates DC suppressor
- A — "A" indicates AC suppressor

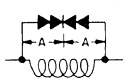


FIG. A

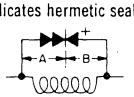


FIG. B

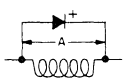


FIG. C

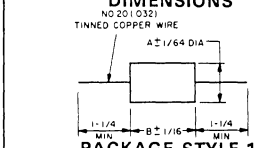
A=BLOCKING SECTION
B=SUPPRESSOR SECTION

Special finishes

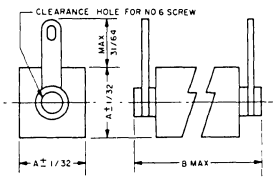
Package style 1 is supplied in a paper tube or in a hermetically sealed can which meets MIL specifications for environmental exposure. Package styles 2, 3 and 4 are supplied with a commercial protective finish. To order special finishes replace the **"X"** in the part number with letters as follows:

"Y" for humidity and salt spray protection
"W" for heavy duty industrial protection
"YF" for humidity, salt spray and fungus protection

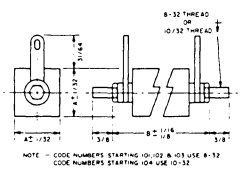
DIMENSIONS



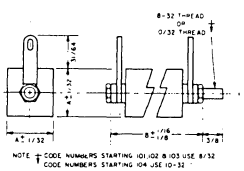
PACKAGE STYLE 1



PACKAGE STYLE 2



PACKAGE STYLE 3



PACKAGE STYLE 4

CHARACTERISTICS

DC APPLICATIONS — 10 BREAKS / SECOND MAX

DC Voltage Range	Max. DC Coil Current mA	Coil Current For 300V Max. Rise mA	ITT Part No.	Package Style	Dimensions A	Dimensions B	ITT Part No.	Package Style	Dimensions A	Dimensions B
0-30	500		8A1PS0	1	25/64	5/8	8A1HS0*	1	1/2	29/32
	1000		15A1PS0	1	1/2	5/8	15A1HS0*	1	9/16	29/32
0-22	1750		101S1EX0	2	11/16	3/8	101S1AX0	4	11/16	9/16
	4700		102S1EX0	2	1	3/8	102S1AX0	4	1	9/16
	9000		103S1EX0	2	1-1/4	11/32	103S1AX0	4	1-1/4	5/8
	14000		104S1EX0	2	1-17/32	11/32	104S1AX0	4	1-17/32	11/16
31-60	500		8A2PS0	1	25/64	5/8	8A2HS0*	1	1/2	29/32
	1000		15A2PS0	1	1/2	5/8	15A2HS0*	1	9/16	29/32
23-44	1750		101S2EX0	2	11/16	1/2	101S2AX0	4	11/16	11/16
	4700		102S2EX0	2	1	1/2	102S2AX0	4	1	11/16
	9000		103S2EX0	2	1-1/4	1/2	103S2AX0	4	1-1/4	11/16
	14000		104S2EX0	2	1-17/32	1/2	104S2AX0	4	1-17/32	13/16
61-90	500		8A3PS0	1	25/64	5/8	8A3HS0*	1	1/2	29/32
	1000		15A3PS0	1	1/2	5/8	15A3HS0*	1	9/16	29/32
45-66	1750		101S3EX0	2	11/16	9/16	101S3AX0	4	11/16	11/16
	4700		102S3EX0	2	1	5/8	102S3AX0	4	1	27/32
	9000		103S3EX0	2	1-1/4	5/8	103S3AX0	4	1-1/4	13/16
	14000		104S3EX0	2	1-17/32	5/8	104S3AX0	4	1-17/32	31/32
91-120	500		8A4PS0	1	25/64	3/4	8A4HS0*	1	1/2	1-1/32
	1000		15A4PS0	1	1/2	3/4	15A4HS0*	1	9/16	1-1/32
67-88	1750		101S4EX0	2	11/16	5/8	101S4AX0	4	11/16	13/16
	4700		102S4EX0	2	1	11/16	102S4AX0	4	1	7/8
	9000		103S4EX0	2	1-1/4	3/4	103S4AX0	4	1-1/4	15/16
	14000	mA FOR 300 VOLT RISE EXCEEDS MAX. CURRENT RATING	104S4EX0	2	1-17/32	23/32	104S4AX0	4	1-17/32	1
121-150	500		8A5PS0	1	25/64	3/4	8A5HS0*	1	1/2	1-1/32
	1000		15A5PS0	1	1/2	5/8	15A5HS0*	1	9/16	1-1/32
89-110	1750		101S5EX0	2	11/16	3/4	101S5AX0	4	11/16	1
	4700		102S5EX0	2	1	7/8	102S5AX0	4	1	1-1/16
	9000		103S5EX0	2	1-1/4	1	103S5AX0	4	1-1/4	13/32
	14000		104S5EX0	2	1-17/32	1	104S5AX0	4	1-17/32	1-3/16
151-180	500		8A6PS0	1	25/64	3/4	8A6HS0*	1	1/2	1-1/32
	1000		15A6PS0	1	1/2	15/16	15A6HS0*	1	9/16	1-1/32
111-132	1750		101S6EX0	2	11/16	1	101S6AX0	4	11/16	1-1/16
	4700		102S6EX0	2	1	1	102S6AX0	4	1	1-1/8
	9000		103S6EX0	2	1-1/4	1	103S6AX0	4	1-1/4	1-1/4
	14000		104S6EX0	2	1-17/32	1-1/8	103S6AX0	4	1-17/32	1-5/16
181-210	500		8A7PS0	1	25/64	15/16	8A7HS0*	1	1/2	1-7/32
	1000		15A7PS0	1	1/2	13/16	15A7HS0*	1	9/16	1-7/32
133-154	1750		101S7EX0	2	11/16	1	101S7AX0	4	11/16	1-1/8
	4700		102S7EX0	2	1	1	102S7AX0	4	1	1-1/4
	9000		103S7EX0	2	1-1/4	1-1/2	103S7AX0	4	1-1/4	1-3/8
	14000		104S7EX0	2	1-17/32	1-1/8	104S7AX0	4	1-17/32	1-7/16
211-240	500		8A8PS0	1	25/64	13/16	8A8HS0*	1	1/2	1-7/32
	1000		15A8PS0	1	1/2	13/16	15A8HS0*	1	9/16	1-7/32
155-176	1750		101S8EX0	2	11/16	1-1/8	101S8AX0	4	11/16	1-3/16
	4700		102S8EX0	2	1	1-5/32	102S8AX0	4	1	1-5/16
	9000		103S8EX0	2	1-1/4	1-1/4	103S8AX0	4	1-1/4	1-7/16
	14000		104S8EX0	2	1-17/32	1-1/4	104S8AX0	4	1-17/32	1-1/2
241-270	500		8A9PS0	1	25/64	15/16	8A9HS0*	1	1/2	1-7/32
	1000		15A9PS0	1	1/2	15/16	15A9HS0*	1	9/16	1-7/32
177-198	1750		101S9EX0	2	11/16	1-1/8	101S9AX0	4	11/16	1-1/4
	4700		102S9EX0	2	1	1-1/4	102S9AX0	4	1	1-15/32
	9000		103S9EX0	2	1-1/4	1-3/8	103S9AX0	4	1-1/4	1-9/16
	14000		104S9EX0	2	1-17/32	1-3/8	103S9AX0	4	1-17/32	1-3/8
271-300	500	375	8A10PS0	1	25/64	15/16	8A10HS0*	1	1/2	1-7/32
	1000	750	15A10PS0	1	1/2	15/16	15A10HS0*	1	9/16	1-7/32
199-220	1750	1300	101S10EX0	2	11/16	1-1/4	101S10AX0	4	11/16	1-5/16
	4700	3500	102S10EX0	2	1	1-3/8	102S10AX0	4	1	1-1/2
	9000	6750	103S10EX0	2	1-1/4	1-1/2	103S10AX0	4	1-1/4	1-5/8
	14000	11000	104S10EX0	2	1-17/32	1-1/2	104S10AX0	4	1-17/32	1-11/16
301-330	500	275	8A11PS0	1	25/64	1-1/8	8A11HS0*	1	1/2	1-13/32
	1000	550	15A11PS0	1	1/2	1-1/8	15A11HS0* *	1	9/16	1-13/32
221-242	1750	950					101S11AX0	3	11/16	1-5/8
	4700	2600					102S11AX0	3	1	1-13/16
	9000	5000					103S11AX0	3	1-1/4	2
	14000	7750					104S11AX0	3	1-17/32	2-1/16
331-360	500	125	8A12PS0	1	25/64	1-1/8	8A12HS0*	1	1/2	1-13/32
	1000	250	15A12PS0	1	1/2	1-1/8	16A12HS0*	1	9/16	1-13/32
243-264	1750	450					101S12AX0	3	11/16	1-9/16
	4700	1200					102S12AX0	3	1	1-13/16
	9000	2250					103S12AX0	4	1-1/4	2
	14000	3500					104S12AX0	3	1-17/32	2-1/16

NOTE: Hermetically sealed tubular construction to meet MIL specifications for environmental exposure.

DC APPLICATIONS — 40 BREAKS / SECOND MAX

DC Voltage Range	Max. DC Coil Current mA	Coil Current For 300V Max. Rise mA	ITT Part No.	Package Style	Dimensions A	Dimensions B	ITT Part No.	Package Style	Dimensions A	Dimensions B
0-30	250	mA FOR 300 VOLT RISE EXCEEDS MAX. CURRENT RATING	8A1PS1	1	25/64	5/8	8A1HS1*	1	1/2	29/32
	600		15A1PS1	1	1/2	5/8	15A1HS1*	1	9/16	29/32
0-22	850		101S1EX1	2	11/16	15/32	101S1AX1	4	11/16	5/8
0-22	2250		102S1EX1	2	1	15/32	102S1AX1	4	1	25/32
	4300		103S1EX1	2	1-1/4	17/32	103S1AX1	4	1-1/4	3/4
	6600		104S1EX1	2	1-17/32	17/32	104S1AX1	4	1-17/32	13/16
31-60	250		8A2PS1	1	25/64	5/8	8A2HS1*	1	1/2	29/32
	600		15A2PS1	1	1/2	5/8	15A2HS1*	1	9/16	29/32
23-44	850		101S2EX1	2	11/16	9/16	101S2AX1	4	11/16	1-3/16
	2250		102S2EX1	2	1	9/16	102S2AX1	4	1	29/32
	4300		103S2EX1	2	1-1/4	17/32	103S2AX1	4	1-1/4	3/4
	6600		104S2EX1	2	1-17/32	19/32	104S2AX1	4	1-17/32	7-8
61-90	250		8A3PS1	1	25/64	3/4	8A3HS1*	1	1/2	1-1/32
	600		15A3PS1	1	1/2	3/4	15A3HS1*	1	9/16	1-1/32
45-66	850		101S3EX1	2	11/16	17/32	101S3AX1	4	11/16	1
	2250		102S3EX1	2	1	9/16	102S3AX1	4	1	1-1/32
	4300		103S3EX1	2	1-1/4	23/32	103S3AX1	4	1-1/4	25/32
	6600		104S3EX1	2	1-17/32	23/32	104S3AX1	4	1-17/32	1
91-120	250		8A4PS1	1	25/64	3/4	8A4HS1*	1	1/2	1-1/32
	600		15A4PS1	1	1/2	3/4	15A4HS1*	1	9/16	1-1/32
67-88	850		101S4EX1	2	11/16	21/32	101S4AX1	4	11/16	1
	2250		102S4EX1	2	1	1	102S4AX1	4	1	1
	4300		103S4EX1	2	1-1/4	1	103S4AX1	4	1-1/4	1-1/16
	6600		104S4EX1	2	1-17/32	3/4	104S4AX1	4	1-17/32	1-1/8
121-150	250		8A5PS1	1	25/64	3/4	8A5HS1*	1	1/2	1-1/32
	600		15A5PS1	1	1/2	3/4	15A5HS1*	1	9/16	1-1/32
89-110	850		101S5EX1	2	11/16	13/16	101S5AX1	4	11/16	1-1/16
	2250		102S5EX1	2	1	7/8	102S5AX1	4	1	1-1/8
	4300		103S5EX1	2	1-1/4	1-1/8	103S5AX1	4	1-1/4	1-1/4
	6600		104S5EX1	2	1-17/32	1-1/8	104S5AX1	4	1-17/32	1-3/8
151-180	250		8A6PS1	1	25/64	15/16	8A6HS1*	1	1/2	1-7/32
	600		15A6PS1	1	1/2	15/16	15A6HS1*	1	9/16	1-7/32
111-132	850		101S6EX1	2	11/16	1	101S6AX1	4	11/16	1-1/8
	2250		102S6EX1	2	1	1	102S6AX1	4	1	1-1/4
	4300		103S6EX1	2	1-1/4	1-1/8	103S6AX1	4	1-1/4	1-3/8
	6600		104S6EX1	2	1-17/32	1-1/8	104S6AX1	4	1-17/32	1-7/16

DC Voltage Range	Max. DC Coil Current mA	Coil Current For 300V Max. Rise mA	ITT Part No.	Package Style	Dimensions A	Dimensions B	ITT Part No.	Package Style	Dimensions A	Dimensions B
181-210	250	mA FOR 300 VOLT RISE EXCEEDS MAX. CURRENT RATING	8A7PS1	1	25/64	15/16	8A7HS1*	1	1/2	1-7/32
	600		15A7PS1	1	1/2	15/16	15A7HS1*	1	9/16	1-7/32
133-154	850		101S7EX1	2	11/16	1-1/8	101S7AX1	4	11/16	1-3/16
	2250		102S7EX1	2	1	31/32	102S7AX1	4	1	1-5/16
	4300		103S7EX1	2	1-1/4	1-1/4	103S7AX1	4	1-1/4	1-7/16
	6600		104S7EX1	2	1-17/32	1-1/4	104S7AX1	4	1-17/32	1-9/16
211-240	250		8A8PS1	1	25/64	15/16	8A8HS1*	1	1/2	1-7/32
	600		15A8PS1	1	1/2	15/16	15A8HS1*	1	9/16	1-7/32
155-176	850		101S8EX1	2	11/16	1-1/8	101S8AX1	4	11/16	1-1/4
	2250		102S8EX1	2	1	1-1/4	102S8AX1	4	1	1-7/16
	4300		103S8EX1	2	1-1/4	1-3/8	103S8AX1	4	1-1/4	1-9/16
	6600		104S8EX1	2	1-17/32	1-1/4	104S8AX1	4	1-17/32	1-5/8
241-270	250	120	8A9PS1	1	25/64	15/16	8A9HS1*	1	1/2	1-7/32
	600	300	15A9PS1	1	1/2	15/16	15A9HS1*	1	9/16	1-7/32
177-198	850	500	101S9EX1	2	11/16	1-1/4	101S9AX1	4	11/16	1-15/16
	2250	1350	102S9EX1	2	1	1-3/8	102S9AX1	4	1	1-1/2
	4300	2600	103S9EX1	2	1-1/4	1-1/2	103S9AX1	4	1-1/4	1-5/8
	6600	4000	104S9EX1	2	1-17/32	1-1/2	104S9AX1	4	1-17/32	1-3/4
271-300	250	100	8A10PS1	1	25/64	1-1/8	8A10HS1*	1	1/2	1-13/32
	600	250	15A10PS1	1	1/2	1-1/8	15A10HS1*	1	9/16	1-13/32
199-220	850	450					101S10AX1	3	11/16	1-5/8
	2250	1125					102S10AX1	3	1	1-13/16
	4300	4150					103S10AX1	3	1-1/4	1-7/8
	6600	3300					104S10AX1	3	1-17/32	2-1/16
301-330	250	50	8A11PS1	1	25/64	1-1/8	8A11HS1*	1	1/2	1-13/32
	600	125	15A11PS1	1	1/2	1-1/8	15A11HS1*	1	9/16	1-13/32
221-242	850	210					101S11AX1	3	11/16	1-5/8
	2250	560					102S11AX1	3	1	1-7/8
	4300	1100					103S11AX1	3	1-1/4	2
	6600	1650					104S11AX1	3	1-17/32	2-1/16
331-360	250	10	8A12PS1	1	25/64	1-1/8	8A12HSA*	1	1/2	1-13/32
	600	25	15A12PS1	1	1/2	1-1/16	15A12HS1*	1	9/16	1-13/32
243-264	850	45					101S12AX1	3	11/16	1-5/8
	2250	110					102S12AX1	3	1	1-7/8
	4300	215					103S12AX1	3	1-1/4	2-1/16
	6600	330					104S12AX1	3	1-17/32	2-3/16

AC APPLICATIONS

DC Voltage Range	Max. DC Coil Current mA	Coil Current For 300V Max. Rise mA	ITT Part No.	Package Style	Dimensions A	Dimensions B	ITT Part No.	Package Style	Dimensions A	Dimensions B
0-26	200	mA FOR 300 VOLT RISE EXCEEDS MAX. CURRENT RATING	8A1PA1	1	25/64	5/8	8A1HA1*	1	1/2	29/32
	400		15A1PA1	1	1/2	5/8	15A1HA1*	1	9/16	29/32
	600		101A1EX1	2	11/16	15/32	101A1AX1	4	11/16	11/16
	1600		102A1EX1	2	1	15/32	102A1AX1	4	1	25/32
	3000		103A1EX1	2	1-1/4	1/2	103A1AX1	4	1-1/4	3/4
	4700		104A1EX1	2	1-17/32	17/32	104A1AX1	4	1-17/32	13/16
27-52	200	200	8A2PA2	1	25/64	5/8	8A2HA2*	1	1/2	1-1/32
	400	400	15A2PA2	1	1/2	3/4	15A2HA2*	1	9/16	1-1/32
	600	600	101A2EX2	2	11/16	1/2	101A2AX2	4	11/16	23/32
	1600	1600	102A2EX2	2	1	11/16	102A2AX2	4	1	1-1/32
	3000	3000	103A2EX2	2	1-1/4	11/16	103A2AX2	4	1-1/4	7/8
	4700	4700	104A2EX2	2	1-17/32	23/32	104A2AX2	4	1-17/32	1
53-78	200	60	8A3PA3	1	25/64	3/4	8A3HA3*	1	1/2	1-1/32
	400	140	15A3PA3	1	1/2	3/4	15A3HA3*	1	9/16	1-1/32
	600	250	101A3EX3	2	11/16	13/16	101A3AX3	4	11/16	27/32
	1600	650	102A3EX3	2	1	7/8	102A3AX3	3	1	1-7/16
	3000	1200	103A3EX3	2	1-1/4	1-3/16	103A3AX3	4	1-1/4	1-1/4
	4700	2000	104A3EX3	2	1-17/32	1	104A3AX3	4	1-17/32	1-5/16

DC Voltage Range	Max. DC Coil Current mA	Coil Current For 300V Max. Rise mA	ITT Part No.	Package Style	Dimensions A	Dimensions B	ITT Part No.	Package Style	Dimensions A	Dimensions B
79-104	200	15	8A4PA4	1	25/64	15/16	8A4HA4*	1	1/2	1-7/32
	400	35	15A4PA4	1	1/2	15/16	15A4HA4*	1	9/16	1-7/32
	600	60	101A4EX4	2	11/16	29/32	101A4AX4	3	11/16	1-3/16
	1600	160	102A4EX4	2	1	31/32	102A4AX4	4	1	29/32
	3000	300	103A4EX4	2	1-1/4	1-5/32	103A4AX4	4	1-1/4	1-1/4
	4700	470	104A4EX4	2	1-17/32	1-5/32	104A4AX4	4	1-17/32	1-1/2
105-130	200	10	8A5PA5	1	25/64	15/16	8A5HA5*	1	1/2	1-7/32
	400	20	15A5PA5	1	1/2	15/16	15A5HA5*	1	9/16	1-7/32
	600	30	101A5EX5	2	11/16	1-1/8	101A5AX5	4	11/16	1-1/8
	1600	80	102A5EX5	2	1	1-11/32	102A5AX5	3	1	1-5/8
	3000	150	103A5EX5	2	1-1/4	1-1/4	103A5AX5	4	1-1/4	1-7/16
	4700	250	104A5EX5	2	1-17/32	1-13/32	104A5AX5	3	1-17/32	1-7/8

NOTE: Hermetically sealed tubular construction to meet MIL specifications for environmental exposure.

CAUSE OF CONTACT ARCING

Consider the circuit shown in **Figure 1.** Close the circuit contacts S_1 and the current flow as indicated by the ammeter M_1 builds up to 400 mA. The flow of current has set up a magnetic field through the core. Electrical energy has been stored in the magnetic field by the current, analogous to the mechanical energy stored in a spring by compression.

Now open the contacts S_1 thus breaking the steady flow of current. Just as the compressed spring will start to release its stored mechanical energy, the magnetic field starts to collapse, releasing its stored energy. While the magnetic field is collapsing it induces a voltage in the coil that acts to maintain the current through the coil in the same direction as the original current which built up the field. The magnitude of this induced voltage is equal to the product of the coil current, and the coil and circuit resistance; and it can attain very high values since the circuit resistance approaches infinity with the switch contacts open.

Theoretically, when the flow of current is suddenly stopped by the opening of S_1, the voltage that appears across the coil could go up to infinity. Approximately 300 volts is required to produce arcing across contacts in free air. Since air is not a perfect insulator, the instant that S_1 is opened and the high induced voltage appears across the contacts, an arc occurs. In typical applications, air breakdown across the contacts will limit the voltage rise to the region of 300 to 1,000 volts in an average 24-volt coil circuit. **See Figure 2.**

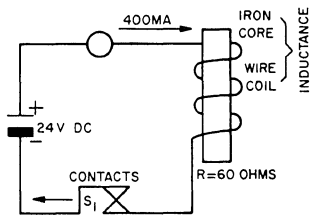


FIG. 1

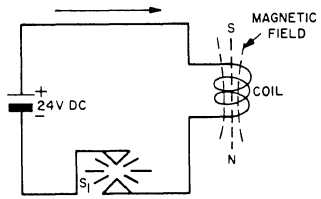


FIG. 2

HOW ITT SELENIUM CONTACT PROTECTORS WORK

Half-wave configuration for DC applications

Consider the circuit of **Figure 3,** showing contact protector cell A connected across the coil terminals. While contacts S_1 are held closed a current of 400 milliamperes flows through the coil, but no part of the coil current flows through the contact protector. When S_1 is opened coil current flows in the low-resistance direction of the contact protector, thus dissipating the energy stored in the coil through the resistance of the coil and contact protector. As the resistance of the contact protector is very low, usually a fraction of the coil resistance, the voltage across the contacts rises only slightly, to a few volts above battery voltage.

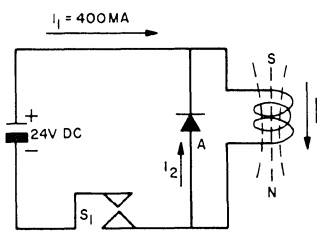


FIG. 3

Half-wave configuration, continued

In the circuit shown in **Figure 4,** cell B has been added in such a direction as to oppose the discharge current I_2. A semiconductor cell has the unique characteristic of exhibiting decreasing resistance with increasing voltage in the blocking direction.

At the instant switch S_1 is opened, the induced voltage rises to approximately 150 volts, due to the blocking action of cell B. This induced voltage is indicated in **Figure 4** and appears as a reverse voltage across cell B, i.e., the high-resistance direction.

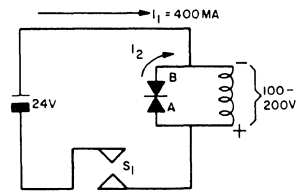


FIG. 4

Figure 5 shows the change in reverse resistance with application of reverse voltage to a typical semiconductor contact-protector cell. At the working voltage of 24 volts, the reverse resistance is approximately 1 megohm. When S_1 is opened, the voltage across the coil builds up to approximately −200 volts. At this voltage the reverse resistance of cell B will be less than 500 ohms. Much of the stored energy is dissipated in this low-resistance region of the cell characteristic.

As the energy is dissipated and the current decreases, the induced voltage also decreases. The remainder of the stored energy is dissipated in a higher-resistance region than initially. For example, as the induced voltage decays to −25 volts, the cell resistance rises to approximately one megohm.

Thus the effect of the nonlinear resistance of cell B is to provide, at the instant of switching, a path of relatively low resistance to prevent the induced voltage from rising to a value which will cause arcing. As the stored energy is dissipated the low resistance increases, due to the nature of the cell characteristics, and provides a damping effect on the discharge current. The result is to reduce the coil release time as compared to the action of the half-wave-type contact protector.

Figure 6. Oscillograph trace voltage across a set of contacts breaking the circuit of a 48-volt telephone relay, without contact protection. Sparking begins at 300 volts (see oscillations), continues as contacts are separated and rises to a voltage peak at 500 volts. Voltage decay is exponential.

Figure 7. Oscillograph trace of voltage across same set of contacts, protected by ITT half-wave semiconductor contact protector.

Figure 8. Oscillograph trace of voltage across same set of contacts, protected by ITT back-to-back semiconductor contact protector.

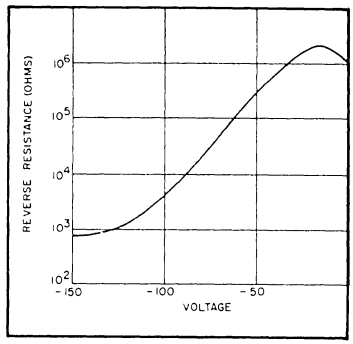


FIG. 5

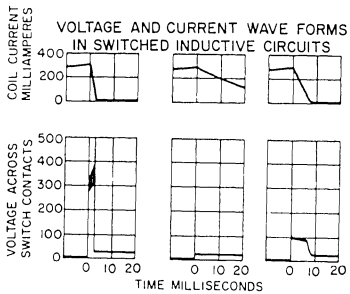


FIG. 6 FIG. 7 FIG. 8

5

Back-to-back configuration for AC applications

The back-to-back configuration is readily adapted to use in AC circuits by providing the same number of cells in each arm of the device. The number of cells in series per arm will depend on the applied AC voltage. The requirement for the same number of cells in each arm arises from the fact that both arms alternately are required to block the input voltage. This arrangement differs from the DC back-to-back configuration in which one arm has sufficient cells to block the battery voltage and the other has only one or two cells to provide the surge suppression.

Factors relating to the opening of inductive circuits

It can be shown mathematically that the time required for the coil current to drop to zero, after the switch contacts have opened, is inversely proportional to the sum of the coil resistance and protector resistance. Also, the magnitude of the voltage induced in the coil at the instant of switching is directly proportional to the sum of these resistances.

When the circuit energizing an inductance is opened the polarity of the voltage across the coil is reversed and is indicated by the equation $E = -L\frac{di}{dt}$

After the circuit opens, and assuming no arcing occurs, the time for the current to fall to a percentage of its initial value is given by the following equation:

$$t = \frac{-L}{R_L + r} \log \frac{i}{EI}$$

When R = Coil resistance
r = Forward resistance of rectifier
L = Inductance of coil
t = Time for current to decrease to i
i = Current at time t
I = Steady-state current through the coil
E = Supply voltage

The voltage induced across the coil is expressed by the equation

$$V = -L\frac{di}{dt} = (R_L + r)\, I_E - \frac{R_L + r}{L}t$$

The maximum value of voltage V occurs when t = O V max. = $I(R+r) = E+Ir$

In an inductive circuit with unprotected switch contacts, the coil current decays through a path that includes the widening air gap between the moving contacts. The high resistance of this gap results in a very short current decay time. However, the voltage induced in the coil at the instant of switching must reach a value high enough to force the current across the air gap. This leads to the electrical breakdown of the air gap with attendant arcing, contact damage and electrical noise.

In the half-wave configuration the resistance of the protector is low when it is acting as a suppressor, since the coil current flows in the low-resistance forward direction of the device. The forward resistance of the half-wave suppressor will usually be only a small fraction of the coil resistance and, for practical purposes, may be regarded as a short circuit around the coil. The low value of protector resistance prevents the induced voltage from rising more than a volt or two over the battery voltage, and increases the current decay time compared to the decay time of a coil with unprotected contacts.

In the back-to-back configuration the reverse resistance of the protector is inversely proportional to the induced voltage. This resistance will be the smallest at the instant of switching and will increase in value as the current decreases. This nonlinear resistance characteristic causes the induced voltage to rise to a value higher than it would reach in a circuit using the half-wave configuration, but it prevents the induced voltage from attaining the contact-damaging values existing in a circuit with unprotected contacts. Although the current decay time is increased somewhat compared to the decay time of a coil with unprotected contacts, it is very appreciably shorter than the decay time of a circuit using the half-wave configuration.

APPLICATION NOTES

Voltage Range

The words "voltage range" are used because the maximum voltage rating increases in discrete steps, according to the number of blocking cells in series. Each protector has a maximum permissible voltage rating which is the low-voltage end of the range for the next higher voltage group.

Max. Coil Current – mA

The maximum permissible coil current is based on the thermal dissipation characteristics of the contact protector when operated at maximum coil voltage and repetition rate.

Coil Current for 300-V Max. Rise – mA

At the instant of switching, the current through the protector is the same as the coil current, and the induced voltage at the coil terminals will rise to the value required to drive this current through the protector. This voltage will add to the supply voltage and appear across the contacts. Sparking at the contacts will be minimized if the sum of these two voltages does not exceed 300 volts, and this requirement is met if the induced voltage is no greater than the difference between 300 and the supply voltage. This condition is achieved by reducing, for a given cell size, the permissible coil current as the supply voltage increases. Thus, it will be observed that the coil current for 300-volt rise will be less than the maximum coil current for many of the higher-voltage units. Conversely, the coil current for 300-volt rise is so great that it exceeds the maximum coil current for the low-voltage units. These protectors carry the note in the rating table "MA for 300-Volt Rise Exceeds Max. Current Rating"; this means that operation at the listed maximum coil current will give a voltage rise of less than 300 volts at the contacts.

The current values listed in the column "Coil Current for 300-V Max. Rise" are representative values, based on the observation of typical relays and solenoids. The specific value of current that will limit the voltage at the contacts to 300 volts is a function of the coil design, the size of the coil, the number of turns of wire, etc., and it is possible for a contact protector to furnish adequate spark suppression when used with coils carrying currents greater than those listed; but the maximum current rating should not be exceeded. For this reason, it is wise to observe the action and efficiency of the protector before freezing a design. Samples and engineering assistance are available upon written request to the Engineering Department.

In selecting a suitable Contact Protector from the list in this data sheet, it should be noted:

Ratings are based upon operation in typical inductive circuits at temperatures of 50°C or lower. Current ratings given in the column headed "Coil Steady State Current for 300 volt max. rise" represent the rating of the protector to limit the voltage rise across the contacts to approximately 300 volts. This rating may be exceeded if a rise in excess of 300 volts is permissible, but the maximum peak current rating should not be exceeded. The voltage rating should not be exceeded under any circumstances.

Fast Contact Action

Rate of operation of contacts in the range 10 to 40 breaks per second. The back-to-back arrangement of the ITT Contact Protector provides adequate arc suppression with a negligible effect upon the release time of the relay. The protectors are fated for applications where the rate of operation of the contacts is in the range of 10 to 40 breaks per second. ITT should be consulted for recommendations if the rate of operation exceeds 40 breaks per second.

TRANSIENT VOLTAGE SUPPRESSOR RECTIFIERS

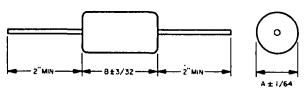
- **AC Input or DC Applications**
- **Improve Equipment Reliability**
- **Reduce Equipment Cost**

ITT transient voltage suppressors eliminate one of the major causes of failure of semiconductor rectifiers by instantaneously short-circuiting transient voltages in excess of the ratings of the rectifiers. They permit the circuit designer to use rectifiers with lower PIV ratings, thereby reducing equipment cost. These specially processed selenium cells have very sharp "zener" breakdown characteristics when operated in the reverse direction. Since the reverse characteristic is used instead of the forward characteristic, aging has very little effect on the resistance and suppressing voltage level of the protector. The small effects of aging and temperature variations have been taken into consideration in the volt-ampere curves and tabulated characteristics.

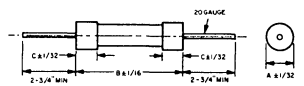
In inductive circuits using mechanical switches, these suppressors can be used to eliminate pitting of the switch contacts by absorbing the high peak voltages generated when the switch is opened. ITT contact protector selenium rectifiers can also be used in this application.

Transient voltage suppressors can be mounted by eyelets or studs in stack types and by clips or pigtail leads in tubular types. Stack types are supplied with a standard industrial finish or with a moisture resistant finish for protection against salt spray and humidity.

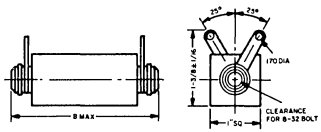
DIMENSIONS



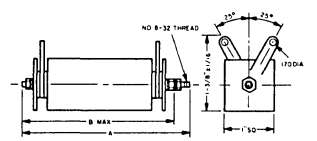
PAPER TUBE TYPE



PHENOLIC TUBE TYPE



EYELET TYPE



STUD TYPE

RATINGS

CHARACTERISTICS	8A SERIES	25A SERIES	102 SERIES	UNITS
Steady State RMS Volts/Cell	30	30	25	Volts
Peak Volts/Cell	42.4	42.4	35	Volts
DC Volts/Cell	20	20	20	Volts
Stack RMS Volts	30-600	36-600	25-500	Volts
Stack DC Volts	20-400	20-400	20-320	Volts
Steady State Leakage Current (max.)	0.8	1.2	12	mA
Single Pulse Current (4 milliseconds) (max.)	0.75	2	8	Amps
Recurrent Pulse Current (1 millisecond @ 60 cps) (max.)	0.25	0.75	3	Amps
Ambient Temperature	—20 to +100	—20 to +100	—20 to +100	°C
Cell Operating Temperature (max.)	130	130	130	°C
Construction	Tubular	Tubular	Stud or Eyelet	

ELECTRICAL AND MECHANICAL CHARACTERISTICS – AC INPUT TYPES

PAPER TUBE TYPES

MAX. RMS INPUT VOLTS	MAX. PEAK INPUT VOLTS	MAX. ZENER VOLTS[1]	DIMENSIONS DIA. (A)	DIMENSIONS LENGTH (B)	ITT PART NO.
30	42	104	3/8	27/32	8A1PG1
60	85	208	3/8	27/32	8A2PG2
90	127	312	3/8	27/32	8A3PG3
120	170	416	3/8	27/32	8A4PG4
150	212	519	3/8	27/32	8A5PG5
180	254	623	3/8	1 3/32	8A6PG6
210	297	727	3/8	1 3/32	8A7PG7
240	339	831	3/8	1 3/32	8A8PG8
270	382	934	3/8	1 3/32	8A9PG9
300	424	1039	3/8	1 3/32	8A10PG10
330	467	1143	3/8	1 21/64	8A11PG11
360	509	1247	3/8	1 21/64	8A12PG12
390	551	1350	3/8	1 21/64	8A13PG13
420	594	1454	3/8	1 21/64	8A14PG14
450	636	1558	3/8	1 21/64	8A15PG15
480	679	1663	3/8	1 37/64	8A16PG16
510	721	1766	3/8	1 37/64	8A17PG17
540	764	1870	3/8	1 37/64	8A18PG18
570	806	1974	3/8	1 37/64	8A19PG19
600	848	2078	3/8	1 37/64	8A20PG20

MAX. RMS INPUT VOLTS	MAX. PEAK INPUT VOLTS	MAX. ZENER VOLTS[2]	DIMENSIONS DIA. (A)	DIMENSIONS LENGTH (B)	ITT PART NO.
30	42	87	37/64	1 1/64	25A1PG1
60	85	177	37/64	1 1/64	25A2PG2
90	127	266	37/64	1 1/64	25A3PG3
120	170	354	37/64	1 1/64	25A4PG4
150	212	443	37/64	1 1/64	25A5PG5
180	254	532	37/64	1 1/4	25A6PG6
210	297	620	37/54	1 1/4	25A7PG7
240	339	709	37/64	1 1/4	25A8PG8
270	382	798	37/64	1 1/4	25A9PG9
300	424	886	37/64	1 1/4	25A10PG10
330	467	975	37/64	1 1/2	25A11PG11
360	509	1063	37/64	1 1/2	25A12PG12
390	551	1152	37/64	1 1/2	25A13PG13
420	594	1241	37/64	1 1/2	25A14PG14
450	636	1329	37/64	1 1/2	25A15PG15
480	679	1417	37/64	1 3/4	25A16PG16
510	721	1507	37/64	1 3/4	25A17PG17
540	764	1595	37/64	1 3/4	25A18PG18
570	806	1684	37/64	1 3/4	25A19PG19
600	848	1772	37/64	1 3/4	25A20PG20

PHENOLIC TUBE TYPES

MAX. RMS INPUT VOLTS	MAX. PEAK INPUT VOLTS	MAX. ZENER VOLTS[1]	DIMENSIONS DIA. (A)	DIMENSIONS LENGTH (B)	DIMENSIONS FERRULE LENGTH (C)	ITT PART NO. FERRULE	ITT PART NO. WIRE LEAD
30	42	104	15/32	31/32	3/8	8A1QBG1	8A1ABG1
60	85	208	15/32	31/32	3/8	8A2QBG2	8A2ABG2
90	127	312	15/32	31/32	3/8	8A3QBG3	8A3ABG3
120	170	416	15/32	31/32	3/8	8A4QBG4	8A4ABG4
150	212	519	15/32	31/32	3/8	8A5QBG5	8A5ABG5
180	254	623	15/32	31/32	3/8	8A6QBG6	8A6ABG6
210	297	727	15/32	31/32	3/8	8A7QBG7	8A7ABG7
240	339	831	15/32	31/32	3/8	8A8QBG8	8A8ABG8
270	382	934	15/32	31/32	3/8	8A9QBG9	8A9ABG9
300	424	1039	15/32	31/32	3/8	8A10QBG10	8A10ABG10
330	467	1143	15/32	1 17/64	3/8	8A11QBG11	8A11ABG11
360	509	1247	15/32	1 17/64	3/8	8A12QBG12	8A12ABG12
390	551	1350	15/32	1 17/64	3/8	8A13QBG13	8A13ABG13
420	594	1454	15/32	1 17/64	3/8	8A14QBG14	8A14ABG14
450	636	1558	15/32	1 17/64	3/8	8A15QBG15	8A15ABG15
480	679	1662	15/32	1 1/2	3/8	8A16QBG16	8A16ABG16
510	721	1766	15/32	1 1/2	3/8	8A17QBG17	8A17ABG17
540	764	1870	15/32	1 1/2	3/8	8A18QBG18	8A18ABG18
570	806	1974	15/32	1 1/2	3/8	8A19QBG19	8A19ABG19
600	848	2078	15/32	1 1/2	3/8	8A20QBG20	8A20ABG20

MAX. RMS INPUT VOLTS	MAX. PEAK INPUT VOLTS	MAX. ZENER VOLTS[2]	DIMENSIONS DIA. (A)	DIMENSIONS LENGTH (B)	DIMENSIONS FERRULE LENGTH (C)	ITT PART NO. FERRULE	ITT PART NO. WIRE LEAD
30	42	104	31/32	1 1/32	13/32	25A1QBG1	25A1ABG1
60	85	208	31/32	1 1/32	13/32	25A2QBG2	25A2ABG2
90	127	312	31/32	1 1/32	13/32	25A3QBG3	25A3ABG3
120	170	416	31/32	1 1/32	13/32	25A4QBG4	25A4ABG4
150	212	519	31/32	1 1/32	13/32	25A5QBG5	25A5ABG5
180	254	623	31/32	1 1/32	13/32	25A6QBG6	25A6ABG6
210	297	727	31/32	1 1/32	13/32	25A7QBG7	25A7ABG7
240	339	831	31/32	1 1/32	13/32	25A8QBG8	25A8ABG8
270	382	934	31/32	1 1/32	13/32	25A9QBG9	25A9ABG9
300	424	1039	31/32	1 1/32	13/32	25A10QBG10	25A10ABG10
330	467	1143	31/32	1 29/64	13/32	25A11QBG11	25A11ABG11
360	509	1247	31/32	1 29/64	13/32	25A12QBG12	25A12ABG12
390	551	1350	31/32	1 29/64	13/32	25A13QBG13	25A13ABG13
420	594	1454	31/32	1 29/64	13/32	25A14QBG14	25A14ABG14
450	636	1558	31/32	1 29/64	13/32	25A15QBG15	25A15ABG15
480	679	1662	31/32	1 11/16	13/32	25A16QBG16	25A16ABG16
510	721	1766	31/32	1 11/16	13/32	25A17QBG17	25A17ABG17
540	764	1870	31/32	1 11/16	13/32	25A18QBG18	25A18ABG18
570	806	1974	31/32	1 11/16	13/32	25A19QBG19	25A19ABG19
600	848	2078	31/32	1 11/16	13/32	25A20QBG20	25A20ABG20

EYELET TYPES

MAX. RMS INPUT VOLTS	MAX. PEAK INPUT VOLTS	MAX. ZENER VOLTS[3]	DIMENSIONS LENGTH (B)	ITT PART NO.
25	35	80	47/64	102G1EX1
50	70	159	13/16	102G2EX2
75	105	239	57/64	102G3EX3
100	140	319	31/32	102G4EX4
125	175	398	1 3/64	102G5EX5
150	210	478	1 1/8	102G6EX6
175	245	558	1 13/64	102G7EX7
200	280	637	1 19/64	102G8EX8

STUD TYPES

MAX. RMS INPUT VOLTS	MAX. PEAK INPUT VOLTS	MAX. ZENER VOLTS[3]	DIMENSIONS STUD LENGTH (A)	DIMENSIONS STACK LENGTH (B)	ITT PART NO.
25	35	80	1 7/16	15/16	102G1BX1
50	70	159	1 1/2	1	102G2BX2
75	105	239	1 5/8	1 1/8	102G3BX3
100	140	319	1 11/16	1 3/16	102G4BX4
125	175	398	1 3/4	1 1/4	102G5BX5
150	210	478	1 7/8	1 3/8	102G6BX6
175	245	558	1 15/16	1 7/16	102G7BX7
200	280	637	2	1 1/2	102G8BX8
225	315	717	2 1/16	1 9/16	102G9BX9
250	350	797	2 3/16	1 11/16	102G10BX10
275	385	876	2 1/4	1 3/4	102G11BX11
300	420	956	2 5/16	1 13/16	102G12BX12
325	455	1035	2 3/8	1 7/8	102G13BX13
350	490	1115	2 1/2	2	102G14BX14
375	525	1195	2 9/16	2 1/16	102G15BX15
400	560	1274	2 5/8	2 1/8	102G16BX16
425	595	1354	2 3/4	2 1/4	102G17BX17
450	630	1434	2 13/16	2 5/16	102G18BX18
475	665	1513	2 7/8	2 3/8	102G19BX19
500	700	1593	2 15/16	2 7/16	102G20BX20
600	840	1913	3 5/16	2 13/16	102G24BX24

NOTES: 1. At 4 millisecond pulse current=0.75 Amperes
2. At 4 millisecond pulse current=2 Amperes
3. At 4 millisecond pulse current=8 Amperes

ELECTRICAL AND MECHANICAL CHARACTERISTICS – DC INPUT TYPES

PAPER TUBE TYPES

MAX. RMS INPUT VOLTS	MAX. PEAK INPUT VOLTS	MAX. ZENER VOLTS	DIMENSIONS DIA. (A)	DIMENSIONS LENGTH (B)	ITT PART NO.
20	31	104	3/8	27/32	8A1PG0
40	63	208	3/8	27/32	8A2PG0
60	93	312	3/8	27/32	8A3PG0
80	126	416	3/8	27/32	8A4PG0
100	157	519	3/8	27/32	8A5PG0
120	188	623	3/8	27/32	8A6PG0
140	220	727	3/8	27/32	8A7PG0
160	251	831	3/8	27/32	8A8PG0
180	282	934	3/8	27/32	8A9PG0
200	314	1039	3/8	27/32	8A10PG0
220	345	1143	3/8	1 3/32	8A11PG0
240	377	1247	3/8	1 3/32	8A12PG0
260	409	1350	3/8	1 3/32	8A13PG0
280	440	1454	3/8	1 3/32	8A14PG0
300	472	1558	3/8	1 3/32	8A15PG0
320	502	1662	3/8	1 3/32	8A16PG0
340	534	1766	3/8	1 3/32	8A17PG0
360	566	1870	3/8	1 3/32	8A18PG0
380	597	1974	3/8	1 3/32	8A19PG0
400	628	2078	3/8	1 3/32	8A20PG0

MAX. RMS INPUT VOLTS	MAX. PEAK INPUT VOLTS	MAX. ZENER VOLTS[2]	DIMENSIONS DIA. (A)	DIMENSIONS LENGTH (B)	ITT PART NO.
20	31	87	37/64	1 1/64	25A1PG0
40	63	177	37/64	1 1/64	25A2PG0
60	93	266	37/64	1 1/64	25A3PG0
80	126	354	37/64	1 1/64	25A4PG0
100	157	443	37/64	1 1/64	25A5PG0
120	188	532	37/64	1 1/64	25A6PG0
140	220	620	37/64	1 1/64	25A7PG0
160	251	709	37/64	1 1/64	25A8PG0
180	282	798	37/64	1 1/64	25A9PG0
200	314	886	37/64	1 1/64	25A10PG0
220	345	975	37/64	1 1/4	25A11PG0
240	377	1063	37/64	1 1/4	25A12PG0
260	409	1152	37/64	1 1/4	25A13PG0
280	440	1241	37/64	1 1/4	25A14PG0
300	472	1329	37/64	1 1/4	25A15PG0
320	502	1417	37/64	1 1/4	25A16PG0
340	534	1507	37/64	1 1/4	25A17PG0
360	566	1595	37/64	1 1/4	25A18PG0
380	597	1684	37/64	1 1/4	25A19PG0
400	628	1772	37/64	1 1/4	25A20PG0

PHENOLIC TUBE TYPES

MAX. RMS INPUT VOLTS	MAX. PEAK INPUT VOLTS	MAX. ZENER VOLTS[1]	DIMENSIONS DIA. (A)	DIMENSIONS LENGTH (B)	DIMENSIONS FERRULE LENGTH (C)	ITT PART NO. FERRULE	ITT PART NO. WIRE LEAD
20	31	104	15/32	31/32	3/8	8A1QBG0	8A1ABG0
40	63	208	15/32	31/32	3/8	8A2QBG0	8A2ABG0
60	93	312	15/32	31/32	3/8	8A3QBG0	8A3ABG0
80	126	416	15/32	31/32	3/8	8A4QBG0	8A4ABG0
100	157	519	15/32	31/32	3/8	8A5QBG0	8A5ABG0
120	188	623	15/32	31/32	3/8	8A6QBG0	8A6ABG0
140	120	727	15/32	31/32	3/8	8A7QBG0	8A7ABG0
160	251	831	15/32	31/32	3/8	8A8QBG0	8A8ABG0
180	282	934	15/32	31/32	3/8	8A9QBG0	8A9ABG0
200	314	1039	15/32	31/32	3/8	8A10QBG0	8A10ABG0
220	345	1143	15/32	31/32	3/8	8A11QBG0	8A11ABG0
240	377	1247	15/32	31/32	3/8	8A12QBG0	8A12ABG0
260	409	1350	15/32	31/32	3/8	8A13QBG0	8A13ABG0
280	440	1454	15/32	31/32	3/8	8A14QBG0	8A14ABG0
300	472	1558	15/32	31/32	3/8	8A15QBG0	8A15ABG0
320	502	1662	15/32	31/32	3/8	8A16QBG0	8A16ABG0
340	534	1766	15/32	31/32	3/8	8A17QBG0	8A17ABG0
360	566	1870	15/32	31/32	3/8	8A18QBG0	8A18ABG0
380	597	1974	15/32	31/32	3/8	8A19QBG0	8A19ABG0
400	628	2078	15/32	31/32	3/8	8A20QBG0	8A20ABG0

MAX. RMS INPUT VOLTS	MAX. PEAK INPUT VOLTS	MAX. ZENER VOLTS[2]	DIMENSIONS DIA. (A)	DIMENSIONS LENGTH (B)	DIMENSIONS FERRULE LENGTH (C)	ITT PART NO. FERRULE	ITT PART NO. WIRE LEAD
20	31	104	31/32	1 1/32	13/32	25A1QBG0	25A1ABG0
40	63	208	31/32	1 1/32	13/32	25A2QBG0	25A2ABG0
60	93	312	31/32	1 1/32	13/32	25A3QBG0	25A3ABG0
80	126	416	31/32	1 1/32	13/32	25A4QBG0	25A4ABG0
100	157	519	31/32	1 1/32	13/32	25A5QBG0	25A5ABG0
120	188	623	31/32	1 1/32	13/32	25A6QBG0	25A6ABG0
140	220	727	31/32	1 1/32	13/32	25A7QBG0	25A7ABG0
160	251	831	31/32	1 1/32	13/32	25A8QBG0	25A8ABG0
180	282	934	31/32	1 1/32	13/32	25A9QBG0	25A9ABG0
200	314	1039	31/32	1 1/32	13/32	25A10QBG0	25A10ABG0
220	345	1143	31/32	1 1/32	13/32	25A11QBG0	25A11ABG0
240	377	1247	31/32	1 1/32	13/32	25A12QBG0	25A12ABG0
260	409	1350	31/32	1 1/32	13/32	25A13QBG0	25A13ABG0
280	440	1454	31/32	1 1/32	13/32	25A14QBG0	25A14ABG0
300	472	1558	31/32	1 1/32	13/32	25A15QBG0	25A15ABG0
320	502	1662	31/32	1 1/32	13/32	25A16QBG0	25A16ABG0
340	534	1766	31/32	1 1/32	13/32	25A17QBG0	25A17ABG0
360	566	1870	31/32	1 1/32	13/32	25A18QBG0	25A18ABG0
380	597	1974	31/32	1 1/32	13/32	25A19QBG0	25A19ABG0
400	628	2078	31/32	1 1/32	13/32	25A20QBG0	25A20ABG0

EYELET TYPES

MAX. RMS INPUT VOLTS	MAX. PEAK INPUT VOLTS	MAX. ZENER VOLTS[3]	DIMENSIONS LENGTH (B)	ITT PART NO.
20	31	80	27/32	102G1EX0
40	63	159	7/8	102G2EX0
60	93	239	29/32	102G3EX0
80	126	319	15/16	102G4EX0
100	157	398	1	102G5EX0
120	188	478	1 1/32	102G6EX0
140	220	558	1 1/16	102G7EX0
160	251	637	1 1/8	102G8EX0
180	282	717	1 5/32	102G9EX0
200	314	795	1 3/16	102G10EX0
220	345	876	1 1/4	102G11EX0
240	377	956	1 9/32	102G12EX0
260	409	1035	1 5/16	102G13EX0
280	440	1115	1 11/32	102G14EX0
300	472	1195	1 3/8	102G15EX0
320	502	1274	1 7/16	102G16EX0

STUD TYPES

MAX. RMS INPUT VOLTS	MAX. PEAK INPUT VOLTS	MAX. ZENER VOLTS[3]	DIMENSIONS STUD LENGTH (A)	DIMENSIONS STACK LENGTH (B)	ITT PART NO.
20	31	80	1 5/16	13/16	102G1BX0
40	63	159	1 3/8	27/32	102G2BX0
60	93	239	1 3/8	7/8	102G3BX0
80	126	319	1 7/16	29/32	102G4BX0
100	157	398	1 1/2	15/16	102G5BX0
120	188	478	1 5/8	1 3/32	102G6BX0
140	220	558	1 5/8	1 1/8	102G7BX0
160	251	637	1 11/16	1 3/16	102G8BX0
180	282	717	1 3/4	1 7/32	102G9BX0
200	314	797	1 3/4	1 1/4	102G10BX0
220	345	876	1 13/16	1 9/32	102G11BX0
240	377	956	1 7/8	1 11/32	102G12BX0
260	409	1035	1 15/16	1 3/8	102G13BX0
280	440	1115	1 15/16	1 13/32	102G14BX0
300	472	1195	1 15/16	1 15/32	102G15BX0
320	502	1274	2	1 1/2	102G16BX0

NOTES: 1. At 4 millisecond pulse current=0.75 Amperes
2. At 4 millisecond pulse current=2 Amperes
3. At 4 millisecond pulse current=8 Amperes

HOW TO SELECT THE PROPER RECTIFIER

Determination of Current Rating

Although the peak value and duration of a transient current cannot always be determined, certain valid assumptions can be made to determine the ITT suppressor rectifier current rating for the application.

For circuits in which a transformer is the power source, usually the greatest transient currents have been observed when the circuit is interrupted with no load on the transformer. The transient current is the magnetizing current of the transformer. If the actual transient current is not known, a valid assumption can be made by the use of the magnetizing current versus voltage on page 4. If the transient results from opening a circuit containing an inductance, the transient current will be the current through the inductance at the instant of interruption. To select the proper ITT suppressor series, assume a single pulse width of 4 milliseconds and refer to the pulse current versus time curve on page 4. The same curve can be used to select the appropriate ITT series when a single pulse width other than 4 milliseconds is known or assumed.

Voltage Rating

After the required current rating has been established, determine the maximum steady-state voltage which will appear across the suppressor rectifier and select the appropriate type number from the tables on pages 2 and 3. Note that both RMS and peak voltage ratings are tabulated for AC types and DC ratings for DC types. Use the RMS value for sinusoidal voltages; otherwise, use the peak value of the input voltage to select the proper rectifier.

Zener Voltage

The Zener voltages shown in the characteristics tables are the maximum instantaneous voltages that will appear across the rectifier if the 4 millisecond current rating is not exceeded. Any ITT suppressor rectifier can safely discharge higher currents than this rating, where the pulse width is less than 4 milliseconds.

For other values of peak current, however, the indicated Zener voltage will be as shown in the curves on page 4. To obtain the expected protection, rectifiers should be used within their rated currents. For optimum protection, the maximum Zener voltage should be below the PIV rating of the semiconductor devices being protected.

The maximum Zener voltages shown in the characteristics tables have been derived from the curves on page 4 which represent the conservative ratings placed on suppressor rectifiers. These volt-ampere curves apply to a single cell. To determine the Zener voltage for a particular rectifier, multiply the peak voltage values that are shown by the number of cells per arm for AC rectifiers, or by the total number of cells for DC rectifiers. The final step is to be sure that the silicon or germanium rectifier or silicon controlled rectifier to be protected has a PIV rating higher than the Zener voltage of the ITT protector rectifier. The volt-ampere curves are also valid for DC applications in determining the proper rectifier for a given peak transient voltage.

Similar protection is also provided to transformers, capacitors, resistors, switches, relays, or any electrical component subject to damage from transient over-voltage.

Example

Assume a single phase full-wave bridge rectifier application with a transformer rated at 8.5KVA, 115V. The rectifier to be protected is across the transformer secondary.

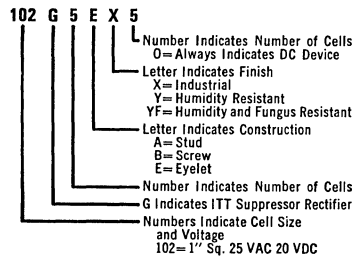
1. Assume a 4 millisecond pulse width.
2. From the curve on page 4, determine the per cent of magnetizing current. Using the "maximum" plot line, 8.5KVA $\approx$5.2% of full load current.

Full load current $\frac{VA}{V} \approx \frac{8500}{115} \approx 74A$

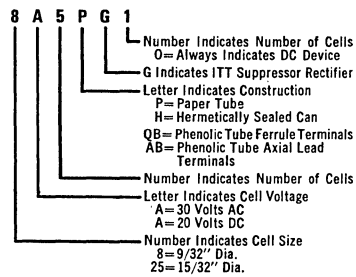
$74A \times 5.2\% \approx 3.85A$ peak.

3. From the RATINGS table on page 1, select a rectifier series which will withstand 3.85A peak @ 4 millisecond pulse width. The 102 series, either stud mounting or eyelet mounting may be used. Assume a stud type is preferred for this application.
4. Select the appropriate ITT part number from the stud mounting table on page 2 by finding a type with a RMS input voltage rating equal to or above 115V. 102G5BX5 meets this requirement.
5. Determine the PIV rating required for the rectifier to be protected. Use the 102 series curve on page 4 to determine the voltage corresponding to 3.85A. The maximum voltage is 73 volts per cell. The number of cells in each rectifier is indicated by the first number after the first letter in the part number. In this case the 102G5BX5 has five cells. The maximum voltage is $73 \times 5 = 365V$. The PIV rating required for the protected rectifier is 365V.

CODING SYSTEM FOR EYELET AND STUD TYPE ITT SELENIUM VOLTAGE SUPPRESSOR RECTIFIERS

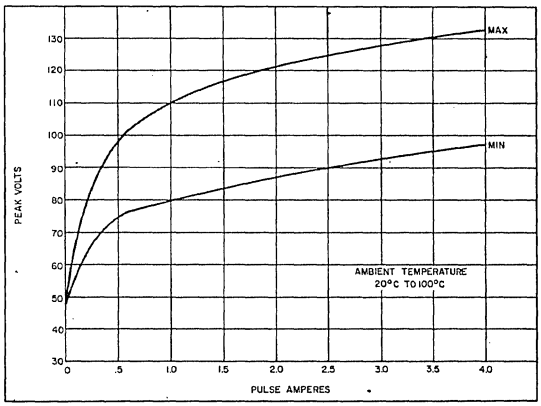


CODING SYSTEM FOR TUBULAR TYPE ITT SELENIUM VOLTAGE SUPPRESSOR RECTIFIERS

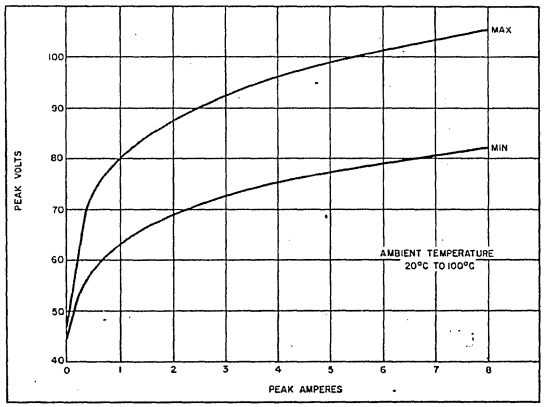


CHARACTERISTIC CURVES

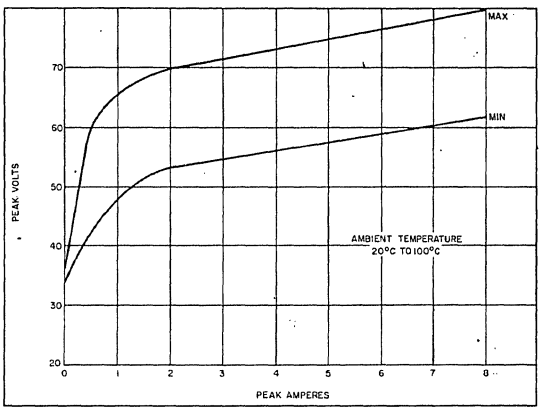
8A1 SERIES PEAK VOLTAGE VS CURRENT



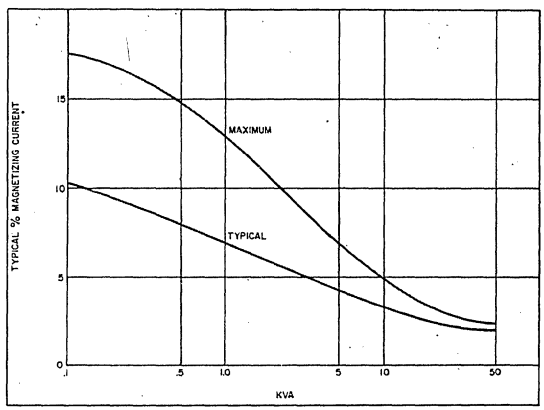
25A1 SERIES PEAK VOLTAGE VS CURRENT



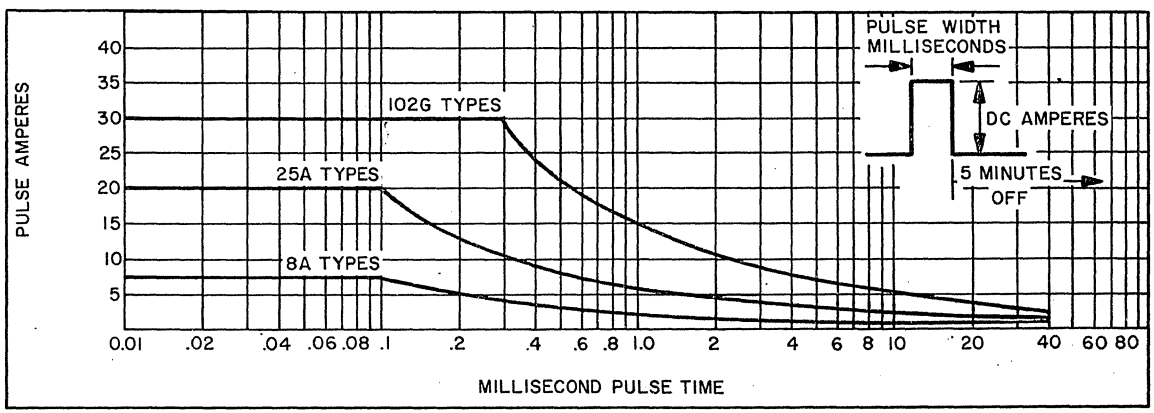
102 SERIES PEAK VOLTAGE VS CURRENT



MAGNETIZING CURRENT VS VOLTAGE

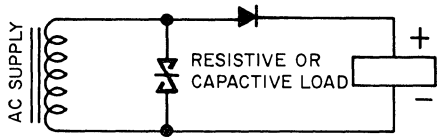


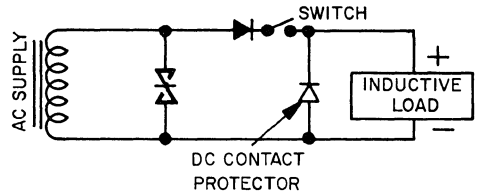
PULSE CURRENT VS TIME



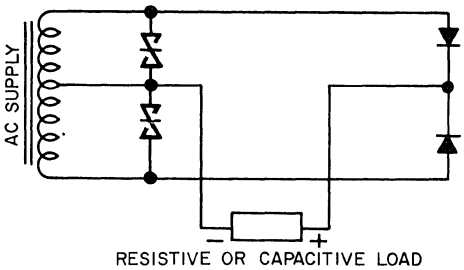
TYPICAL APPLICATIONS

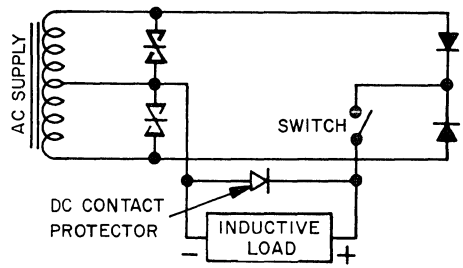
Single-Phase Half-Wave Silicon Rectifier



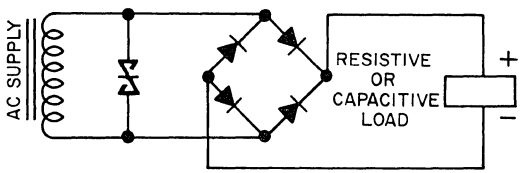


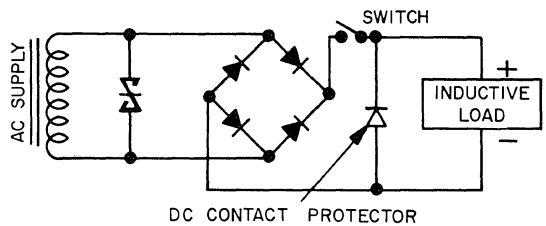
Single-Phase Full-Wave Center Tap Silicon Rectifier



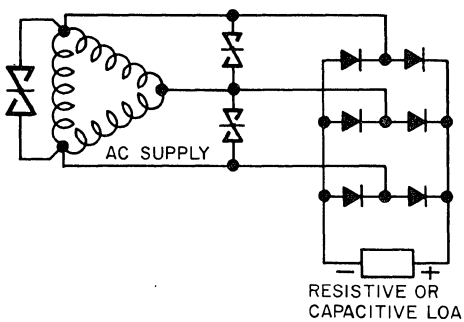


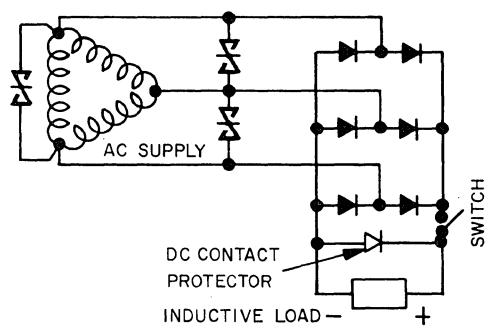
Single-Phase Full-Wave Bridge Silicon Rectifier



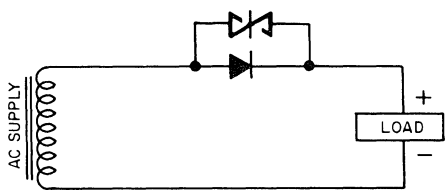


Three-Phase Full-Wave Bridge Silicon Rectifier

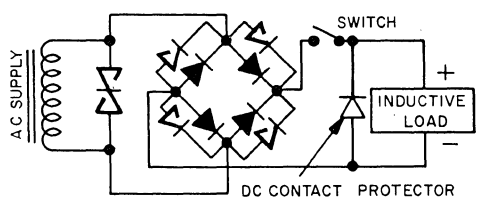




Single-Phase Half-Wave Silicon-Controlled Rectifier



Single-Phase Full-Wave Silicon Rectifier



Package: DO-7

DIFFUSED SILICON GENERAL-PURPOSE DIODES

ABSOLUTE MAXIMUM RATINGS at 25°C free-air temperature (unless otherwise noted)

Symbol	Characteristics	1N645	1N646	1N647	1N648	1N649	Unit
$V_{RM(wkg)}$	Working Peak Reverse Voltage over Operating Free-Air Temperature Range	225	300	400	500	600	V
I_O	Average Rectified Forward Current at (or below) 25°C Free-Air Temperature (See Note 1)	400					mA
I_O	Average Rectified Forward Current at 150°C Free-Air Temperature (See Note 1)	150					mA
$I_{FM(surge)}$	Peak Surge Current, One Second, at 25°C to 150°C Free-Air Temperature (See Note 2)	3					A
P	Continuous Power Dissipation at (or below) 25°C Free-Air Temperature (See Note 3)	600					mW
$T_{A(opr)}$	Operating Free-Air Temperature Range	−65 to 150					°C

ELECTRICAL CHARACTERISTICS at 25°C free-air temperature (unless otherwise noted)

Symbol	Parameter	1N645* Min Max	1N646 Min Max	1N647* Min Max	1N648 Min Max	1N649* Min Max	Unit	Conditions
$V_{(BR)}$	Reverse Breakdown Voltage	275	360	480	600	720	V	I_R = 100 μA, T_A = 100°C
I_R	Static Reverse Current	0.2	0.2	0.2	0.2	0.2	μA	V_R = Rated $V_{RM(wkg)}$
		15	15	20	20	25	μA	V_R = Rated $V_{RM(wkg)}$, T_A = 100°C
V_F	Static Forward Voltage	1	1	1	1	1	V	I_F = 400 mA
C_T	Total Capacitance	6 typ	6 typ	6 typ	6 typ	6 typ	pF	V_R = 12 V, f = 1 MHz

NOTES:

1. These values may be applied continuously under single-phase 60-Hz half-sine-wave operation with resistive load. Above 25°C see Thermal Characteristics Chart.
2. These values apply for a one-second square-wave pulse with the device at nonoperating thermal equilibrium immediately prior to the surge.
3. Derate linearly to 200 mW at 150°C free-air temperature at the rate of 3.2 mW/deg.

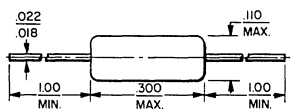
* IN645, IN647 and IN649 are available in JAN and JAN TX versions.

JAN 1N645®
SILICON DIODE

DIFFUSED SILICON HIGH POWER GLASS RECTIFIER

The ITT JAN 1N645 meets MIL-S-19500/240B.

DIMENSIONS



DO-7

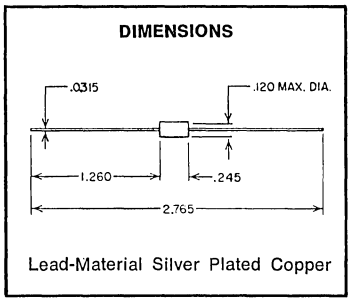
ABSOLUTE MAXIMUM RATINGS

CHARACTERISTICS @ 25°C unless otherwise noted.		UNITS
Peak Inverse Voltage	270	Volts
Power Dissipation	500	mW
Storage Temperature	−65 to +200	°C
Surge Current, 1/120 second, 150°C	5	Amps

ELECTRICAL CHARACTERISTICS @ 25°C unless otherwise noted.

SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS
PIV	270			Vdc	I_R=100μA
I_R			25 15	nA μA	V_R=225V V_R=225V, T=150°C
V_F			1.0	Vdc	I_F=400 mA
C			20	pF	V_R=4V

1-AMP PLASTIC SILICON RECTIFIERS



The ITT Plastic Silicon Rectifier is molded using a new plastic formulation with the following advantages over silicone and epoxy compounds:

- **Lower thermosetting temperature (170°F) resulting in less strain to junctions and surfaces during the molding process.**
- **No pre-cure or post-cure needed.**
- **Moisture resistance and humidity resistance far superior to others.**

ELECTRICAL CHARACTERISTICS @ 25°C unless otherwise noted

		*1N4000 Series	EM500 Series	Units
Peak Reverse Voltage (PRV)	50	1N4001 50	(EM500)	Volts
	100	1N4002 100	(EM501)	
	200	1N4003 200	(EM502)	
	400	1N4004 400	(EM504)	
	600	1N4005 600	(EM506)	
	800	1N4006 800	(EM508)	
	1000	1N4007 1000	(EM510)	
Average Rectified Current @ 25°C Ambient		1.0	1.0	Amps
75°C Ambient		1.0	0.5	Amps
Forward Voltage Drop @ 1 Amp		1.1	1.1	Volts
Reverse Current @ Rated DC Voltage		10	1.0	Volts
Full Cycle Average Reverse Current @ Rated PRV @				
85°C Ambient @ Rated Average Rectified Current		200	200	Volts
100°C Ambient @ Rated Average Rectified Current		50	50	Volts
Half Cycle Surge Current, 60 Hz		30	50	Amps
Temperature Range (operating)		−65 to +175	−65 to +175	°C
Temperature Range − Storage		−65 to +200	−65 to +200	°C

*Electrical Equivalent

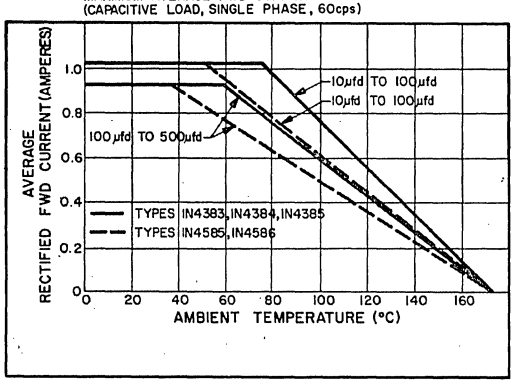
ITT SILICON RECTIFIER CROSS-REFERENCE

Now you can replace older types of rectifiers with dependable, inexpensive ITT Plastic types. In most cases, the ITT types will have higher output current and PRV ratings than the types to be replaced. Case dimensions are not always physically identical, in many cases the ITT types are smaller.

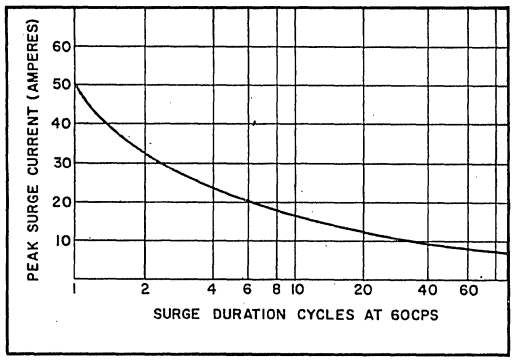
TYPE TO BE REPLACED	ITT REPLACEMENT
1N253	1N4002
1N254	1N4003
1N255	1N4004
1N256	1N4005
1N316	1N4001
1N316A	1N4001
1N317	1N40J2
1N317A	1N4002
1N318	1N4003
1N318A	1N4003
1N319	1N4004
1N319A	1N4004
1N320	1N4005
1N320A	1N40J5
1N321A	1N4007
1N322A	1N4007
1N323A	1N4001
1N324A	1N40J2
1N325A	1N4003
1N326A	1N4004
1N327A	1N4005
1N328A	1N4007
1N329A	1N4007
1N332	1N4004
1N333	1N4004
1N334	1N4004
1N335	1N4004
1N336	1N4003
1N337	1N4003
1N338	1N4002
1N339	1N4002
1N340	1N4002
1N341	1N4004
1N342	1N4004
1N343	1N4004
1N344	1N4004
1N345	1N4003
1N346	1N4003
1N347	1N4002
1N348	1N4002
1N349	1N4002
1N359A	1N4002
1N360A	1N4002
1N361A	1N4003
1N362A	1N4004
1N363A	1N4005
1N364A	1N4007
1N365A	1N4007
1N440	1N4002
1N440B	1N4002
1N441	1N4003
1N441B	1N4003
1N442	1N4004
1N442B	1N4004
1N443	1N4004
1N43B	1N4004
1N444	1N4005
1N44B	1N4005
1N445	1N4005
1N445B	1N4005
1N530	1N4002
1N531	1N4003
1N532	1N4004
1N533	1N4004
1N534	1N4005
1N535	1N4005
1N536	1N4001
1N537	1N4002
1N538	1N4003
1N539	1N4004
1N540	1N4004
1N547	1N4005
1N550	1N4002
1N551	1N4003
1N552	1N4004
1N553	1N4004
1N554	1N4005
1N555	1N4005
1N560	1N4006
1N561	1N4007
1N562	1N4006
1N563	1N4007
1N596	1N4005
1N597	1N4006
1N598	1N4007
1N599	1N4001
1N599A	1N4001
1N600	1N4002
1N600A	1N4002
1N601	1N4003
1N601A	1N4003
1N602	1N4003
1N602A	1N4003
1N603	1N4004
1N603A	1N4004
1N604	1N4004
1N604A	1N4004
1N605	1N4005
1N605A	1N4005
1N606	1N4005
1N606A	1N4005
1N607	1N4001
1N607A	1N4001
1N608	1N4002
1N608A	1N4002
1N609	1N4003
1N609A	1N4003
1N610	1N4003
1N610A	1N4003
1N611	1N4004
1N611A	1N4004
1N612	1N4004
1N612A	1N4004
1N613	1N4005
1N613A	1N4005
1N614	1N4005
1N614A	1N4005
1N645	1N4004
1N645A	1N4004
1N646	1N4004
1N647	1N4004
1N648	1N4005
1N649	1N4005
1N676	1N4002
1N677	1N4002
1N678	1N4003
1N679	1N4003
1N681	1N4004
1N682	1N4004
1N683	1N4004
1N684	1N4004
1N685	1N4005
1N686	1N4005
1N687	1N4005
1N689	1N4005
1N846	1N4001
1N847	1N4002
1N848	1N4003
1N849	1N4004
1N850	1N4004
1N851	1N4005
1N852	1N4005
1N853	1N4006
1N854	1N4006
1N855	1N4007
1N856	1N4007
1N857	1N4001
1N858	1N4002
1N859	1N4003
1N860	1N4004
1N861	1N4004
1N862	1N4005
1N863	1N4005
1N864	1N4006
1N865	1N4006
1N866	1N4007
1N867	1N4007
1N868	1N4001
1N869	1N4002
1N870	1N4003
1N871	1N4004
1N872	1N4004
1N873	1N4005
1N874	1N4005
1N875	1N4006
1N876	1N4006
1N877	1N4007
1N878	1N4007
1N879	1N4001
1N880	1N4002
1N881	1N4003
1N882	1N4004
1N883	1N4004
1N884	1N4005
1N885	1N4005
1N886	1N4006
1N887	1N4006
1N888	1N4007
1N889	1N4007
1N1081	1N4002
1N1082	1N4003
1N1083	1N4004
1N1084	1N4004
1N1095	1N4005
1N1096	1N4005
1N1100	1N4002
1N1101	1N4003
1N1102	1N4004
1N1103	1N4004
1N1104	1N4005
1N1105	1N4005
1N1122A	1N4004
1N1169	1N4004
1N1217	1N4001
1N1217A	1N4001
1N1218	1N4002
1N1218A	1N4002
1N1219	1N4003
1N1219A	1N4003
1N1220	1N4003
1N1220A	1N4003
1N1221	1N4004
1N1221A	1N4004
1N1222	1N4004
1N1223	1N4005
1N1224	1N4005
1N1224A	1N4005
1N1225	1N4006
1N1225A	1N4006
1N1226	1N4006
1N1226A	1N4006
1N1251	1N4002
1N1252	1N4002
1N1253	1N4003
1N1254	1N4004
1N1255	1N4004
1N1443	1N4007
1N1486	1N4005
1N1487	1N4002
1N1488	1N4003
1N1489	1N4004
1N1490	1N4004
1N1491	1N4005
1N1492	1N4005
1N1538	1N4002
1N1539	1N4003
1N1540	1N4003
1N1541	1N4004
1N1542	1N4004
1N1543	1N4005
1N1544	1N4005
1N1617	1N4002
1N1618	1N4003
1N1619	1N4004
1N1620	1N4004
1N1692	1N4002
1N1693	1N4003
1N1694	1N4004
1N1695	1N4004
1N1696	1N4005
1N1697	1N4005
1N1701	1N4001
1N1702	N4002
1N1703	1N4003
1N1704	1N4004
1N1705	1N4004
1N1706	1N4005
1N1707	1N4001
1N1708	1N4002
1N1709	1N4003
1N1710	1N4004
1N1711	1N4004
1N1712	1N4005
1N1730	1N4007
1N1763	1N4004
1N1764	1N4005
1N1907	1N4001
1N1908	1N4002
1N1909	1N4003
1N1911	1N4004
1N1912	1N4005
1N1913	1N4005
1N1914	1N4006
1N1915	1N4006
1N1916	1N4007
1N2069	1N4003
1N2069A	1N4003
1N2070	1N4004
1N2070A	1N4004
1N2071	1N4005
1N2071A	1N4005
1N2072	1N4001
1N2073	1N4002
1N2074	1N4003
1N2075	1N4003
1N2076	1N4004
1N2077	1N4004
1N2078	1N4004
1N2079	1N4005
1N2103	1N4001
1N2104	1N4002
1N2105	1N4003
1N2106	1N4004
1N2107	1N4004
1N2108	1N4005
1N2482	1N4003
1N2483	1N4004
1N2484	1N4005
1N2485	1N4003
1N2486	1N4004
1N2487	1N4004
1N2488	1N4005
1N2489	1N4005
1N2609	1N4001
1N2610	1N4002
1N2611	1N4003
1N2612	1N4004
1N2613	1N4004
1N2614	1N4005
1N2615	1N4005
1N2616	1N4006
1N2617	1N4007
1N2858	1N4001
1N2859	1N4002
1N2860	1N4003
1N2861	1N4004
1N2862	1N4004
1N2863	1N4005
1N2864	1N4005
1N2878	1N4006
1N2879	1N4006
1N2880	1N4007
1N2881	1N4007
1N2882	1N4007
1N2883	1N4007
1N3189	1N4003
1N3190	1N4004
1N3191	1N4005
1N3193	1N4003
1N3194	1N4004
1N3195	1N4005
1N3196	1N4006
1N3253	1N4003
1N3254	1N4004
1N3255	1N4005
1N3256	1N4006
1N3544	1N4002
1N3545	1N4003
1N3546	1N4004
1N3547	1N4004
1N3548	1N4005
1N3549	1N4005
1N3611	1N4003
1N3612	1N4004
1N3613	1N4005
1N3614	1N4006
1N3639	1N4003
1N3640	1N4004
1N3641	1N4005
1N3642	1N4006
1N4245	1N4003
1N4246	1N4004
1N4247	1N4005
1N4248	1N4006
1N4249	1N4007
1N4250	1N4006
1N4251	1N4007
1N4361	1N4007
1N4364	1N4002
1N4365	1N4003
1N4366	1N4004
1N4367	1N4004
1N4368	1N4005
1N4369	1N4005
1N4383	1N4003
1N4384	1N4004
1N4385	1N4005
2E4	1N4004
3MS5	1N4001
3MS10	1N4002
3MS20	1N4003
3MS30	1N4004
3MS40	1N4004
3MS50	1N4005
5A2	1N4003
5A4	1N4004
5A5	1N4005
5A6	1N4005
5A8	1N4006
5A10	1N4007
5E4	1N4004
5E5	1N4005
5E6	1N4006
5MA2	1N4003
5MA4	1N4004
5MA5	1N4005
5MA6	1N4005
5MA8	1N4006
5MA10	1N4007
5MS5	1N4001
5MS10	1N4002
5MS20	1N4003
5MS30	1N4004
5MS40	1N4004
5MS50	1N4005
10B1	1N4002
10B2	1N4003
10B3	1N4004
10B4	1N4004
10B5	1N4005
10B6	1N4005
10B8	1N4006
10B10	1N4007
10D2	1N4003
10D3	1N4004
10D4	1N4004
10D5	1N4005
10D6	1N4005
10D7	1N4006
10D8	1N4006
10D10	1N4007
320A	1N4001
320B	1N4002
320C	1N4003
320D	1N4003
320F	1N4004
320H	1N4004
320M	1N4005
320K	1N4005
320P	1N4006
320S	1N4006
320Z	1N4007
359B	1N4002
359D	1N4003
359F	1N4004
359H	1N4004
359K	1N4005
359M	1N4005
359P	1N4006
359S	1N4006
359Z	1N4007
A10A	1N4002
A10B	1N4003
A10C	1N4004
A10D	1N4004
A10E	1N4005
A10M	1N4005
A10N	1N4006
A10P	1N4007
A13A2	1N4002
A13B2	1N4003
A13C2	1N4004
A13D2	1N4004
A13E2	1N4005
A13F2	1N4001
A13M2	1N4005
AH805	1N4006
AH810	1N4006
AH815	1N4006
AH1005	1N4007
AH1010	1N4007
AH1015	1N4007
AM3	1N4001
AM13	1N4002
AM23	1N4003
AM33	1N4004
AM43	1N4004
AM53	1N4005
AM63	1N4005
G100K	1N4006
G100M	1N4007
PA3	1N4004
PA069	1N4003
PA070	1N4004
PA071	1N4005
PA305	1N4001
PA310	1N4002
PA315	1N4003
PA320	1N4003
PA325	1N4004
PA330	1N4004
PA340	1N4004
PA350	1N4005
PA360	1N4005
PA380	1N4006
PT3	1N4004
PT5	1N4004
PT5B	1N4005
PT505	1N4001
PT510	1N4002
PT515	1N4003
PT520	1N4003
PT525	1N4004
PT530	1N4004
PT540	1N4004
PT550	1N4005
PT560	1N4005
S91	1N4002
S91H	1N4002
S92	1N4003
S92H	1N4003
S93	1N4004
S93H	1N4004
S94	1N4004

TYPICAL CHARACTERISTICS @ 25°C unless otherwise noted

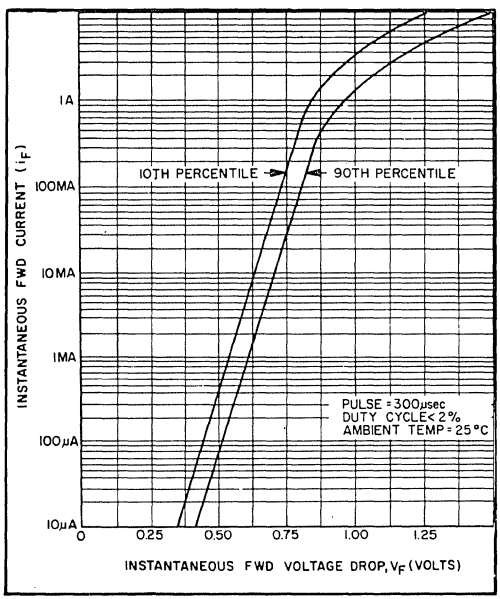
MAXIMUM AVERAGE FWD CURRENT RATING-3/8" LEAD LENGTH
(CAPACITIVE LOAD, SINGLE PHASE, 60cps)



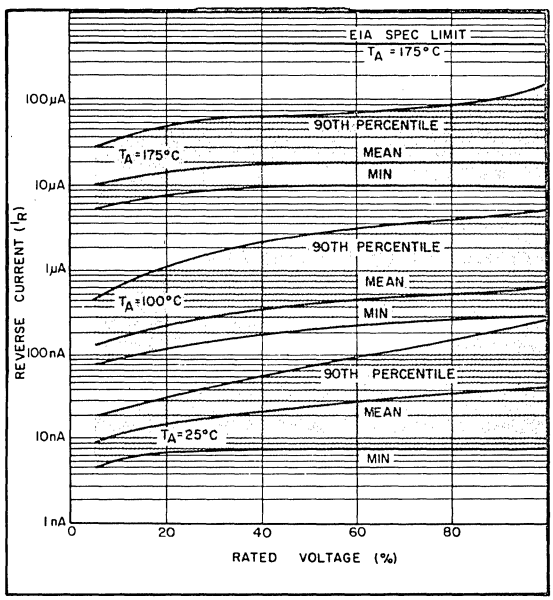
NON-RECURRENT SURGE RATING



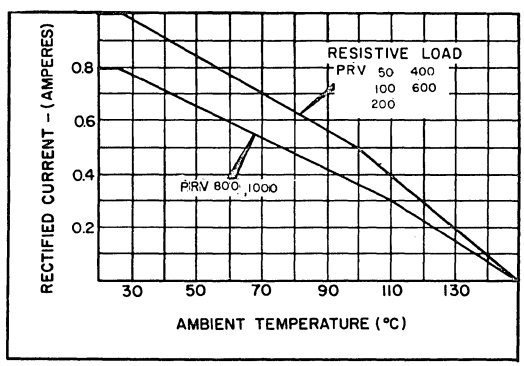
FORWARD VOLTAGE DROP



REVERSE CURRENT



RECTIFIED CURRENT RATING
VS TEMPERATURE

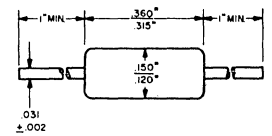


1-AMP SILICON GLASS RECTIFIERS

- **V_R Ratings 50 to 1000 Volts**
- **Surge Current Rating 50 Amperes**
- **100% Scope Tested**

The ITT 1N4383-5, 1N4585-6, offer up to one-amp rectified current at 100°C in a small, hermetically sealed DO-29 glass package. All units are passivated, 100 percent tested, and have a 50-amp surge current rating to insure a stable, highly reliable rectifier. Rectifiers are supplied with solderable leads and may be delivered reel-packed for automatic insertion equipment.

DIMENSIONS



DO-29

MECHANICAL DATA

Case: Hermetically sealed glass
Leads: Solderable, tin plated
Weight: 0.02 oz.
Mounting position: Any
Marking: ITT, cathode band, part number.

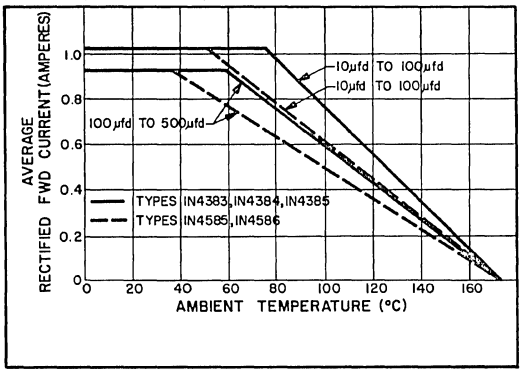
ABSOLUTE MAXIMUM RATINGS[1]

CHARACTERISTICS	RG1122	RG1123	1N4383	1N4384	1N4385	1N4585	1N4586	UNITS
Maximum recurrent peak reverse voltage	50	100	**200**	**400**	**600**	**800**	**1000**	Volts
Maximum RMS voltage	35	70	140	280	420	560	700	Volts
Maximum DC blocking voltage	50	100	200	400	600	800	1000	Volts
Maximum average forward rectified current 3/8" lead length.. 50°C Ambient	1.0	1.0	1.0	1.0	1.0	1.0	1.0	Amps
100°C Ambient	1.0	1.0	1.0	1.0	1.0	0.6	0.6	Amps
150°C Ambient	0.3	0.3	0.3	0.3	0.3	0.2	0.2	Amps
Maximum peak surge overload current 1 Cycle	**50**	**50**	**50**	**50**	**50**	**50**	**50**	Amps
10 Cycles	16	16	16	16	16	16	16	Amps
100 Cycles	6	6	6	6	6	6	6	Amps
Maximum forward voltage drop at 1 amp DC, 25°C	1.0	1.0	1.0	1.0	1.0	1.0	1.0	Volts
Maximum full cycle average reverse current, @rated average forward current and 100°C ambient	275	250	275	250	225	200	200	μamps
Maximum DC leakage at rated DC blocking voltage and 25°C ambient	10	10	10	10	10	10	10	μamps
Typical recovery time at 25°C ambient	10	10	10	10	10	10	10	μsecs
Temperature Range, op & stg.	—65 to +175							°C

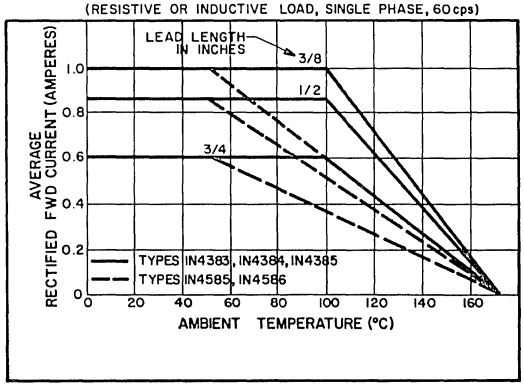
NOTE: 60 cps, inductive or resistive load, single phase half wave.

TYPICAL CHARACTERISTICS @ 25°C unless otherwise noted

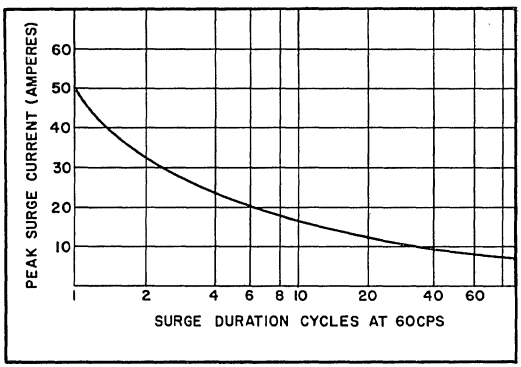
MAXIMUM AVERAGE FWD CURRENT RATING-3/8" LEAD LENGTH
(CAPACITIVE LOAD, SINGLE PHASE, 60cps)



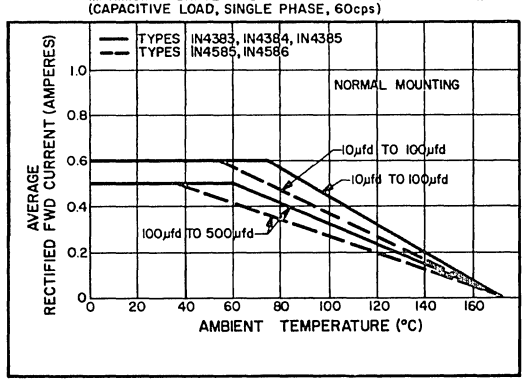
MAXIMUM AVERAGE FORWARD CURRENT RATING
(RESISTIVE OR INDUCTIVE LOAD, SINGLE PHASE, 60cps)



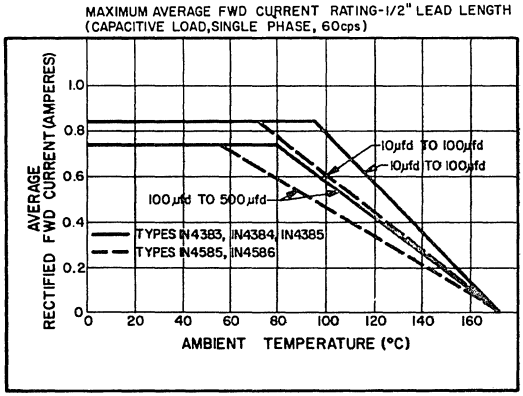
NON-RECURRENT SURGE RATING
(-65°C TO 175°C)



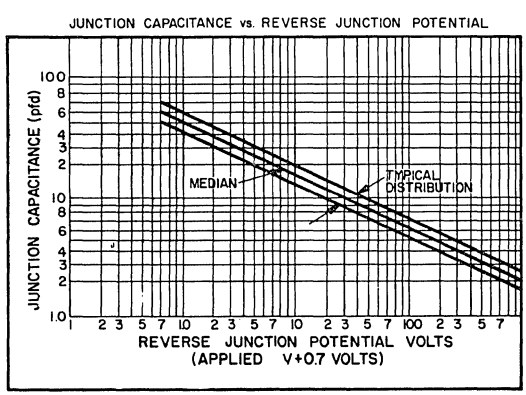
MAXIMUM AVERAGE FWD CURRENT RATING-3/4" LEAD LENGTH
(CAPACITIVE LOAD, SINGLE PHASE, 60cps)



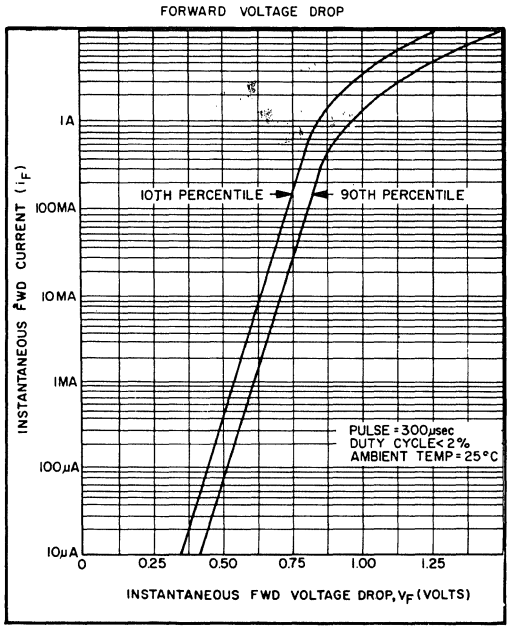
MAXIMUM AVERAGE FWD CURRENT RATING-1/2" LEAD LENGTH
(CAPACITIVE LOAD, SINGLE PHASE, 60cps)

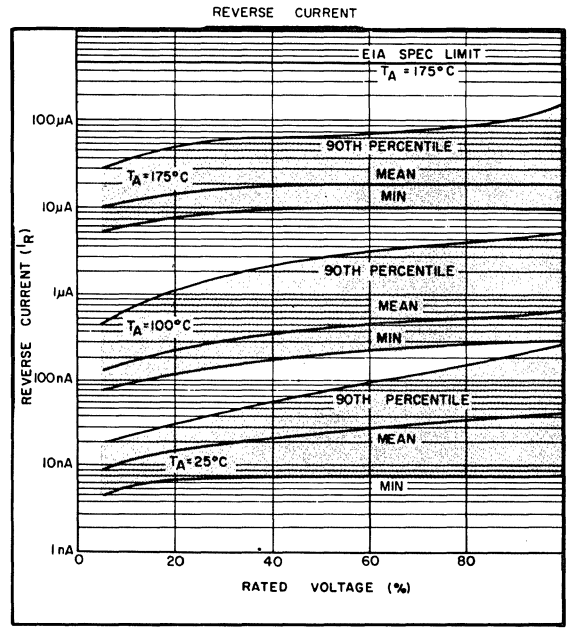


JUNCTION CAPACITANCE vs. REVERSE JUNCTION POTENTIAL



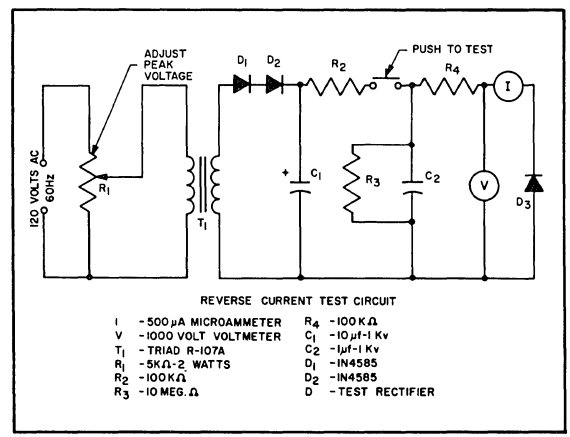
TYPICAL CHARACTERISTICS, continued





DC REVERSE LEAKAGE TEST

The circuit at right provides a simple and inexpensive means for checking the instantaneous leakage characteristics of the 1N4383 series and other low current rectifiers. The pushbutton switch should *not* be omitted as it minimizes junction heating when testing is being done at high voltage, and prevents the possibility of thermal runaway. Tests may be conducted at high temperature by placing the test rectifier(s) in an oven. Junction temperature rise above ambient due to internal heating is generally low enough to be neglected.



REVERSE CURRENT TEST CIRCUIT

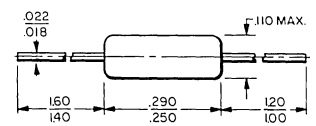
I	- 500 μA MICROAMMETER	R_4	- 100 KΩ
V	- 1000 VOLT VOLTMETER	C_1	- 10 μf - 1 Kv
T_1	- TRIAD R-107A	C_2	- 1 μf - 1 Kv
R_1	- 5KΩ - 2 WATTS	D_1	- 1N4585
R_2	- 100 KΩ	D_2	- 1N4585
R_3	- 10 MEG. Ω	D	- TEST RECTIFIER

4-LAYER DIODE THYRISTORS

- Firing Voltages 20 to 100 volts
- Switching current <125 μA @ 25°C
- ON resistance <2Ω @ 70mA

The ITT diode thyristor is a reliable negative resistance device designed for use in switching circuits. Typical applications include ring counters, matrixes, pulse generators, relay drivers, multivibrators, pulse modulators, and timing circuits.

DIMENSIONS



DO-7

ELECTRICAL SPECIFICATIONS

Type Number	Switching Voltage (V_S)		Reverse Breakdown Voltage (Min.)
	25°C	−40° to 85°C	
1N3831	20±4	14-25	12
1N3832	25±4	19-30	15
1N3833	30±4	23-36	18
1N3834	35±4	28-41	21
1N3835	40±4	32-46	24
1N3836	45±4	37-51	27
1N3837	50±4	41-57	30
1N3838	100±10	80-115	60
1N3839	20±4	14-25	12
1N3840	25±4	19-30	15
1N3841	30±4	23-36	18
1N3842	35±4	28-41	21
1N3843	40±4	32-46	24
1N3844	45±4	37-51	27
1N3845	50±4	41-57	30
1N3846	100±10	80-115	60

MECHANICAL DATA

Case:
Hermetically sealed glass

Finish:
All external surfaces corrosion resistant and leads readily solderable

Leads:
Dumet, tin plated

Weight:
0.135 grams (approx.)

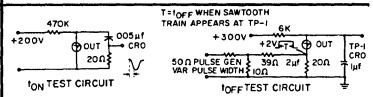
Mounting Position:
Any

Marking:
The symbol for the 4-layer diode is a modified "4". The slant line of the "4" indicates the forward direction of current passing through the device when in the ON state.

ABSOLUTE MAXIMUM RATINGS

CHARACTERISTICS		UNITS
Average Forward Current, 50°C	150	mA
Power Dissipation, 50°C	150	mW
Power-Temperature Derating	1.5	mW/°C
Reverse Breakdown Voltage from T_A = −60 to +125°C	nominal $V_S/2$	min.
Operating and Storage Temperature	−60 to +125	°C

ELECTRICAL CHARACTERISTICS @ 25°C unless otherwise noted

SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS
I_S (forward switching current)			125	μA	
			250	μA	−60 to +125°C
I_H (holding current)	0.5		15	mA	IN3831-38
	14		50	mA	IN3839-46
			40	mA	IN3831-38 @ −40°C
	5			mA	IN3839-46 @ +85°C
I_{ik} (OFF state) (forward leakage current)			5	μA	60% of nom. V_S
V_{ON} (forward voltage drop)			1.2	V	I_f = 70 mA
			2.7	V	I_f = 5A (pulsed)
r_{on} (dynamic forward impedance)			2.0	Ω	I_f = 70 mA
t_{on}		0.1		μsec	
t_{off}		5		μsec	

HOW THE 4-LAYER DIODE OPERATES

The voltage-current characteristic for the 4-layer diode shows three essential operating regions:

I—"off" or high resistance state

II—transition or negative resistance state

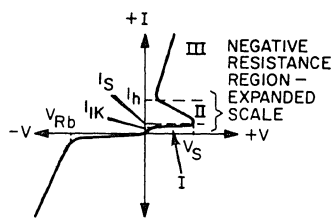
III—"on" or low resistance state

This curve is shown on a very expanded scale (non-linear) for illustration purposes only. Note that as the voltage rises and reaches the switching voltage (V_S), the device begins to switch "on." The current at this point (I_S) is typically several microamperes. The device switches because of an internal feedback mechanism allowing the diode to pass a steadily increasing current as the voltage decreases (negative resistance state, Region II). When "on" (Region III), the 4-layer diode passes a current which is limited principally by the external circuit.

In the "on" state, the device has a dynamic resistance of less than a few ohms and a voltage drop of about one volt. As long as sufficient current is passed by the circuit, the device will remain in the "on" condition. At the point on the curve marked I_h, the circuit is passing just enough current to keep the device in the "on" condition. If the current drops below I_h the diode switches back to the high resistance or "off" condition.

Rate Effect

In its "off" condition the device will pass a capacitive current in response to a sharply rising voltage wave. If the rise rate of this voltage wave is large enough (usually 10 to 100 volts / μS), switching occurs below the DC switching voltage.

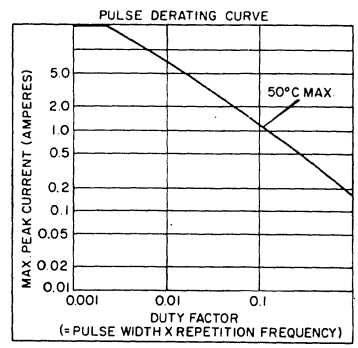


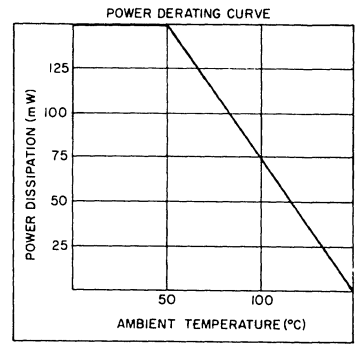
V-I CHARACTERISTICS

TERMS AND SYMBOLS

V_s	Switching Voltage—Closest point to peak voltage in Region II where slope of V-I curve is −330Ω. This definition is adopted because of instrumentation requirements
I_s	Switching Current—Current which flows through the diode at V_S
I_h	Holding Current—The closest point to the minimum voltage in Region II where the slope of the V-I curve is −100Ω
V_h	Holding Voltage—Voltage across the diode at I_h
I_p	Peak Current—Current which the diode can pass when in Region III; duration limited to 50 μs
R_{on}	ON Resistance—Slope of V-I curve measured at currents > I_h
I_{ik}	Leakage Current—Measured in Region I at 60% V_S
V_{rb}	Reverse Breaker Voltage

DERATING CURVES



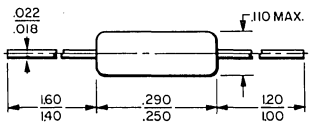


4-LAYER DIODE THYRISTORS

- **Firing Voltages 20 to 200 volts**
- **Switching current <125 μA @ 25°C**
- **ON resistance <2Ω @ 70mA**

The ITT diode thyristor is a reliable negative resistance device designed for use in switching circuits. Typical applications include ring counters, matrixes, pulse generators, relay drivers, multivibrators, pulse modulators, and timing circuits.

DIMENSIONS



DO-7

MECHANICAL DATA

Case:
Hermetically sealed glass
Finish:
All external surfaces corrosion resistant and leads readily solderable
Leads:
Dumet, tin plated
Weight:
0.135 grams (approx.)
Mounting Position:
Any
Marking:
Cathode band
Type number
Manufacturer's Symbol

ELECTRICAL SPECIFICATIONS

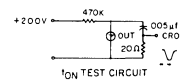
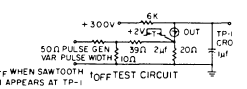
TYPE	Switching Voltage (V_S) (Volts)	Holding Current (I_h) (mA)	Reverse Breakdown Voltage (Min.)
4E20-8	20±4	1-15	12
4E20-28	20±4	14-45	12
4E30-8	30±4	1-15	18
4E30-28	30±4	14-45	18
4E40-8	40±4	1-15	24
4E40-28	40±4	14-45	24
4E50-8	50±4	1-15	30
4E50-28	50±4	14-45	30
4E80-8	80±8V	1-15	48
4E80-28	80±8V	14-45	48
4E100-8	100±10	1-15	60
4E100-28	100±10	14-45	60
4E200-8	200±20 V	1-15	120
4E200-28	200±20 V	14-45	120
Series A (Broad Spec)			
4E20A	20±6	0.5-60	12
4E30A	30±6	0.5-60	18
4E40A	40±6	0.5-60	24
4E50A	50±6	0.5-60	30
4E80A	80±8	0.5-60	48
4E100A	100±10	0.5-60	60
4E200A	200±20	0.5-60	120

ABSOLUTE MAXIMUM RATINGS

CHARACTERISTICS		UNITS
Average Forward Current, 50°C	150	mA
Power Dissipation, 50°C	150	mW
Power-Temperature Derating	1.5	mW/°C
Reverse Breakdown Voltage from T_A = −40 to +70°C	nominal $V_S/2$	min.
Operating and Storage Temperature	−40 to +70	°C

TYPE E 4E20 - 4E200

ELECTRICAL CHARACTERISTICS @ 25°C unless otherwise noted

SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS
I_S (forward switching current)			125 250	μA μA	 −60 to +125°C
I_{ik} (OFF state) (forward leakage current)			15	μA	75% of nom. V_S
V_{ON} (forward voltage drop)			1.4 1.2	V V	I_f = 70 mA@V_S 80, 100, 200 I_f = 70 mA@V_S 20, 30, 40, 50
r_{on} (dynamic forward impedance)			2.0	Ω	I_f = 70 mA
t_{on}		0.1		μsec	
t_{off}		5		μsec	

HOW THE 4-LAYER DIODE OPERATES

The voltage-current characteristic for the 4-layer diode shows three essential operating regions:

I—"off" or high resistance state

II—transition or negative resistance state

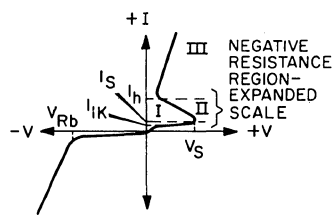
III—"on" or low resistance state

This curve is shown on a very expanded scale (non-linear) for illustration purposes only. Note that as the voltage rises and reaches the switching voltage (V_S), the device begins to switch "on." The current at this point (I_S) is typically several microamperes. The device switches because of an internal feedback mechanism allowing the diode to pass a steadily increasing current as the voltage decreases (negative resistance state, Region II). When "on" (Region III), the 4-layer diode passes a current which is limited principally by the external circuit.

In the "on" state, the device has a dynamic resistance of less than a few ohms and a voltage drop of about one volt. As long as sufficient current is passed by the circuit, the device will remain in the "on" condition. At the point on the curve marked I_h, the circuit is passing just enough current to keep the device in the "on" condition. If the current drops below I_h the diode switches back to the high resistance or "off" condition.

Rate Effect

In its "off" condition the device will pass a capacitive current in response to a sharply rising voltage wave. If the rise rate of this voltage wave is large enough (usually 10 to 100 volts / μS), switching occurs below the DC switching voltage.



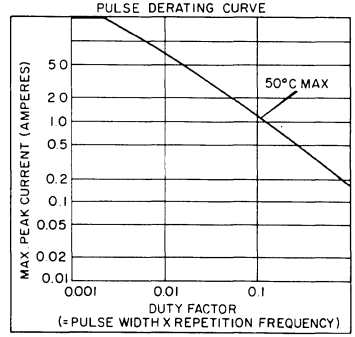
V-I CHARACTERISTICS

TERMS AND SYMBOLS

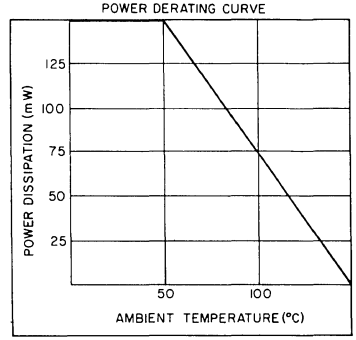
- V_s Switching Voltage—Closest point to peak voltage in Region II where slope of V-I curve is −330Ω. This definition is adopted because of instrumentation requirements
- I_s Switching Current—Current which flows through the diode at V_S
- I_h Holding Current—The closest point to the minimum voltage in Region II where the slope of the V-I curve is −100Ω
- V_h Holding Voltage—Voltage across the diode at I_h
- I_p Peak Current—Current which the diode can pass when in Region III; duration limited to 50 μs
- R_{on} ON Resistance—Slope of V-I curve measured at currents > I_h
- I_{ik} Leakage Current—Measured in Region I at 75% V_S
- V_{rb} Reverse Breaker Voltage

DERATING CURVES

PULSE DERATING CURVE



POWER DERATING CURVE

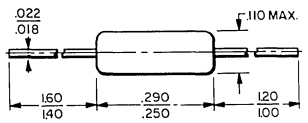


4-LAYER DIODE THYRISTORS

- **Firing Voltages 20 to 200 volts**
- **Switching current <125 μA @ 25°C**
- **ON resistance <2Ω @ 70mA**

The ITT diode thyristor is a reliable negative resistance device designed for use in switching circuits. Typical applications include ring counters, matrices, pulse generators, relay drivers, multivibrators, pulse modulators, and timing circuits.

DIMENSIONS



DO-7

MECHANICAL DATA

Case:
Hermetically sealed glass
Finish:
All external surfaces corrosion resistant and leads readily solderable
Leads:
Dumet, tin plated
Weight:
0.135 grams (approx.)
Mounting Position:
Any
Marking:

Cathode band
Type number
Manufacturer's Symbol

ELECTRICAL SPECIFICATIONS

Mil-Line Series for extended temperature ranges

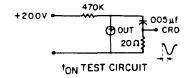
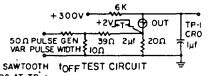
TYPE	Switching Voltage (V_S)		Holding Current (I_h) (mA) 25°C	Reverse Breakdown Voltage (Min.) −60 to 125°C
	25°C	−60 to 125°C		
4E20M-8	20±4	14-25	1-15	10
4E20M-28	20±4	14-25	14-45	10
4E30M-8	30±4	23-36	1-15	15
4E30M-28	30±4	23-36	14-45	15
4E40M-8	40±4	32-46	1-15	20
4E40M-28	40±4	32-46	14-45	20
4E50M-8	50±4	41-57	1-15	25
4E50M-28	50±4	41-57	14-45	25
4E30M-8	80±8	68-92	1-15	40
4E30M-28	80±8	68-92	14-45	40
4E100M-8	100±10	80-115	1-15	50
4E100M-28	100±10	80-115	14-45	50
4E200M-8	200±20	160-230	1-15	100
4E200M-28	200±20	160-230	14-45	100

ABSOLUTE MAXIMUM RATINGS

CHARACTERISTICS		UNITS
Average Forward Current, 50°C	150	mA
Power Dissipation, 50°C	150	mW
Power-Temperature Derating	1.5	mW/°C
Reverse Breakdown Voltage from T_A = −60 to +125°C	nominal $V_S/2$	min.
Operating and Storage Temperature	−60 to +125	°C

TYPE E 4E20M - 4E200M

ELECTRICAL CHARACTERISTICS @ 25°C unless otherwise noted

SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS
I_S (forward switching current)			125 250	μA μA	−60 to +125°C
I_{ik} (OFF state) (forward leakage current)			15	μA	75% of nom. V_S
V_{ON} (forward voltage drop)			1.4 1.2	V V	I_f = 70 mA@V_S 80, 100, 200 I_f = 70 mA@V_S 20, 30, 40, 50
r_{on} (dynamic forward impedance)			2.0	Ω	I_f = 70 mA
t_{on}		0.1		μsec	 t_{ON} TEST CIRCUIT
t_{off}		5		μsec	 $T=t_{OFF}$ WHEN SAWTOOTH TRAIN APPEARS AT TP-1 t_{OFF} TEST CIRCUIT

HOW THE 4-LAYER DIODE OPERATES

The voltage-current characteristic for the 4-layer diode shows three essential operating regions:

I—"off" or high resistance state

II—transition or negative resistance state

III—"on" or low resistance state

This curve is shown on a very expanded scale (non-linear) for illustration purposes only. Note that as the voltage rises and reaches the switching voltage (V_S), the device begins to switch "on." The current at this point (I_S) is typically several microamperes. The device switches because of an internal feedback mechanism allowing the diode to pass a steadily increasing current as the voltage decreases (negative resistance state, Region II). When "on" (Region III), the 4-layer diode passes a current which is limited principally by the external circuit.

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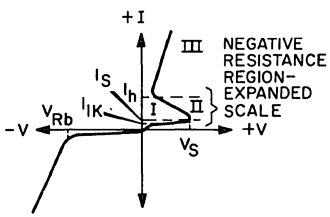
Rate Effect

In its "off" condition the device will pass a capacitive current in response to a sharply rising voltage wave. If the rise rate of this voltage wave is large enough (usually 10 to 100 volts / μS), switching occurs below the DC switching voltage.

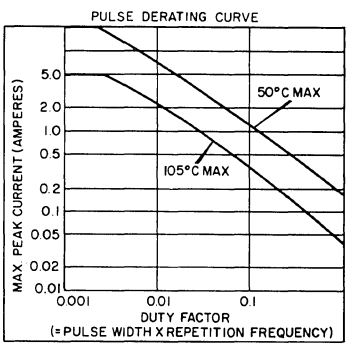


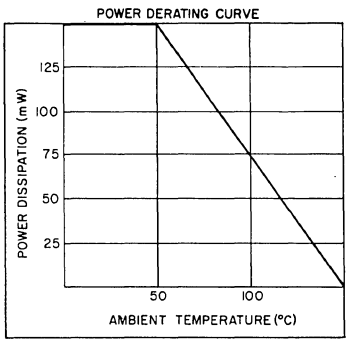
V-I CHARACTERISTICS

TERMS AND SYMBOLS

- V_s Switching Voltage—Closest point to p\ voltage in Region II where slope of \ curve is −330Ω. This definition is adopte because of instrumentation requirements
- I_s Switching Current—Current which flows through the diode at V_S
- I_h Holding Current—The closest point to the minimum voltage in Region II where the slope of the V-I curve is −100Ω
- V_h Holding Voltage—Voltage across the diode at I_h
- I_p Peak Current—Current which the diode can pass when in Region III; duration limited to 50 μs
- R_{on} ON Resistance—Slope of V-I curve measured at currents > I_h
- I_{ik} Leakage Current—Measured in Region I at 75% V_S
- V_{rb} Reverse Breaker Voltage

DERATING CURVES





TWENTY-FOUR CIRCUIT APPLICATIONS FOR ITT 4-LAYER DIODES

THEORY OF OPERATION

The ITT Semiconductor Four-Layer Diode is a two-terminal semiconductor switch, sometimes referred to as a negative-resistance diode. These PNPN silicon devices are useful in many applications including pulse generators, oscillators, telephone switching, sweep generators, and multivibrators.

The diode has two stable states; the ON or low impedance state, and the OFF or high impedance state. To turn the device ON, voltage across the terminals must exceed the switching voltage (V_s). The device can be turned OFF by reducing the current through the device below the holding current (I_h).

Figure 1

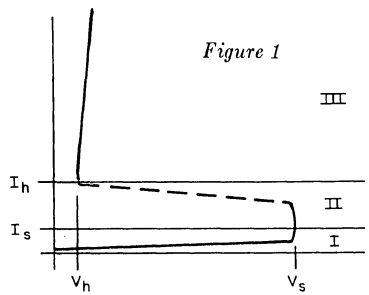


Figure 1 is the V-I characteristic of a typical device. V_s is the point at which the device breaks down and switches to the ON state where current is limited only by the external circuit impedance.

I_h is the minimum current that must be passed through the diode to keep it in the ON state. If the current drops below this value the diode will switch to the OFF state.

Figure 2A

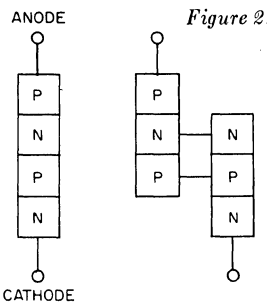
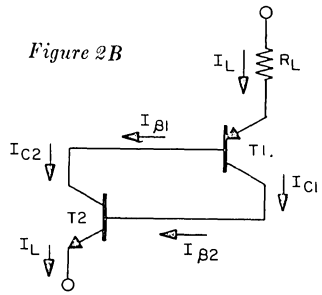


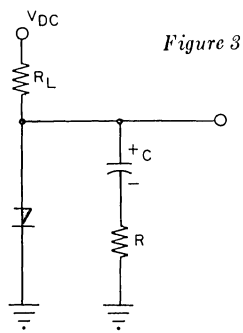
Figure 2B



The PNPN diode can be thought of as a complimentary pair of transistors, one a PNP and the other an NPN as shown in Figure 2A. Figure 2B shows the two transistors as they would appear schematically. The collector of T_2 drives the base of T_1 giving rise to a positive feedback loop with a gain of B_1B_2. As long as B_1B_2 is less than 1 the equivalent circuit is stable with the upper and lower PN junctions biased forward and the middle junction reversed biased. In this condition only a small leakage current flows.

The diode will remain in this condition until either the temperature or the anode voltage is increased to a point where $B_1B_2 = 1$. At this point, the middle junction breaks down and the circuit becomes regenerative. This occurs because the collector of each transistor supplies current to the base of the complimentary transistor in the equivalent circuit and their Betas are current dependent. As soon as they reach unity the device effectively "runs away" or "fires" and the current through the circuit is limited only by external impedance.

Figure 3

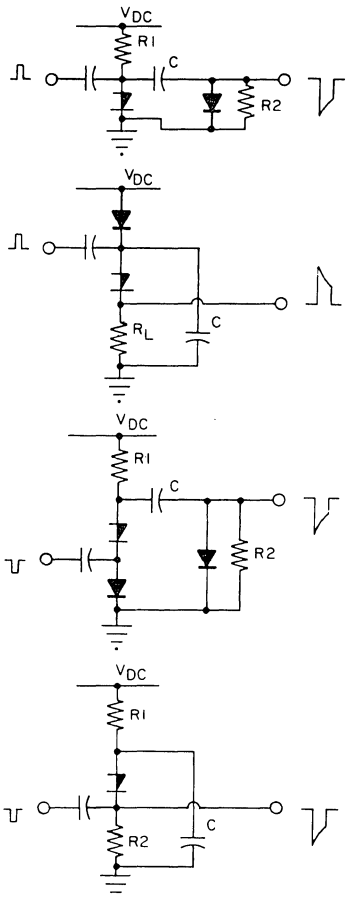


**Application notes will be found in the last pages of this section.

CIRCUITS

Relaxation Oscillator

Figure 3 illustrates a circuit used for oscillator, sweep generator, and timing applications. The output is a saw-tooth voltage the amplitude of which is dependent on the diode V_s. Frequency is dependent upon the $R_L C$ time constant and the supply voltage. The supply voltage should be chosen so that the charging of C is done in the linear portion of the curve. When C reaches V_s the diode breaks down and conducts. C rapidly discharges through the diode. R_L should be large enough so that it will not pass I_h or the diode will remain in the ON condition after C has discharged. With C discharged the diode turns OFF and C commences to charge again. R_L must be able to pass the switching current (I_s) when C reaches V_s and the diode fires again.



Triggered Pulse Generators

These circuits are used mainly for generating or amplifying pulses and for triggering purposes. They are similar to Figure 3 except that the switching voltage of the diode is greater than the supply voltage. Four variations, with their input and output pulses, are shown in Figure 4. A pulse, large enough to break down the diode, is capacitively coupled either positive to the anode or negative to the cathode. The conventional diode is used to present a high impedance to the input pulse.

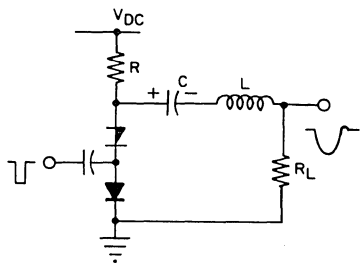
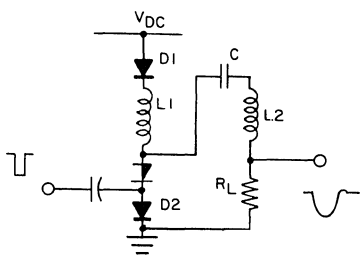


Figure 5

L-C Pulse Generators

As with the circuits in foregoing section, those in this section also require a pulse to fire the diode. V_s of the diode is greater than the supply voltage. In Figure 5, a negative pulse is applied to the cathode which breaks down the diode. C, which was charged to V_{DC} through R, discharges through the diode, L, and R_L. This is a resonant circuit and the wave shape across R_L is a half sinusoid. When the current goes through zero, the voltage across the diode becomes negative, turning it OFF. A small positive output will occur due to the pulse recovery current through the diode.

Figure 6



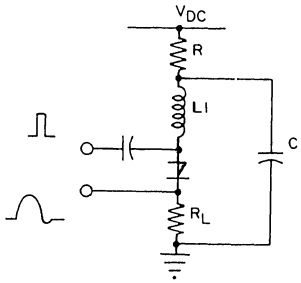


Figure 7

This type of generator does not depend on R being large enough not to pass I_h but rather on the fact that ringing of the L-C loop turns OFF the diode. During the OFF half cycle C charges to V_{DC} but in the opposite polarity. With the completion of the output pulse and the cessation of ringing, C begins to recharge toward the power supply voltage and polarity. Figures 6 and 7 illustrate the same principle but with a resonant charging circuit. C may charge to approximately twice the supply voltage if the circuit Q is high. The resistance of L must be large enough to keep the current through the four-layer diode below its rated maximum. The anode of the diode must be kept negative long enough to turn completely OFF, otherwise the diode will turn back ON when the anode goes positive. This requirement limits the maximum operating repetition rate.

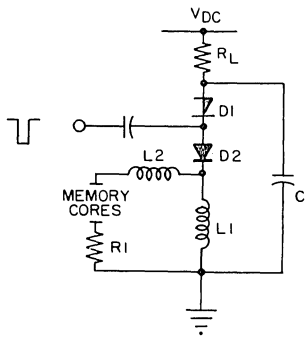


Figure 8

Magnetic Memory Driver Circuits

The purpose of a magnetic memory driving circuit is to provide a current wave form which reads the memory and then restores (writes) the initial flux condition. In Figure 8, the V_s of the four-layer diode is greater than V_{DC}. C charges to V_{DC} through R_L When a negative pulse of the proper magnitude is coupled to the cathode, the four-layer diode (D_1) conducts. R_L is made large enough so that it will not deliver the minimum I_h. C discharges through the four-layer diode (D_1) the conventional diode (D_2), and the inductive load. C must be large enough to supply the "read" peak current. The shape of the curve is dependent on the inductances and R_1. The R_LC product must be selected so that C charges in less time than the time from the end of the "read" pulse to the beginning of the next complete cycle.

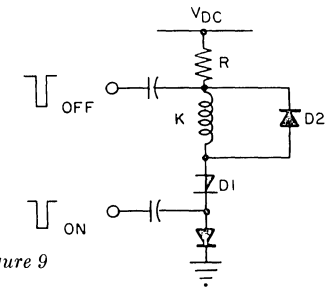


Figure 9

Relay Drivers

In Figure 9, V_s is greater than V_{DC}. A negative pulse on the cathode turns D_1 ON. It remains in this state until it is pulsed OFF by a negative pulse on the anode. This is a typical relay driver application. D_2 prevents excessive spiking caused by the relay inductance.

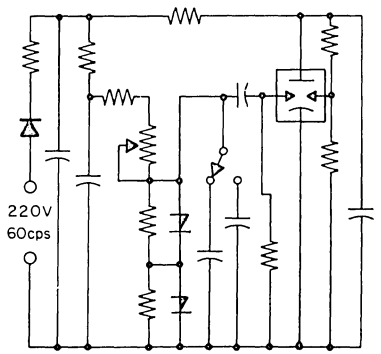


Figure 10

Stroboscope

In Figure 10, the four-layer diodes replace thyratrons as triggers to activate a stroboscope flash tube. The diodes form a relaxation oscillator delivering pulses up to 150V at a few hundred per second depending on the circuit constants. Because of the pulse magnitude two diodes are used in series with equalizing resistors across them.

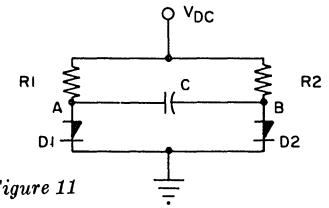


Figure 11

A-Stable Circuit

V_{DC} is greater than V_s of both diodes in Figure 11. When power is applied, one of the diodes will conduct. Let it be assumed that D_1 fires first. Point A will go approximately to ground potential and the current through R_1 will be greater than I_h. The capacitor C will begin to charge through R_2 and D_1 to ground. When the voltage at B exceeds the breakdown potential of D_2, it will conduct and point B will go to ground. Since the capacitor can not charge instantly, point A will drop approximately V_s volts. This puts a negative voltage at A, which if kept there until the turn OFF potential of D_1 is reached, will prevent it from switching back until the voltage at A reaches V_s. C therefore charges through R_1. The circuit oscillates back and forth from D_1 to D_2 with the frequency dependent on R_1C and R_2C and on V_{DC} and the switching voltage of the diodes.

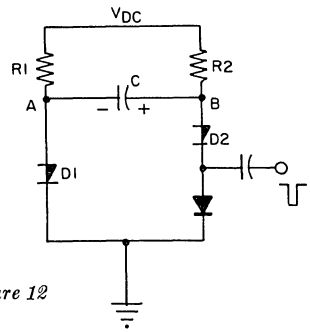


Figure 12

Monostable Multivibrator

If diode D_1 in Figure 12 is selected so that its switching voltage is less than V_{DC}, and diode D_2's is greater than V_{DC}, diode D_1 will normally be in the ON condition and D_2 will be OFF. Capacitor C will charge through R_2. When D_2 is pulsed ON, D_1 will turn OFF due to the commutating action of C. The voltage at point A will then start rising as C charges through R_1 and D_2. When the voltage at point A reaches the switchover voltage of D_1 it will turn ON and D_2 will turn OFF until another pulse is received. Frequency is determined by R_1C, V_{DC}, and V_s of diode D_1.

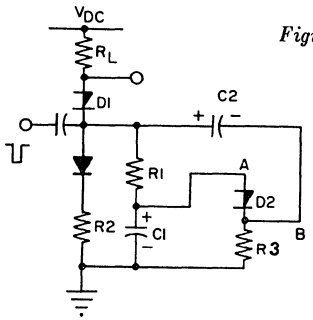


Figure 13

A modification of the gate circuit where both diodes are in the OFF state until a pulse is applied is shown in Figure 13. The V_s of D_1 is slightly higher than V_{DC}. A pulse of current is applied through R_L which turns D_1 ON. C_2 charges through D_1 and R_2 to V_{DC}. C_1 charges through R_1 and D_1 toward V_{DC} also. When the voltage at point A reaches V_s of D_2, it will commence to conduct. The voltage rise at B is commutated back to D_1, turning it OFF, which in turn, turns OFF D_2.

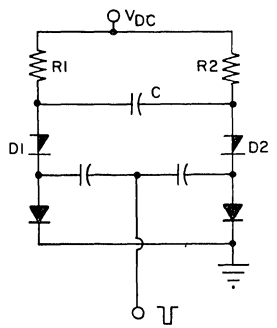


Figure 14

Bi-Stable Multivibrator Flip-Flop

The V_s of both diodes are chosen so that they are greater than V_{DC} in Figure 14. Whichever diode is ON, it remains in that condition until a trigger pulse arrives turning OFF the diode which was ON and turning ON the previously OFF diode by the commutating action of C.

By interchanging one 4-layer diode with its series cathode diode, the circuit will become sensitive to the polarity of the pulses. The circuit will then switchover only when the polarity of the trigger pulse reverses. This is shown in Figure 15. Diode 1 triggers on negative pulses only and diode 2 on positive pulses. Therefore, a positive pulse keeps branch B ON and a negative pulse keeps branch A ON.

Figure 15

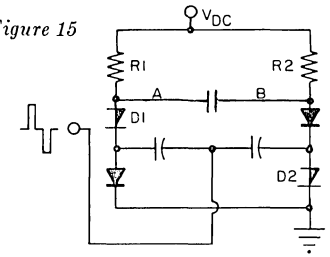
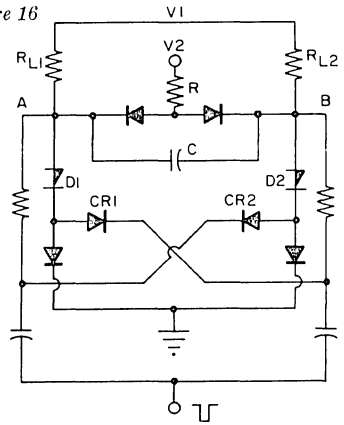
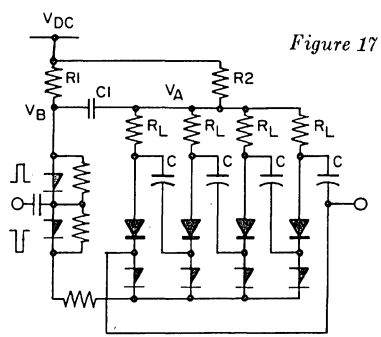


Figure 16



A different steering circuit is shown in Figure 16. Assume that D_1 is ON. Point A will be approximately at ground potential and point B at V_1. When a negative pulse is applied it is blocked by CR_1 but passes through CR_2, causing switchover to take place. Current from V_2 passes through R and D_2 to ground. The principal source of current for the conducting branch is V_2. The R_L's are needed to maintain a voltage of less than V_s across the OFF diode.

Figure 17



Ring Counters

The basic requirement of a ring counter is to turn one stage at a time ON in a simple progression. Each time a trigger pulse is applied, the ON stage will advance one stage. The circuit forms a closed loop, or ring, so that when the final stage has been activated the next pulse will move the ON condition back to the first stage where the cycle begins over again. In Figure 17, one stage will turn ON as soon as power is applied. The commutating capacitor C between the ON stage and the next successive stage charges through R_L and the ON 4-layer diode to V_A, which is less than the V_s of the diodes and keeps them from turning ON. A trigger pulse, either positive or negative, causes V_B to drop almost to ground potential, which in turn, causes V_A to drop at the same time due to the coupling action of C_1. Since R_1 is large enough so that a current of less than I_h flows through the trigger diodes, the pulse is only momentary. The drop in voltage at A turns OFF the ON diode. At the same time C_1 begins to charge and the voltage at A rises again.

The voltage at the high end of the charged commutating capacitor C adds to V_A causing the next stage to fire. The repetition rate of the output pulses equals the rate of the trigger pulses divided by the number of stages.

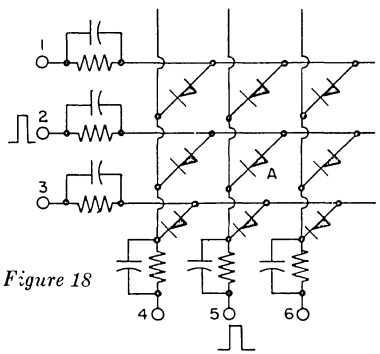


Figure 18

Telephone Switching

When trigger signals of the polarity shown in Figure 18 are simultaneously applied to the lines, one of positive polarity to lines 1, 2, or 3, and the other of negative polarity to lines 4, 5, or 6, two of the lines will be connected. If triggers are applied to lines 2 and 5 as shown, the 4-layer diode A will conduct connecting them together. The series resistors allow a current greater than I_h to flow, thus keeping the diode in the ON state. To open the circuit, a contact is opened to interrupt the flow of current through the diode which will then revert to its OFF condition.

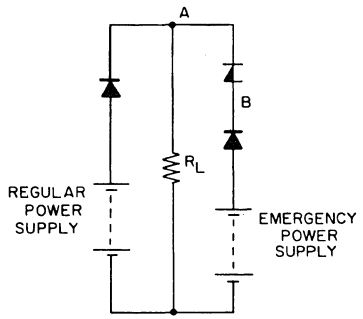


Figure 19

Emergency Power Transfer

In the normal state, the 4-layer diode in Figure 19 is OFF and the regular power supply is the source of power for the load R_L. If the supply voltage should fall off for any reason, the voltage at point A will drop. If this change in voltage is sufficient to cause the potential from B to A to exceed the diode V_s, it will turn ON and the emergency power supply will provide power to the load until the condition is corrected.

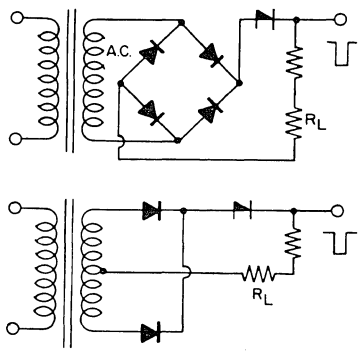


Figure 20

Rectifier Control Circuits

Figure 20 illustrates a method for controlling the power output of a rectifier by varying the point at which a 4-layer diode is triggered. Pulses may be applied at any phase angle from the start of the input waveform (100% power) to 180° (zero power).

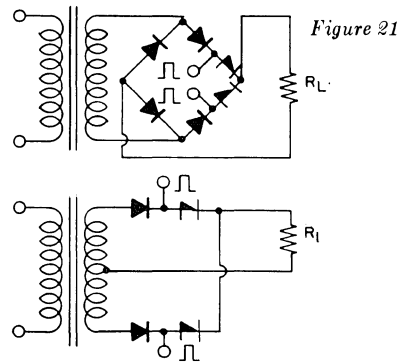


Figure 21

In Figure 21, succeeding half cycles can have different firing angles since there are two control diodes, one for each leg of the rectifier circuit.

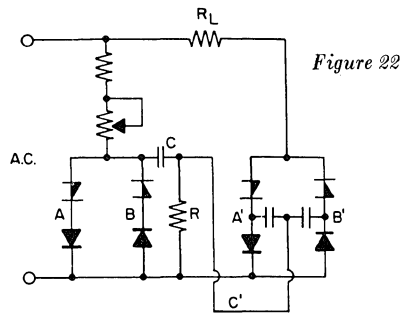


Figure 22

AC Control Circuits

The circuit in Figure 22 is useful for the control of AC power in such applications as light dimmers and motor controls. The trigger portion is composed of two back-to-back relaxation oscillators with an adjustable resistor controlling the time at which they fire the control diodes and thus the amount of current through the load.

The load resistor of the oscillator and C set up the time constant to fire the trigger diodes at approximately 90° in each half cycle. When a positive input cycle occurs the diode A will break down at approximately 90°. The charged capacitor C will discharge through diode A with the result that a negative pulse will appear at point C_1.

This pulse will turn ON control diode A_1 which will allow current to flow until the half cycle is completed. Both diodes will then turn OFF since the current through them will drop below their holding current. This cycle is repeated during the negative portion of the input waveform.

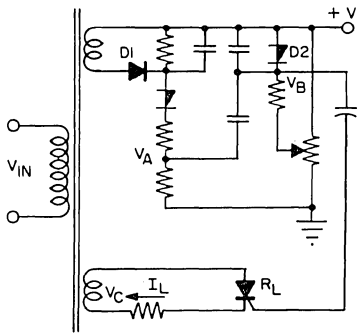


Figure 23

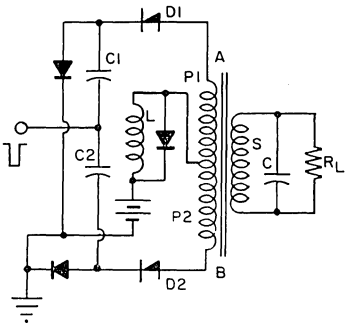


Figure 24

SCR Phasing Circuit

Diode 1 and 2 are both designed into relaxation oscillator circuits in Figure 23. The diode 1 circuit has a frequency of just under 60 cycles per second. The half-wave supply circuit at its anode causes the frequency of the oscillator to be synchronized with the line frequency. The output at V_A is a sawtooth which is coupled to the cathode of D_2. It is superimposed on a DC value set by the potentiometer in the cathode of D_2. As the voltage across D_2 is increased by decreasing the cathode potential, the negative peak of the waveform from D_1 will exceed V_s of D_2 putting it into oscillation at a frequency much greater than that of D_1. This signal is fed to the gate of the SCR which is fired by the steep wave front at the start of oscillations. The timing of the conduction of the SCR is controlled by the setting of the potentiometer.

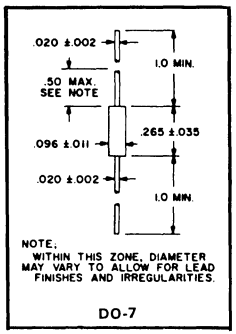
Inverter Circuits

The circuit in Figure 24 is a typical power inverter used to convert DC power to AC power over a range of frequency from 60 to a few thousand cycles. When power is applied, one of the 4-layer diodes begins to conduct. Assume this to be D_1. The battery supplies current through the coil L, primary 1 and D_1. The reflected load limits the current through D_1.

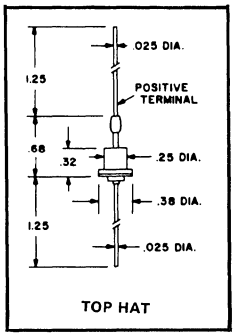
When a negative trigger pulse is applied D_2 will conduct. The commutating capacitor C which is reflected into the primary from across R_L will cause point A to go negative thus turning OFF D_1. L smooths the current during switching. The following negative trigger pulse turns D_1 ON again and C turns D_2 OFF. This completes one cycle.

The switchover voltage of the diodes must be greater than $2XV_{DC}$ and capacitor C must be big enough so that when reflected back into the primary it can turn OFF the diode which was ON just prior to the triggering pulse. The capacitor can be across the primary or the secondary.

THYRISTOR DIODES



DO-7



TOP HAT

DO-7 PACKAGE

TYPE	Switching Voltage (V_S) (Volts) 25°C	−40 to 85°C	Holding Current (I_h) (Milliamps) 25°C	−40°C	Reverse Breakdown 25°C	Capacitance (Typical) 0V Bias
1N3831	20 ± 4	14-25	0.5-15	40 max	12v min	80 pf
1N3832	25 ± 4	19-30	0.5-15	40 max	15v min	70 pf
1N3833	30 ± 4	23-36	0.5-15	40 max	18v min	60 pf
1N3834	35 ± 4	28-41	0.5-15	40 max	21v min	50 pf
1N3835	40 ± 4	32-46	0.5-15	40 max	24v min	45 pf
1N3836	45 ± 4	37-51	0.5-15	40 max	27v min	45 pf
1N3837	50 ± 4	41-57	0.5-15	40 max	30v min	40 pf
1N3838	100 ± 10	80-115	0.5-15	40 max	60v min	30 pf

TYPE	Switching Voltage (V_S) (Volts) 25°C	−40 to 58°C	Holding Current (I_h) (Milliamps) 25°C	85°C	Reverse Breakdown 25°C	Capacitance (Typical) 0V Bias
1N3839	20 ± 4	14-25	14-50	5 min	12v min	80 pf
1N3840	25 ± 4	19-30	14-50	5 min	15v min	70 pf
1N3841	30 ± 4	23-36	14-50	5 min	18v min	60 pf
1N3842	35 ± 4	24-81	14-50	5 min	21v min	50 pf
1N3843	40 ± 4	32-46	14-50	5 min	24v min	45 pf
1N3844	45 ± 4	37-51	14-50	5 min	27v min	45 pf
1N3845	50 ± 4	41-57	14-50	5 min	30v min	40 pf
1N3846	100 ± 10	80-115	14-50	5 min	60v min	30 pf

Commercial Series

TYPE	Switching Voltage (V_S) (Volts)	Holding Current (I_h) (mA)
4E20-8	20 ± 4	1-15
4E20-28	20 ± 4	14-45
4E30-8	30 ± 4	1-15
4E30-28	30 ± 4	14-45
4E40-8	40 ± 4	1-15
4E40-28	40 ± 4	14-45
4E50-8	50 ± 4	1-15
4E50-28	50 ± 4	14-45
4E100-8	100 ± 10	1-15
4E100-28	100 ± 10	14-45
4E200-8	200 ± 20	1-15
4E200-28	200 ± 20	14-15

Mil-Line Series for extended temperature ranges

TYPE	Switching Voltage (V_S) 25°C	−60 to 125°C	Holding Current (I_h) (mA)
4E20M-8	20 ± 4	14-25	1-15
4E20M-28	20 ± 4	14-25	14-45
4E30M-8	30 ± 4	23-36	1-15
4E30M-28	30 ± 4	23-36	14-45
4E40M-8	40 ± 4	32-46	1-15
4E40M-28	40 ± 4	32-46	14-45
4E50M-8	50 ± 4	41-57	1-15
4E50M-28	50 ± 4	41-57	14-45
4E100M-8	100 ± 10	80-115	1-15
4E100M-28	100 ± 10	80-115	14-45
4E200M-8	200 ± 20	160-230	1-15
4E200M-28	200 ± 20	160-230	14-45

Series A (Broad Spec)

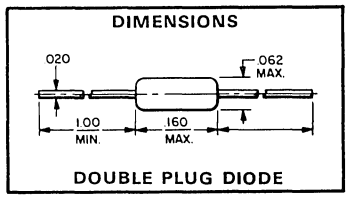
TYPE	Switching Voltage (V_S) (Volts)	Holding Current (I_h) (mA)
4E20A	20 ± 6	0.5-60
4E30A	30 ± 6	0.5-60
4E40A	40 ± 6	0.5-60
4E50A	50 ± 6	0.5-60

TOP-HAT PACKAGE—TYPE J

TYPE	Switching Voltage (V_S) (Volts)	Holding Current (I_h) (mA)
4J50-5	50 ± 5	1-10
4J50-25	50 ± 5	9-45
4J100-5	100 ± 10	1-10
4J100-25	100 ± 10	9-45
4J200-5	200 ± 20	1-10
4J200-25	200 ± 20	9-45

Current Carrying Capacity: 300 mA steady dc.
Maximum peak current rating 20 amperes — dependent on duty factor, repetition rate, pulse duration, ambient temperature.

SILICON PLANAR EPITAXIAL TUNER DIODE



The ITT silicon planar epitaxial tuner diode is intended for television receiver tuner applications where three or four units will provide complete coverage of the VHF broadcast bands respectively. The high guaranteed capacitance ratio of these diodes allows design of electronically tuned FM tuners for 12V operation.

ABSOLUTE MAXIMUM RATINGS

		UNITS
Power dissipation @ 50°C	150	mW
Operating temperature range	0 to 90	°C
Storage temperature range	0 to 100	°C
Peak reverse voltage	30	Volts

ELECTRICAL CHARACTERISTICS (T_j = 25°C unless otherwise specified)

SYMBOL		ITT 109			UNITS	CONDITIONS
		MIN.	TYP.	MAX.		
C_J			30.0		pF	V_R = 3V
		4.2		6.5	pF	V_R = 25V
$\frac{C(V=3V)}{C(V=25V)}$		5				
R_S			0.5		Ohms	V_R = 3V, f = 100 MHz
Q		200	280			V_R = 3V, f = 47MHz
		90				V_R = 3V, f = 100MHz
		55				V_R = 3V, f = 170MHz
L_S			2.5 nH			
I_R				0.5	μA	V_R = 28V

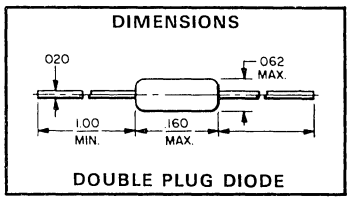
NOTES:

The error of matching in capacitance within a matched set in the voltage range V = 3 . . . 25 Volts is ± 1.5%.

These diodes are available on request in matched sets of any desired capacitance tolerance between 0 and 25 Volts for special applications.

SILICON PLANAR EPITAXIAL TUNER DIODES (LOW INDUCTANCE)

ITT silicon planar epitaxial tuner diodes are intended for television receiver tuner applications where three or four units will provide complete coverage of the VHF and UHF broadcast bands respectively. The high guaranteed capacitance ratio of these diodes allows design of electronically tuned FM tuners for 12V operation.



ABSOLUTE MAXIMUM RATINGS

CHARACTERISTICS		UNITS
Power dissipation @ 50°C	150	mW
Operating temperature range	0 to 90	°C
Storage temperature range	0 to 100	°C
Peak reverse voltage	30	Volts
Soldering temperature (5 secs. at body of diode package)	260	°C

ELECTRICAL CHARACTERISTICS ($T_j = 25°C$ unless otherwise specified)

SYMBOL	ITT 141			ITT 142			UNITS	CONDITIONS
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.		
C_J		11			12		pF	$V_R = 3V$
		2.2	2.5	2.0	2.5	3.0	pF	$V_R = 25V$
$\frac{C_{3.0V}}{C_{25V}}$	4.5	4.8	5.5 5.2	4.0	4.8	6.0		
R_S		0.5			1.0		Ohms	$V_R = 3V$, $f \approx 330$ MHz
Q	300			160				$V_R = 3V$, f=47MHz
				80				$V_R = 3V$, f=100MHz
	80			50				$V_R = 3V$, f=170MHz
	30							$V_R = 3V$, f=470MHz
f_c	20			10			GHz	$V_R = 3V$, Q = 1.0
f_o	2.5			2.2			GHz	$V_R = 25V$
L_S		2.5			2.5		nH	At body of diode package
V_{BR}	30			30			Volts	
I_R			5.0			5.0	μA	$V_R = 28V$

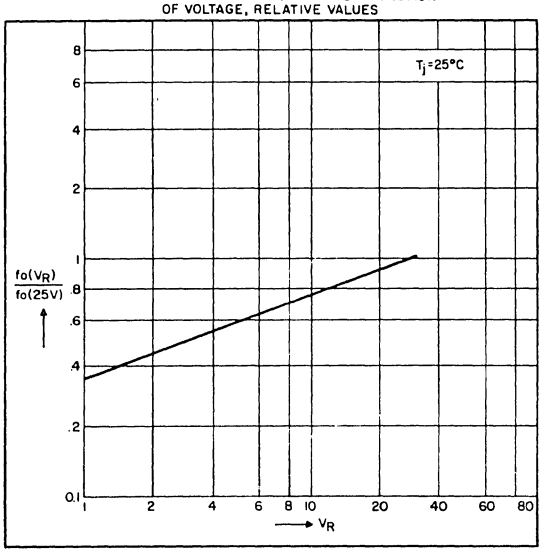
NOTES:

The error of matching in capacitance within a matched set in the voltage range V = 3 . . . 25 Volts is ± 1.5%.

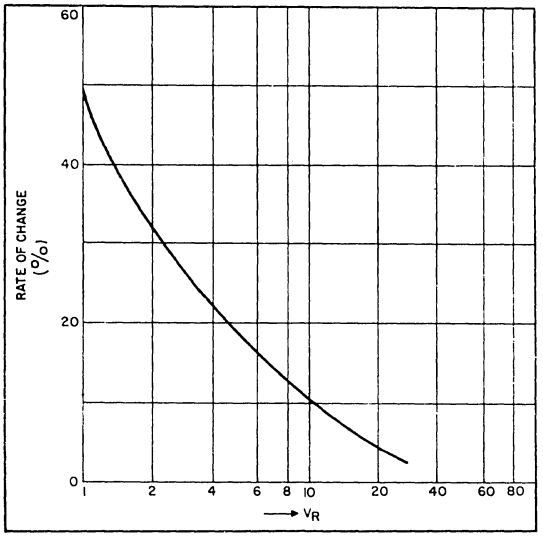
These diodes are available on request in matched sets of any desired capacitance tolerance between 0 and 25 Volts for special applications.

TYPICAL CHARACTERISTICS

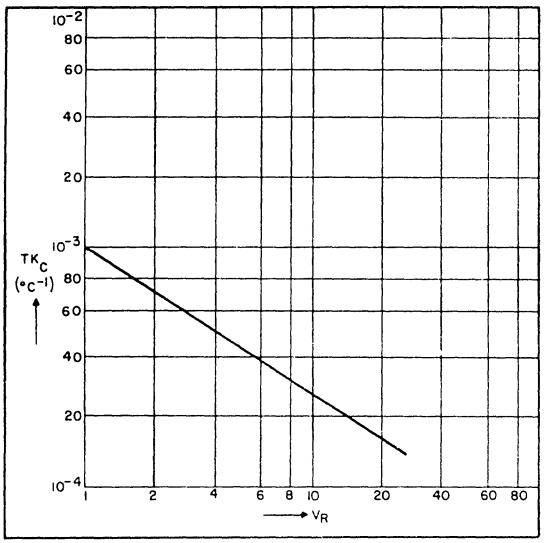
SERIES RESONANCE FREQUENCY AS A FUNCTION OF VOLTAGE, RELATIVE VALUES



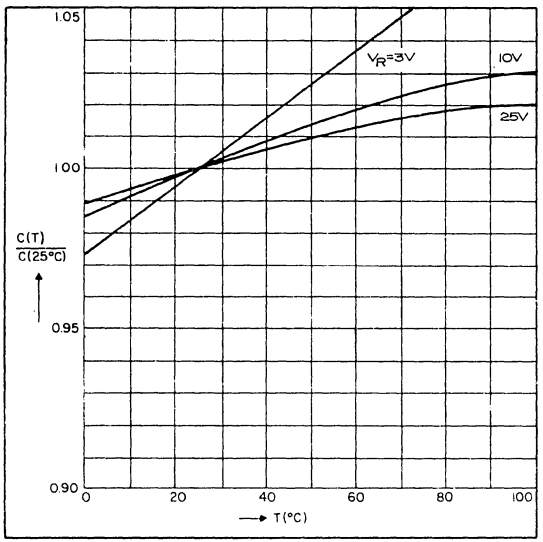
RATE OF CHANGE OF CAPACITANCE VS. VOLTAGE.



TEMPERATURE COEFFICIENT AS A FUNCTION OF VOLTAGE, RELATIVE VALUES

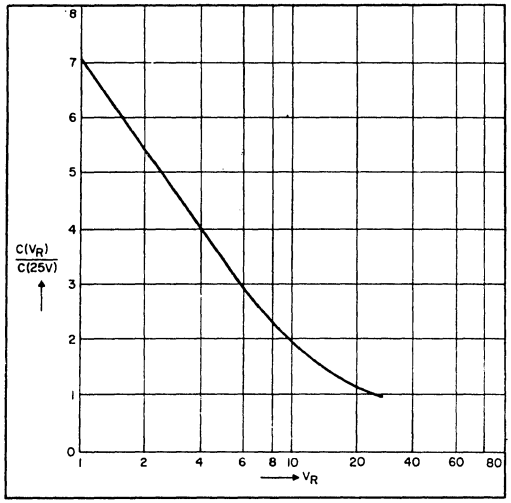


CAPACITANCE AS A FUNCTION OF TEMPERATURE, RELATIVE VALUES

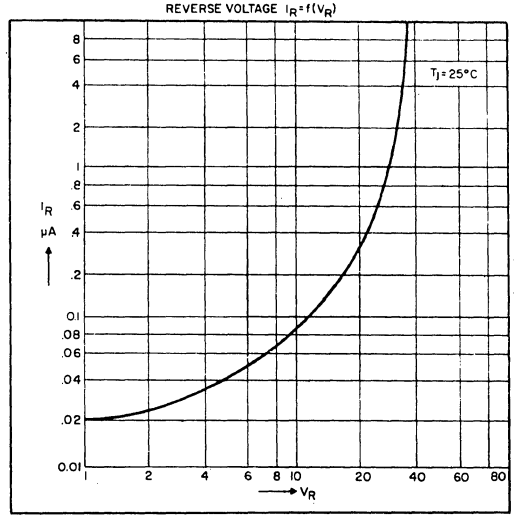


TYPICAL CHARACTERISTICS, continued

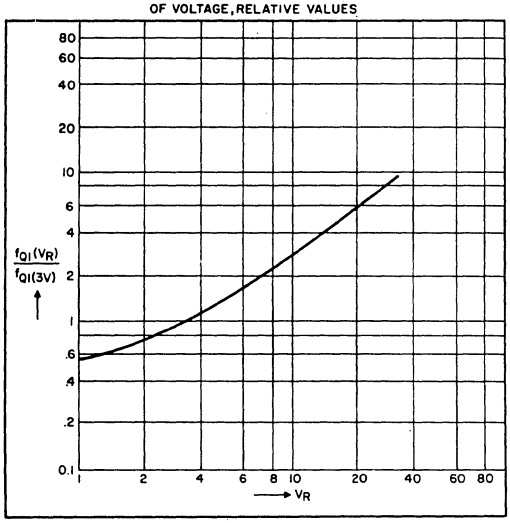
JUNCTION CAPACITANCE (C) AS A FUNCTION OF VOLTAGE, RELATIVE VALUES



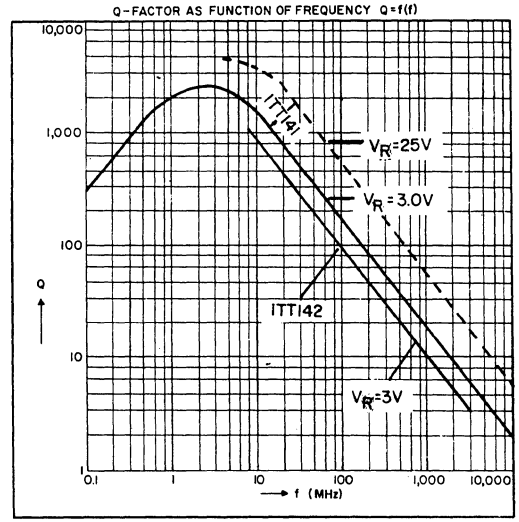
REVERSE CURRENT AS FUNCTION OF REVERSE VOLTAGE $I_R = f(V_R)$



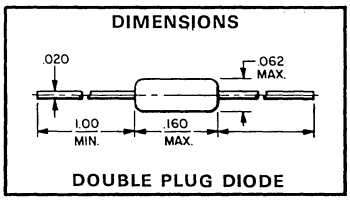
CUTOFF FREQUENCY (fc) AS A FUNCTION OF VOLTAGE, RELATIVE VALUES



Q-FACTOR AS FUNCTION OF FREQUENCY $Q = f(f)$



SILICON PLANAR EPITAXIAL CAPACITANCE DIODE



The ITT-210 is an improved variable capacitance diode intended for television receiver Automatic Frequency Control and other tuning applications between 1 and 1,000 MHz.

ABSOLUTE MAXIMUM RATINGS

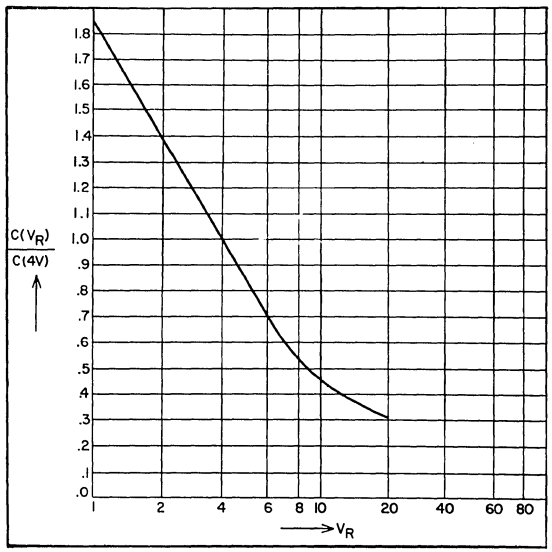
CHARACTERISTICS		UNITS
Reverse Voltage Breakdown @ 5μa	20	Volts
Power Dissipation @ 50°C	150	MW
Operating Temperature Range	0 to 100	°C
Storage Temperature Range	−50 to + 150	°C

ELECTRICAL CHARACTERISTICS @ 25°C unless otherwise noted.

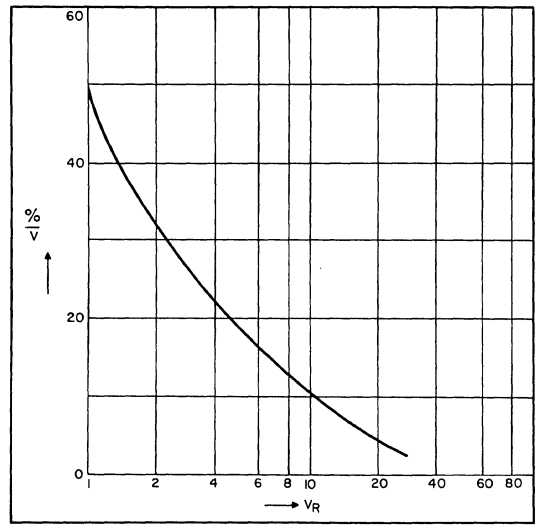
SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS
C	8	20	12	pF	$V_r = 1.0V$
		10		pF	$V_r = 4V$
		8.3		pF	$V_r = 6V$
		5		pF	$V_r = 10V$
Rs		1.0		ohms	F = 30 MHz $V_r = 2V$
Q		540			F = 30 MHz $V_r = 5V$
V_F		.85	1.5	V.	$I_F = 60mA$

TYPICAL CHARACTERISTICS

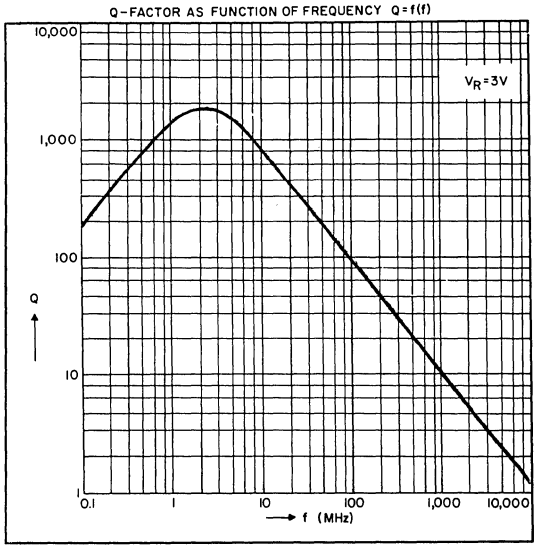
JUNCTION CAPACITANCE (C) AS A FUNCTION OF VOLTAGE, RELATIVE VALUES



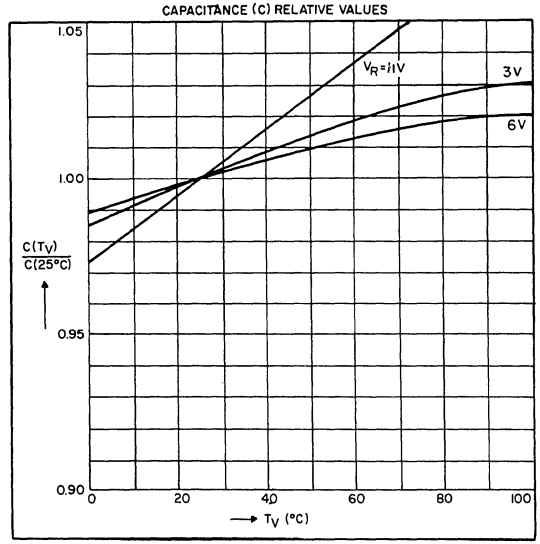
RATE OF CHANGE OF CAPACITANCE VS. VOLTAGE.



Q-FACTOR AS FUNCTION OF FREQUENCY Q=f(f)



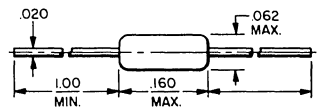
TEMPERATURE AS FUNCTION OF JUNCTION CAPACITANCE (C) RELATIVE VALUES



UHF/VHF WAVE BAND SWITCH

The ITT 243/244 is intended to replace mechanical devices, for switching channels or bands, in the frequency range of 10 to 1000 MHz. The differential forward resistance is constant and extremely small over a wide frequency and current range. The junction capacitance is small and relatively independent of voltage.

DIMENSIONS

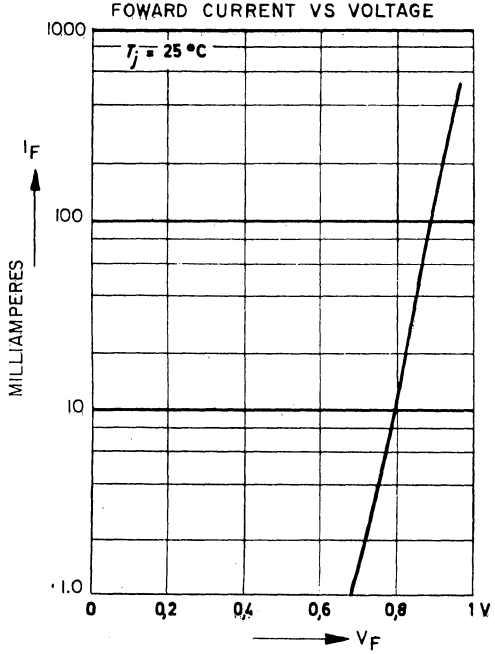


DOUBLE PLUG DIODE

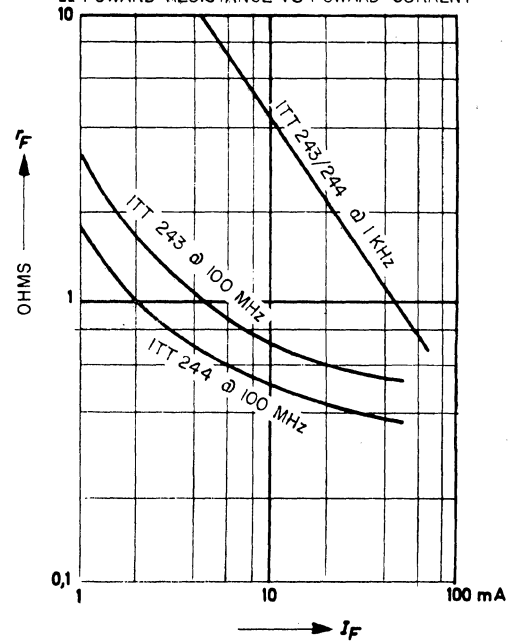
ELECTRICAL CHARACTERISTICS @ 25°C	**UNITS**
Reverse Voltage (Vr)	20 Volts
Forward Current (If)	100 mA
Forward Voltage (Vf) @ If = 100 mA	<1 Volt
Reverse Current (Ir) @ Vr = 15 V	<100 n Amps
Junction Temperature (Tj)	100°C
Storage Temperature (Ts)	− 55 to + 100°C

DYNAMIC CHARACTERISTICS @ 25°C	**ITT 244**	**ITT 243**
Differential Forward Resistance @ f = 50 to 1000 MHz @ If = 10 mA	0.5Ω (TYP 0.4Ω)	1Ω (TYP 0.7Ω)
Relative Change of Forward Resistance with change in Forward Current	3%/mA	5%/mA
Junction Capacitance @ Vr = 15V	< 2.2 Pf	< 2.2 Pf
Relative Change of Junction Capacitance with change of reverse voltage	1%/V	1%/V
Series Inductance (case)	< 2.5 nH	< 2.5 nH
Parallel Resistance (Rp) @ Vr = 15V	1 MΩ	1 MΩ

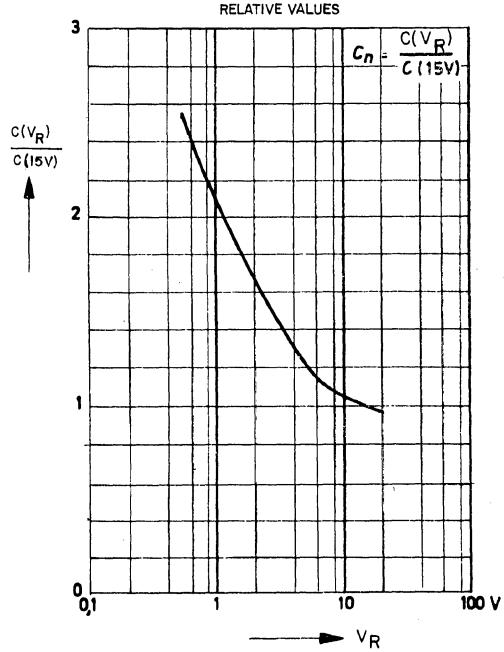
FOWARD CURRENT VS VOLTAGE



Ω FOWARD RESISTANCE VS FOWARD CURRENT



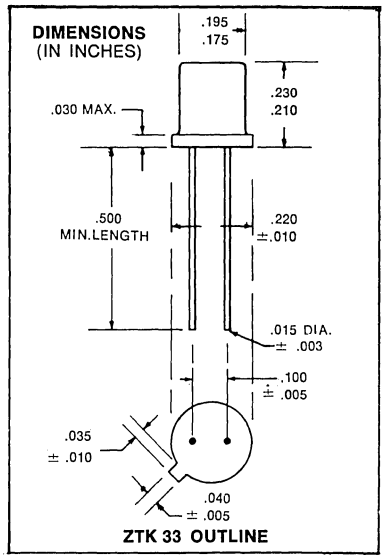
CAPACITANCE AS A FUNCTION OF VOLTAGE, RELATIVE VALUES



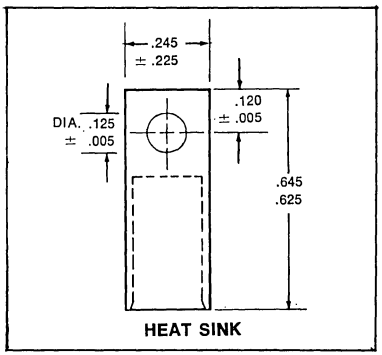
MONOLITHIC TEMPERATURE COMPENSATED ZENER DIODE

- **SINGLE MONOLITHIC ELEMENT**
- **HERMETICALLY SEALED TO-18**
- **MAXIMUM T.C. .005%/°C**

The ZTK33 Series is a new type of reference voltage temperature compensation device which uses proven integrated circuit technology. Devices are hermetically sealed monolithic elements possessing an unusually high degree of stability with maximum temperature coefficients of .005%/°C over the temperature range of −55°C to +100°C. The ZTK33 Series voltage ranges from 30 volts to 36 volts with a ±5% V_Z tolerance around each individual unit's nominal voltage. Special selection can be performed to provide devices with tighter temperature coefficients or voltage tolerances for custom circuit applications. A metal heat sink is available where thermal environment warrants.



ZTK 33 OUTLINE



HEAT SINK

GENERAL DATA:

Case	TO-18 Metal
Mounting Position	Any
Polarity	Cathode To Case, Tab indicates Anode
Operating Temperature	−55°C to +125°C
Storage Temperature	−55°C to +125°C

ELECTRICAL CHARACTERISTICS (T_A=25°C):

ITT Device Type (1)	Zener Test Current I_{ZT} mA	Zener Voltage V_Z @ I_{ZT} Min. Volts	Zener Voltage V_Z @ I_{ZT} Max. Volts	Maximum Dynamic Impedance (2) Z_{ZT} @ I_{ZT} Ohms	Maximum Zener Current I_{ZM} mA	Maximum $\triangle V_Z$ Over Temperature Range (3) V_Z=30V. Volts	Maximum $\triangle V_Z$ Over Temperature Range (3) V_Z=36V. Volts
ZTK33	5	30	36	25	10	.105	.126
ZTK33A	5	30	36	25	10	.232	.279

(1) Device Type: No Suffix; 0°C to +25°C to +70°C
"A" Suffix; −55°C to +25°C to +100°C

(2) Dynamic Impedance: Measured by superimposing a .50mA AC Signal.

(3) Maximum $\triangle V_Z$: All Devices possess a maximum ±.005%/°C Temperature Coefficient over the specified temperature range. Maximum $\triangle V_Z$ limits applicable to total V_Z distribution.

FIG. 1

Typical Transient time lapse from $\triangle V_Z$ after operation a. without heat sink b. with heat sink.

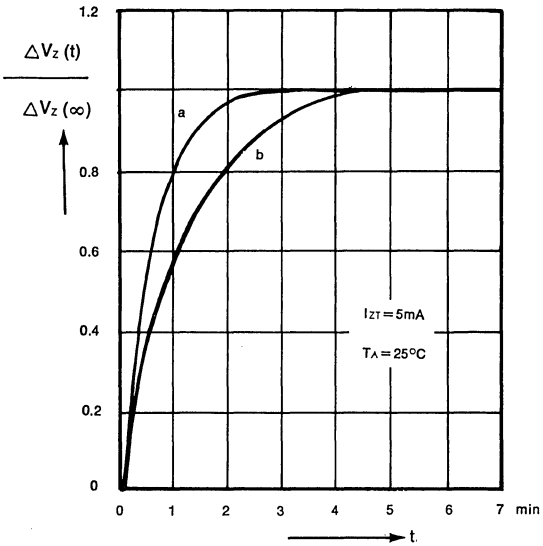


FIG. 2

Typical Change of Dynamic Impedance with Zener Current.

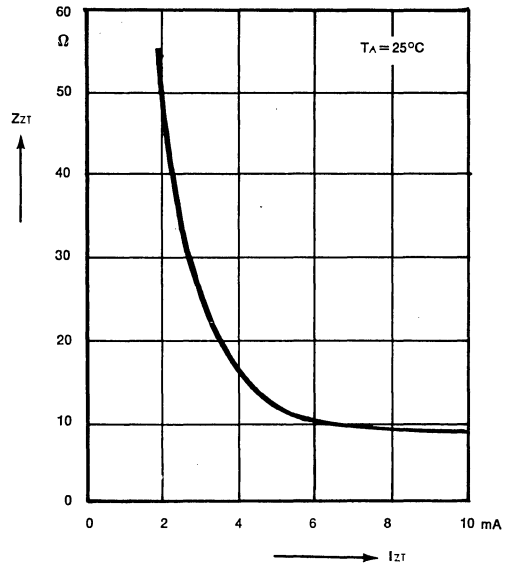
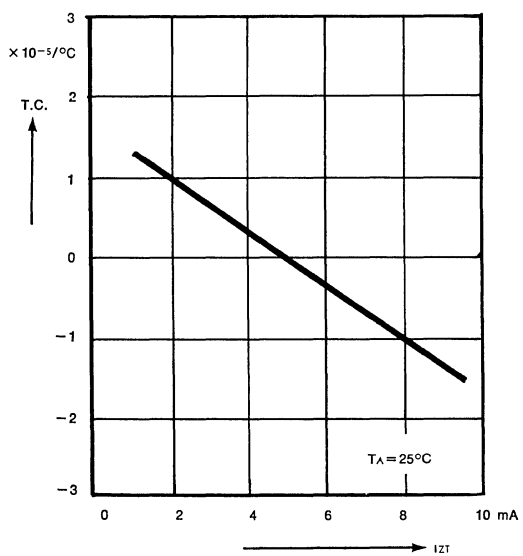


FIG. 3

Typical Change of Temperature Coefficient with Zener Current.

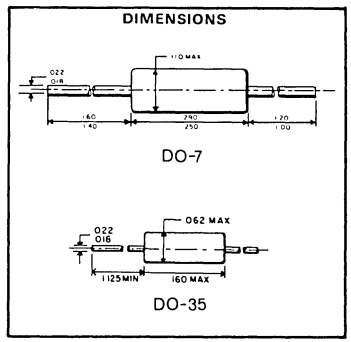


400 mW SILICON ZENER DIODES

- **HERMETICALLY SEALED**
- **INDUSTRY PREFERRED**
- **DO-7 GLASS PACKAGE**

The 400 mW Zener Diodes specified herein are all industry preferred JEDEC types being supplied in the following packages: 1N702 through 1N706 and 1N746 through 1N753 in DO-7 package, 1N707 through 1N726 and 1N754 through 1N759 in DO-35 package, 1N957 through 1N973 in DO-35 package.

Nominal voltages range from 2.7 volts thru 33 volts. Special selection can be performed to provide devices for custom circuit applications. All units are 100% tested and capable of meeting stringent environmental test requirements of MIL-S-19500.



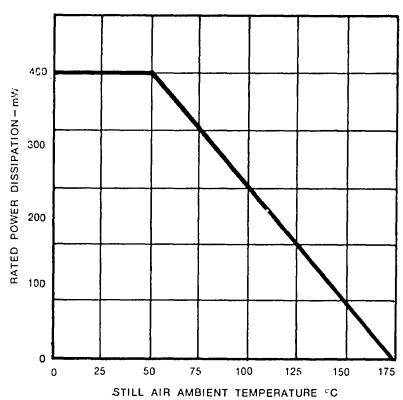
MAXIMUM RATINGS

Junction and Storage Temperatures . . . −65 to +175°C
D.C. Power Dissipation 400mW
Derating . . . . . Per derating curve (3.2mW/°C)

TYPE	Zener Voltage Vz (volts)	Zener Current Iz (MA)	Dynamic Impedance Zz (ohms)	Reverse Current (uA)	Reverse Voltage (volts)	Max. Forward Voltage (volts)	Forward Current (MA)
1N702	2.0/3.2	5	60	—	—	73	1.0
1N703	3.0/3.9	5	55	—	—	10	1.0
1N704	3.7/4.5	5	45	—	—	5	1.0
1N705	4.3/5.4	5	35	—	—	5	1.5
1N706	5.2/6.4	5	20	—	—	5	1.5
1N707	6.2/8.0	5	10	—	—	5	3.5
1N708	5.6	25	2.5	—	—	5	3.5
1N709	6.2	25	4.1	—	—	5	3.5
1N710	6.8	25	4.7	—	—	5	3.5
1N711	7.5	25	5.3	—	—	5	3.5
1N712	8.2	25	6.0	—	—	5	3.5
1N713	9.1	12	7.0	—	—	5	3.5
1N714	10.0	12	8.0	—	—	5	3.0
1N715	11.0	12	9.0	—	—	5	3.0
1N716	12.0	12	10.0	—	—	5	9.0
1N717	13.0	12	11.0	—	—	—	—
1N718	15.0	12	13.0	—	—	—	—
1N719	16.0	12	15.0	—	—	—	—
1N720	18.0	12	17.0	—	—	—	—
1N721	20.0	4	20.0	—	—	—	—
1N722	22.0	4	24.0	—	—	—	—
1N723	24.0	4	28.0	—	—	—	—
1N724	27.0	4	35.0	—	—	—	—
1N725	30.0	4	42.0	—	—	—	—
1N726	33.0	4	50.0	—	—	—	—

MECHANICAL CHARACTERISTICS

CASE: Hermetically sealed glass case.
DIMENSIONS: Per outline drawing.
FINISH: All external surfaces are corrosion resistant and leads solderable.
THERMAL RESISTANCE: 250° C/W (Typical) junction to ambient.
POLARITY: Band indicates cathode.
WEIGHT: 2 grams.
MOUNTING POSITION: Any.



1N746 SERIES
ELECTRICAL CHARACTERISTICS ($T_A = 25°C$):

Device Type*	Nominal Zener Voltage V_Z @ I_{ZT} Volts	Test Current I_{ZT} mA	Zener Impedance Max** Z_{ZT} @ I_{ZT} Ohms	Max DC Zener Current I_{ZM} mA	Reverse Leakage Current $T_A = 25°C$ T_R @ $V_R = 1V$ μA	Reverse Leakage Current $T_A = 150°C$ I_R @ $V_R = 1V$ μA
1N746	3.3	20	28	110	10	30
1N747	3.6	20	24	100	10	30
1N748	3.9	20	23	95	10	30
1N749	4.3	20	22	85	2	30
1N750	4.7	20	19	75	2	30
1N751	5.1	20	17	70	1	20
1N752	5.6	20	11	65	1	20
1N753	6.2	20	7	60	0.1	20
1N754	6.8	20	5	55	0.1	20
1N755	7.5	20	6	50	0.1	20
1N756	8.2	20	8	45	0.1	20
1N757	9.1	20	10	40	0.1	20
1N758	10.0	20	17	35	0.1	20
1N759	12.0	20	30	30	0.1	20

*Tolerance Designation:
No Suffix Denotes $V_Z \pm 10\%$;
"A" Suffix, ±5%.

**Zener Impedance: Measured by superimposing an AC Signal equal to 10% of the DC Test Current.

1N957 SERIES ELECTRICAL CHARACTERISTICS ($T_A = 25°C$):

Device Type*	Nominal Zener Voltage V_Z Volts	Test Current I_{ZT} mA	Maximum Zener Impedance** Z_{ZT} @ I_{ZT} Ohms	Z_{ZK} @ I_{ZK} Ohms	I_{ZK} mA	Max. DC Zener Current I_{ZM} mA	Reverse Leakage Current I_R Maximum μA	Test Voltage*** V_{R1}	V_{R2}
1N957	6.8	18.5	4.5	700	1.0	47	150	5.2	4.9
1N958	7.5	16.5	5.5	700	0.5	42	75	5.7	5.4
1N959	8.2	15	6.5	700	0.5	38	50	6.2	5.9
1N960	9.1	14	7.5	700	0.5	35	25	6.9	6.6
1N961	10	12.5	8.5	700	0.25	32	10	7.6	7.2
1N962	11	11.5	9.5	700	0.25	28	5	8.4	8.0
1N963	12	10.5	11.5	700	0.25	26	5	9.1	8.6
1N964[1]	13	9.5	13	700	0.25	24	5	9.9	9.4
1N965[1]	15	8.5	16	700	0.25	21	5	11.4	10.8
1N966[1]	16	7.8	17	700	0.25	19	5	12.2	11.5
1N967[1]	18	7.0	21	750	0.25	17	5	13.7	13.0
1N968[1]	20	6.2	25	750	0.25	15	5	15.2	14.4
1N969[1]	22	5.6	29	750	0.25	14	5	16.7	15.8
1N970[1]	24	5.2	33	750	0.25	13	5	18.2	17.3
1N971[1]	27	4.6	41	750	0.25	11	5	20.6	19.4
1N972[1]	30	4.2	49	1000	0.25	10	5	22.8	21.6
1N973[1]	33	3.8	58	1000	0.25	9.2	5	25.1	23.8

*Tolerance Designation
No Suffix Denotes $V_Z \pm 20\%$; A Suffix, ±10%; B Suffix, ± 5%.
**Zener Impedance: Measured by superimposing an AC Signal equal to 10% of the DC Test Current.
***Reverse Leakage:
V_{R1} - Test Voltage for 5% Tolerance Device
V_{R2} - Test Voltage for 10% Tolerance Device
No Leakage Specified for 20% Tolerance Device
1. Inquire for availability.

Package DO-41

ONE-WATT (5.1V - 33V) SILICON ZENER DIODES

ABSOLUTE MAXIMUM RATINGS

Characteristics	Unit
DC Power Dissipation	1.0 Watt
Derating Factor	6.67 mW/°C
Junction and Storage Temperature	-65 to +200 °C

One-watt silicon zener diodes designed for constant voltage reference from 5.1 thru 33 volts, with 10% and 5.0% tolerances. These diodes are hermetically sealed for greater reliability.

NOTE 1: The JEDEC type numbers shown have a 5% tolerance on nominal zener voltage. No suffix signifies a 10% tolerance.

NOTE 2: The Zener impedance is derived from the 60 Hz AC voltage, which results when an AC current having an rms value equal to 10% of the DC Zener current (I_{ZT} or I_{ZK}) is superimposed on I_{ZT} or I_{ZK}. Zener impedance is measured at two points to insure a sharp knee on the breakdown curve and eliminate unstable units.

MECHANICAL CHARACTERISTICS

CASE: Hermetically sealed glass case.

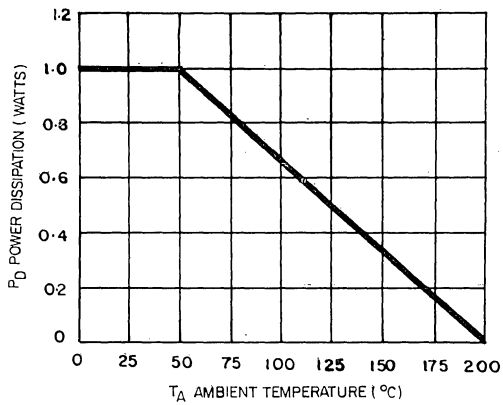
DIMENSIONS: Per outline drawing.

FINISH: All external surfaces are corrosion resistant and leads solderable.

POLARITY: Color Band indicates cathode. When in zener mode cathode is positive.

MOUNTING POSITION: Any.

POWER RATING VS AMBIENT TEMPERATURE



JEDEC TYPE NUMBER	ZENER VOLTAGE (V_Z) NOTE 1	TEST CURRENT (I_{ZT})	MAXIMUM DYNAMIC IMPEDANCE (Z_Z @ I_{ZT}) NOTE 2	MAXIMUM REVERSE CURRENT (I_R @ V_R)	TEST VOLTAGE (V_R)	MAXIMUM REGULATOR CURRENT (I_{ZM})	MAXIMUM KNEE IMPEDANCE (Z_{ZK} @ I_{ZK})	TEST CURRENT (I_{ZK})	MAXIMUM (SURGE) CURRENT (I_S)
	VOLTS	mA	OHMS	mA	VOLTS	mA	OHMS	mA	mA
1N4733A	5.1	49	7	10	1	178	550	1.0	890
1N4734A	5.6	45	5	10	2	162	600	1.0	810
1N4735A	6.2	41	2	10	3	146	700	1.0	730
1N4736A	6.8	37	3.5	10	4	133	700	1.0	660
1N4737A	7.5	34	4.0	10	5	121	700	0.5	605
1N4738A	8.2	31	4.5	10	6	110	700	0.5	550
1N4739A	9.1	28	5.0	10	7	100	700	0.5	500
1N4740A	10	25	7	10	7.6	91	700	0.25	454
1N4741A	11	23	8	5	8.4	83	700	0.25	414
1N4742A	12	21	9	5	9.1	76	700	0.25	380
1N4743A	13	19	10	5	9.9	69	700	0.25	344
1N4744A	15	17	14	5	11.4	61	700	0.25	304
1N4745A	16	15.5	16	5	12.2	57	700	0.25	285
1N4746A	18	14	20	5	13.7	50	750	0.25	250
1N4747A	20	12.5	22	5	15.2	45	750	0.25	225
1N4748A	22	11.5	23	5	16.7	41	750	0.25	205
1N4749A	24	10.5	25	5	18.2	38	750	0.25	190
1N4750A	27	9.5	35	5	20.6	34	750	0.25	170
1N4751A	30	8.5	40	5	22.8	30	1000	0.25	150
1N4752A	33	7.5	45	5	25.1	27	1000	0.25	135

IN5231 thru IN5250
500 mW ZENER DIODES
Package: DO-35

500 millwatt zener diode hermetically sealed in the DO-35 package for greater reliability. Designed for constant reference voltage between 3.3 and 33 volts with 10% and 5% tolerance.

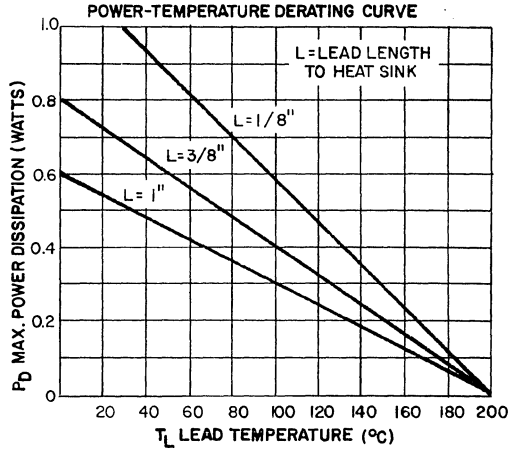
MAXIMUM RATINGS

Junction and Storage Temperature: −65 to +200°C

Lead Temperature not less than 1/16" from the case for 10 seconds: 230°C

DC Power Dissipation: 500 mW @ T_L = 75°C, Lead Length = 3/8" (Derate 4.0 mW/°C above 75°C)

Surge Power: 10 Watts (Non-recurrent square wave @ PW = 8.3 ms, T_J = 55°C)



Type Number	Regulator Voltage (V_Z)	Test Current (I_Z)	Maximum Dynamic Impedance (Z_Z)	Maximum Reverse Current (I_R) 25°C	I_R Test Voltage (V_R) (For A Suffix)	I_R Test Voltage (V_R) (For B Suffix)	Maximum Regulator Current (I_{ZM})	Maximum Dynamic Knee Impedance (Z_{ZK})	Maximum Temperature Coefficient
	v	ma de	ohms	μa	v	v	ma	ohms	%/°C
1N5231	5.1	20	17	5	1.9	2.0	89	1600	± .030
1N5232	5.6	20	11	5	2.9	3.0	81	1600	+ .038
1N5233	6.0	20	7	5	3.3	3.5	76	1600	+ .038
1N5234	6.2	20	7	5	3.8	4.0	73	1000	+ .045
1N5235	6.8	20	5	3	4.8	5.0	67	750	+ .050
1N5236	7.5	20	6	3	5.7	6.0	61	500	+ .058
1N5237	8.2	20	8	3	6.2	6.5	55	500	+ .062
1N5238	8.7	20	8	3	6.2	6.5	52	600	+ .065
1N5239	9.1	20	10	3	6.7	7.0	50	600	+ .068
1N5240	10	20	17	3	7.6	8.0	45	600	+ .075
1N5241	11	20	22	2	8.0	8.4	41	600	+ .076
1N5242	12	20	30	1	8.7	9.1	38	600	+ .077
1N5243	13	9.5	13	0.5	9.4	9.9	35	600	+ .079
1N5244	14	9.0	15	0.1	9.5	10	32	600	+ .082
1N5245	15	8.5	16	0.1	10.5	11	30	600	+ .082
1N5246	16	7.8	17	0.1	11.4	12	28	600	+ .083
1N5247	17	7.4	19	0.1	12.4	13	27	600	+ .084
1N5248	18	7.0	21	0.1	13.3	14	25	600	+ .085
1N5249	19	6.6	23	0.1	13.3	14	24	600	+ .086
1N5250	20	6.2	25	0.1	14.3	15	23	600	+ .086
1N5251	22	5.6	29	0.1	16.2	17	21	600	+ .087
1N5252	24	5.2	33	0.1	17.1	18	19.1	600	+ .088
1N5253	25	5.0	35	0.1	18.1	19	18.2	600	+ .089
1N5254	27	4.6	41	0.1	20	21	16.8	600	+ .090
1N5255	28	4.5	44	0.1	20	21	16.2	600	+ .091
1N5256	30	4.2	49	0.1	22	23	15.1	600	+ .091
1N5257	33	3.8	58	0.1	24	25	13.8	700	+ .092

SILICON PLANAR DOUBLE PLUG DIODES (DPD's)

ITT Semiconductors' Silicon DPD's (Double Plug Diodes) are Planar Epitaxial Passivated to assure utmost reliability and uniform electrical parameters. They feature carefully controlled forward characteristics over wide current ranges. The pellet is fused to the end plugs, not soldered. Thus, the stability of the anode and cathode contacts is much greater than that of soldered contacts. Sealing is performed in an inert atmosphere eliminating any possibility of sealed-in contamination.

DPD's are smaller than similar DO-7 type diodes. Yet, they have greater inherent reliability due to their fused construction and higher dissipation capabilities. Baked at a minimum of 300°C, DPD's are completely stabilized. Their ruggedness is unsurpassed.

There is a DPD equivalent for all ITT Semiconductors' DO-7 Silicon Planar diodes making it easy to take advantage of these improved characteristics:

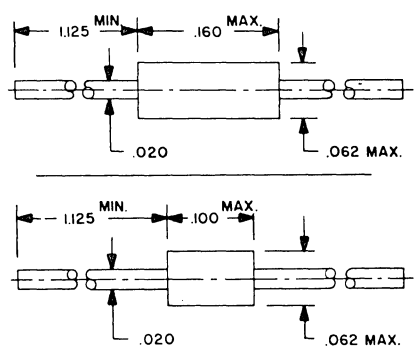
- Low leakage current
- High conductance
- Low capacitance
- Fast switching
- Uniform characteristics
- Improved stability

MECHANICAL DATA

CASE: Hermetically sealed glass
FINISH: All external surfaces corrosion resistant and leads readily solderable
LEADS: Dumet, tin plated
POLARITY: Banded end cathode
WEIGHT: .135 grams (approx.)
MTG. POSITION: Any

DIMENSIONS

STANDARD



AVAILABLE

SWITCHING DIODES TYPICAL CHARACTERISTICS

DPD TYPE #	DO-7 EQUIV. #	BV @ 5 uA V	MAXIMUM VF @ 25°C V @ IF		V @ IF		V@ IF		V @ IF		V @ IF		V @ IF		TRR ns	MAXIMUM REVERSE CURRENT uA @ 25°C	mA @ 150°C	VR	CAP. @ 0.0V PF	TFR	TRR (5) ns	Stored Charge PC	ABSOLUTE MAXIMUM RATINGS Ave. Rect. Fwd. I @ 25°C mA	Max. Oper. Volt. Cont.	Power Diss. @ 25°C (12) MW
			V	mA	V	mA	V	mA	V	mA	V	mA	V	mA												
1N4148	1N914	75(1)	1.0	10											4(2)	.025	.05	20	4				75		500
1N4149	1N916	75(1)	1.0	10											4(2)	.025	.05	20	2				75		500
1N4150	1N3600		.54/.62	1.0	.66/.74	10	.76/.86	50	.82/.92	100	.87/1.0	200			(3)	0.1	0.1	50	2.5	10ns(4)			150		500
1N4151	1N3604	75	.1.0	50											2(2)	.05	.05	50	2		4		150	50	500
1N4152	1N3605	40	.49/.55	0.1	.53/.59	.25	.59/.67	1.0	.62/.70	2.0	.70/.81	10	.74/.88	20	2(2)	.05	.05	30	2		4		150	30	500
1N4153	1N3606	75	.49/.55	0.1	.53/.59	.25	.59/.67	1.0	.62/.70	2.0	.70/.81	10	.74/.88	20	2(2)	.05	.05	50	2		4		150	50	500
1N4154	1N4009	35	1.0	30											2(2)	0.1	0.1	25	4		4		25	25	500
1N4305	1N4063	75	.505/.575	.25	.55/.65	1.0	.61/.71	2.0	.70/.85	10					2(2)	0.1	0.1	50	2		4		150		500
1N4444		70	.44/.55	0.1	.56/.68	1.0	.69/.82	10	.85/1.0	100						.05	.05	50	2		7		200	50	500
1N4446	1N914A	75(1)	1.0	20											4(2)	.025	.05	20	4				150	75	500
1N4447	1N916A	75(1)	1.0	20											4(2)	.025	.05	20	2				150	75	500
1N4448	1N914B	75(1)	.62/.72	5	1.0	100									4(2)	.025	.05	20	4	2.5V(6)			150	75	500
1N4449	1N916B	75(1)	.63/.73	5	1.0	30									4(2)	.025	.05	20	2	2.5V(6)			150	75	500
1N4450		40(1)	.42/.54	0.1	.52/.64	1.0	.64/.76	10	.80/.92	100	1.0	200			4(2)	.05	.05	30	4				200	30	500
1N4451		40	.40/.50	0.1	.51/.61	1.0	.62/.72	10	.75/.875	100	1.0	300				.05	.05	30	6		10		200	30	500
1N4452		40	.42/.54	0.1	.51/.62	1.0	.60/.71	10	.71/.83	100	1.0	600	.90/1.2	1A	50(7)	.05	.05	30	30				200	30	500
1N4453		30	.43/.55	.01	.51/.63	0.1	.60/.71	1.0	.69/.80	10	.80/.92(8)	100				.05	.05	20	30			50/500(9)		20	400
1N4454	1N3064	75	1.0	10											2(2)	0.1	0.1	50	2	3.0V(10)	4			75	500
1N5194	1N483B	80(11)	1.0	100												.025	.005	70						80	250
1N5195	1N485B	200(11)	1.0	100												.025	.005	180						200	250
1N5196	1N486B	250(11)	1.0(13)	100												.025	.005	225						250	250
1N5605	1N457	70(11)	1.0	20												.025	.005	60						70	250
1N5606	1N458	150(11)	1.0	7.0												.025	.005	125						150	200
1N5607	1N459	200(11)	1.0	3.0												.025	.005	175						200	200
1N5608	1N658	120(11)	1.0	100											300(16)	.050	.025	50						120	250
1N5609	1N660	120(11)	1.0	6.0											300(17)	5.0	.050 (15)	100	2.7(14)					120	250

NOTES
(1) BV = 100V @ IR 100 uA
(2) IF = 10 mA Recover to 1 mA
VR = 6V
RL = 100 Ohms
(3) TRR = 4ns @ IF = IR = 10 to 200 mA irr = 0.1 IF
TRR = 6ns @ IF = IR = 200 to 400 mA irr = 0.1 IF
TRR = 6ns @ IF = 10 mA, IR = 1 mA irr = 0.1 mA
(4) IF = 200 mA tr ≤ 0.4 ns, tp = 100 ns
VFR = 1.0V, DU ≤ 1%
(5) iF = 10 mA
IR = 10 mA
Recover to 1 mA
(6) 50 mA peak square wave, 0.1 us pulse width, 5 to 100 KC rep. rate, generator tr ≤ 30 ns
(7) IF 500 mA
VR = adjust for IR = 500 mA Recover to 50 mA
(8) Pulse width = 30 us, duty cycle = 3%, VF measured at 25 ± 3us
(9) Q @ IF = 1 mA MIL-STD-750 method 4061
(10) IF = 100 mA peak square wave 0.1 us pulse width RL = 50 Ohms tr ≤ 30 ns, 5 to 100 KC
(11) @ 100 uA
(12) Rated Max, Junction Temp. = 200°C
(13) Pulse width = 8.5 msec, duty cycle ≤ 2%.
(14) VR = 10V, f = 1 MHz
(15) TA = 100 °C
(16) IF = 5 mA, VR = 40V RI = 2K, CI = 10 pF Recover to 80 kΩ
(17) IF = 30 mA, VR = 35V Recover to 400 kΩ

SILICON PLANAR DIODES

HOW TO USE THIS BUYING GUIDE

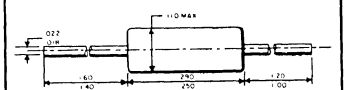
Standard general purpose diodes are listed in numerical order below. Each diode has a line number referenced to the specification tables on pages 2, 3 and 4. Use this buying guide two ways: select the diode by type number, or locate the type number from the specification data.

ITT is the world's leading producer of diodes. Call your ITT sales engineer or distributor for quotation on all your diode needs.

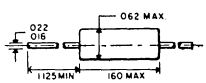
Part No.	Line No.	Part No.	Line No.	Part No.	Line No.	Part No.	Line No.
1N194	45	1N659	68	1N905A	12	1N3654	144
1N194A	44	1N662	126	1N906	10	1N3669	98
1N195	46	1N662A	145	1N906A	13	1N3731	147
1N196	43	1N663	129	1N907	27	1N3872	140
1N251	20	1N663A	146	1N907A	30	1N4009	16
1N379	1	1N690	60	1N908	53	1N4148[1]	108
1N380	2	1N691	130	1N908A	56	1N4149[1]	110
1N381	3	1N692	164	1N914	107	1N4150[1]	71
1N382	6	1N696	54	1N914JAN	142	1N4151[1]	120
1N383	11	1N697	163	1N914A	114	1N4152[1]	41
1N384	14	1N778	155	1N914B	124	1N4153[1]	100
1N385	23	1N789	25	1N916	109	1N4154[1]	37
1N386	40	1N790	24	1N916A	115	1N4305[1]	117
1N387	66	1N791	32	1N916B	118	1N4380	76
1N388	77	1N792	34	1N920	61	1N4444[1]	95
1N389	90	1N793	79	1N921	132	1N4446[1]	113
1N390	103	1N794	78	1N922	165	1N4447[1]	116
1N391	137	1N795	82	1N925	48	1N4448[1]	122
1N392	152	1N796	85	1N926	49	1N4449[1]	123
1N393	168	1N797	157	1N927	91	1N4450[1]	57
1N456	31	1N798	156	1N928	158	1N4451[1]	59
1N456A	36	1N799	159	1N929	15	1N4453[1]	33
1N457	80	1N806	153	1N930	111	1N4454[1]	104
1N457A	84	1N808	154	1N931	167	S298	86
1N460	138	1N810	69	1N934	81	S398	65
1N460A	139	1N811	7	1N993	8	S400	131
1N461	28	1N812	17	1N3062	112	S401	75
1N461A	35	1N813	4	1N3063	102	S402	143
1N462	93	1N814	47	1N3064	105	S403	125
1N462A	96	1N815	5	1N3065	99	S500	133
1N464	169	1N818	128	1N3066	106	S501	87
1N482	38	1N837	149	1N3067	21	S502	62
1N482A	39	1N837A	150	1N3068	22	S504	134
1N482B	58	1N838	170	1N3069	92	S505	88
1N483	94	1N840	70	1N3123	50	S506	63
1N483A	97	1N841	171	1N3124	51	S507	135
1N619	18	1N844	151	1N3206	127	S508	89
1N625	19	1N891	83	1N3298	136	S509	64
1N626	67	1N892	160	1N3600	72	WG140[1]	166
1N627	141	1N903	52	1N3600USN	73	WG141[1]	148
1N643	172	1N903A	55	1N3604	119	WG142[1]	74
1N643A	173	1N904	26	1N3605	42		
1N658	161	1N904A	29	1N3606	101		
1N658A	162	1N905	9	1N3607	121		

Note: 1. Double plug diode package

DIMENSIONS



DO-7 PACKAGE



DOUBLE PLUG DIODE PACKAGE

MECHANICAL DATA

Case:
Hermetically sealed glass

Finish:
All external surfaces corrosion resistant and leads readily solderable

Leads:
Dumet, tin plated

Weight:
0.135 grams (approx.)

Mounting Position:
Any

Marking:
Diodes carry ITT identification, and are EIA Color Coded. Bands 1, 2, 3 and 4 on the illustration above indicate the first, second, third and fourth digit respectively of the type designation, starting from the cathode end of the diode.

Black.....0	Green.....5
Brown.....1	Blue.....6
Red.....2	Violet.....7
Orange.....3	Gray.....8
Yellow.....4	White.....9

ELECTRICAL CHARACTERISTICS @ 25°C unless otherwise noted

V_{RM}	I_F		I_R		High Temp I_R			Reverse Recovery Time trr					Cap. C		Part No.	Line No.
	mA @	V_F	μA @	V_R	μA	V_R	°C	I_FmA	V_R	Rec. to	nsec	Test Condition	pf @	V_R		
9	35	1	0.5	8.2	5	8.2	100						35	6	1N379	1
11	30	1	0.5	10	5	10	100						30	6	1N380	2
13.5	23	1	0.5	12	5	12	100						28	64	1N381	3
15	5	1	0.5	5	10	5	125	5	—10	0.5mA	250	JAN 256			1N813	4
15	100	1.5	0.5	5	10	5	125	5	—10	0.5mA	250	JAN 256			1N815	5
17	17	1	0.5	15	5	15	100						25	6	1N382	6
20	1	1	1	10	10	10	125	5	—10	0.5mA	250	JAN 256	2	0	1N811	7
20	10	1.2	1	6				10	—6	3mA	4	R_L=75Ω			1N993	8
20	10	1	0.1	20	10	20	100	10	—5		4	R_L=100Ω	1	6	1N905	9
20	10	1	0.1	20	10	20	100	10	—5		4	R_L=100Ω	2.5	6	1N906	10
20	12	1	0.1	18	10	18	100						20	6	1N383	11
20	20	1	0.1	20	10	20	100	10	—5	1mA	4	R_L=100Ω	1	6	1N905A	12
20	20	1	0.1	20	10	20	100	10	—5	1mA	4	R_L=100Ω	2.5	6	1N906A	13
25	9	1	0.1	22	10	22	100						15	6	1N384	14
25	20	1	0.1	20											1N929	15
25	30	1	0.1	25	100	25	150	10	—6		2	R_L=100Ω	4	0	1N4009	16
30	2	1	1	10	10	10	125	5	—10	0.5mA	250	JAN 256	2	0	1N812	17
30	3	1	.08	10	16	10	100								1N619	18
30	4	1.5	1	20	30	20	100	30	—35	400kΩ	1000	IBM Y Mod			1N625	19
30	5	1	0.1	10	10	10	100	5	—10	0.5mA	150		1	0	1N251	20
30	5	1	0.1	20	100	20	150	10	—6	1mA	2	R_L=100Ω	4	0	1N3067	21
30	5	1	0.1	20	100	20	150	30	30mA[2]	1mA	50	R_L=100Ω	6	0	1N3068	22
30	7	1	0.1	27	10	27	100						12	6	1N385	23
30	10	1	5	20	30	20	100	5	—20	200kΩ	250				1N790	24
30	10	1	1	20	30	20	100	5	—20	200kΩ	500				1N789	25
30	10	1	0.1	30	10	30	100	10	—5		4	R_L=100Ω	1	6	1N904	26
30	10	1	0.1	30	10	30	100	10	—5		4	R_L=100Ω	2.5	6	1N907	27
30	15	1	0.5	25	30	25	150						10	0	1N461	28
30	20	1	0.1	30	10	30	100	10	—5	1mA	4	R_L=100Ω	1	6	1N904A	29
30	20	1	0.1	30	10	30	100	10	—5	1mA	4	R_L=100Ω	2.5	6	1N907A	30
30	40	1	0.025	25	5	25	150								1N456	31
30	50	1	5	20	30	20	100	5	—20	200KΩ	500				1N791	32
30	0.01	.43/.55	0.05	20	50	20	150						30	0	1N4453[1]	33
	0.1	.51/.63														
	1	.60/.71														
	10	.69/.80														
	100	.80/.92														
30	100	1	5	20	30	20	100	5	—20	100kΩ	500				1N792	34
30	100	1	0.5	25	30	25	150								1N461A	35
30	100	1	0.025	25	5	25	150						5	0	1N456A	36
35	30	1	0.1	25	100	25	150	10	—6	1mA	2	R_L=100Ω			1N4154[1]	37
36	100	1.1	0.25	30	30	30	150								1N482	38
36	100	1	0.025	30	15	30	150								1N482A	39
37	5.5	1	0.1	33	10	33	100						10	6	1N386	40
40	0.1	.49/.55	0.05	30	50	30	150	10	—6	1mA	2	R_L=100Ω	2	0	1N4152[1]	41
	0.25	.53/.59														
	1	.59/.67														
	2	.62/.70														
	10	.70/.81														
	20	.74/.88														
40	0.1	0.55	0.05	30	50	30	150	10	—6	1mA	2	R_L=100Ω	2	0	1N3605	42
40	1	2	10	40	300	50	150	30	—35		100				1N196	43
40	1	1	10	40	300	40	150	30	—35		200				1N194A	44
40	1.5	2	10	40	300	40	150	30	—35		200				1N194	45
40	2	2	10	40	300	40	150	30	—35		300				1N195	46
40	2	1	0.1	20	10	20	125	5	—10	0.5mA	250	JAN 256			1N814	47
40	5	1	1	10	20	10	100	5	—10	20kΩ	150	JAN 256			1N925	48
40	5	1	0.1	10	10	10	100	5	—10	20kΩ	150	JAN 256			1N926	49
40	10	1.5	0.1	40	10	40	100	10	—5	1mA	4	R_L=100Ω	0.8	6	1N3123	50
40	10	1.5	0.1	40	10	40	100	10	—5	1mA	4	R_L=100Ω	2	6	1N3124	51
40	10	1	0.1	40	10	40	100	10	—5		4	R_L=100Ω	1	6	1N903	52
40	10	1	0.1	40	10	40	100	10	—5		4	R_L=100Ω	2.5	6	1N908	53
40	10	1	0.015	20	20	20	150	10		10mA	5		4	0	1N696	54
40	20	1	0.1	40	10	40	100	10	—5	1mA	4	R_L=100Ω	1	6	1N903A	55
40	20	1	0.1	40	10	40	100	10	—5	1mA	4	R_L=100Ω	2.5	6	1N908A	56
40	0.1	.42/.54	0.05	30	50	30	150	10	—6	1mA	4	R_L=100Ω	4	0	1N4450[1]	57
	1	.52/.64														
	10	.64/.76														
	100	.80/.92														
	200	1														

Notes: 1. Double plug diode package 2. I_RmA

ELECTRICAL CHARACTERISTICS, continued

V_{RM}	I_F		I_R		High Temp I_R			Reverse Recovery Time trr					Cap. C		Part No.	Line No.
	mA	@ V_F	μA	@ V_R	μA	V_R	°C	I_FmA	V_R	Rec. to	nsec	Test Condition	pf	@ V_R		
40	100	1	0.025	30	5	30	150								1N482B	58
40	0.1	.40/.50	0.05	30	50	30	150						6	0	1N4451[1]	59
	1	.51/.61														
	10	.62/.72														
	100	.75/.88														
	300	1														
40	400	1	0.25	30	50	30	150	500	−30	10kΩ	800	R_L=1kΩ			1N690	60
40	500	1	0.25	30	50	30	150	500	−30	10kΩ	300	R_L=1kΩ	9	7.5	1N920	61
40	500	1	0.05	25				500	−30	10kΩ	15	R_L=100Ω	7	9	S502	62
40	500	1	0.05	25				500	−30	10kΩ	30	R_L=100Ω	7	9	S506	63
40	500	1	0.05	25				500	−30	10kΩ	50	R_L=100Ω	7	9	S509	64
40	500	0.9	0.2	25				500	−30	10kΩ	200	R_L=1kΩ	7	9	S398	65
43	4.5	1	0.1	39	10	39	100						8	6	1N387	66
50	4	1.5	1	35	30	35	100	30	−35	400kΩ	1000	IBM Y Mod			1N626	67
50	6	1	5	50	25	50	100	30	−35	400kΩ	300	JAN 256	2.7	10	1N659	68
50	10	1	1	40				10			50				1N810	69
50	150	1	0.1	40	15	40	100	30	−35	400kΩ	300	JAN 256			1N840	70
50	1	.54/.62	0.1	50	100	50	150	20 to 200	20 to 200[2]		4	irr=0.1 I_F	2.5	0	1N4150[1]	71
	10	.66/.74														
	50	.76/.86						200 to 400	200 to 400[2]		6	irr=0.1 I_F				
	100	.86/.92														
	200	.87/1.0						10	12		6	irr=0.1 mA				
50	200	1	0.1	50	100	50	150	10		0.1mA	6		2.5	0	1N3600	72
50	200	1	0.1	50	100	50	150	10		1.1mA	4	R_L=100Ω	2.5	0	1N3600 USN	73
50	250	1	0.1	30				10	−6	1mA	6	R_L=100Ω	4	0	WG142[1]	74
50	400	1	0.1	30				400	−30	10kΩ	15	R_L=100Ω	7	9	S401	75
50	570	1.4	50	50				570	−15	1mA	1.8	R_L=100Ω	3	15	1N4380	76
52	3.5	1	0.1	47	10	47	100						6	6	1N388	77
60	10	1	5	50	30	50	100	5	−40	200kΩ	250				1N794	78
60	10	1	1	50	30	50	100	5	−20	200kΩ	500				1N793	79
60	20	1	0.025	60	5	60	150						8	0	1N457	80
60	30	1	0.025	60	6	60	150	30	−35	400kΩ	1000				1N934	81
60	50	1	5	50	3	50	100	5	−40	200kΩ	500				1N795	82
60	50	1	0.1	50	25	50	100			80kΩ	300	JAN 256			1N891	83
60	100	1	0.025	60	5	60	150								1N457A	84
60	100	1	5	50	30	50	100	5	−40	100kΩ	500				1N796	85
60	500	1	0.2	30				500	−50	10kΩ	200	R_L=1kΩ	7	9	S298	86
60	500	1	0.1	30				500	−30	10kΩ	15	R_L=100Ω	7	9	S501	87
60	500	1	0.1	30				500	−30	10kΩ	30	R_L=100Ω	7	9	S505	88
60	500	1	0.1	30				500	−30	10kΩ	50	R_L=100Ω	7	9	S508	89
62	2.7	1	1	56	50	50	100						5.6	6	1N389	90
65	10	1	0.1	10	10	10	100	5	−10	20kΩ	150	JAN 256			1N927	91
65	50	1	0.1	50	100	50	100	30	30mA[2]	1mA	50	R_L=100Ω	6	0	1N3069	92
70	5	1	0.5	60	30	60	150						8	0	1N462	93
70	100	1.1	0.25	60	30	60	150								1N483	94
70	0.1	.44/.55	0.05	50	50	50	150	10	−6	1mA	2	R_L=100Ω	2	0	1N4444[1]	95
	1	.56/.68														
	10	.69/.82														
	100	.85/1.0														
70	100	1	0.5	60	30	60	150								1N462A	96
70	100	1	0.025	60	15	60	150								1N483A	97
70	400	1.1	0.25	70				300	−10	1mA	200	R_L=100Ω	10	10	1N3669	98
75	0.1	0.53	0.1	50	100	50	150	10	−6	1mA	2	R_L=100Ω	1.5	0	1N3065	99
75	0.1	.49/.55	0.05	30	50	30	150	10	−6	1mA	2	R_L=100Ω	2	0	1N4153[1]	100
	0.25	.53/.59														
	1	.59/.67														
	1	.62/.70														
	10	.70/.81														
	20	.74/.88														
75	0.1	0.55	0.05	50	50	50	150	10	−6	1mA	2	R_L=100Ω	2	0	1N3606	101
75	0.25	0.58	0.1	50	100	50	150	10	−1	1mA	4	R_L=100Ω	2	0	1N3063	102
75	2	1	1	68	50	68	100						5.2	6	1N390	103
75	10	1						10	−6	1mA	2	R_L=100Ω	2	0	1N4454[1]	104
75	10	1	0.1	50	100	50	150	10	−1	1mA	4	R_L=100Ω	2	0	1N3064	105
75	10	1	0.1	50	100	50	150	10	−6	1mA	2	R_L=100Ω	1	0	1N3066	106
75	10	1	0.025	20	50	20	150	10	−6	1mA	4	R_L=100Ω	4	0	1N914	107
75	10	1	0.025	20	50	20	150						4	0	1N4148[1]	108
75	10	1	0.025	20	50	20	150	10	−6	1mA	4	R_L=100Ω	2	0	1N916	109
75	10	1	0.025	20	50	20	150						2	0	1N4149[1]	110

Notes: 1. Double plug diode package 2. I_RmA

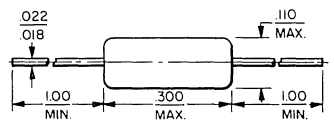
ELECTRICAL CHARACTERISTICS, continued

V_{RM}	I_F		I_R		High Temp I_R			Reverse Recovery Time trr					Cap. C		Part No.	Line No.
	mA @	V_F	μA @	V_R	μA	V_R	°C	I_FmA	V_R	Rec. to	nsec	Test Condition	pf @	V_R		
75	20	1	0.1	50											1N930	111
75	20	1	0.1	50	100	50	150	10	—6	1mA	2	R_L=100Ω	1	0	1N3062	112
75	20	1	0.025	20	50	20	150	10	—6	1mA	4	R_L=100Ω	4	0	1N4446[1]	113
75	20	1	0.025	20	50	20	150	10	—8	1mA	4	R_L=100Ω	4	0	1N914A	114
75	20	1	0.025	20	50	20	150	10	—6	1mA	4	R_L=100Ω	2	0	1N916A	115
75	20	1	0.025	20	50	20	150	10	—6	1mA	4	R_L=100Ω	2	0	1N4447[1]	116
75	0.25	.50/.58						10	—6	1mA	2	R_L=100Ω	2	0	1N4305[1]	117
	1	.55/.65														
	2	.61/.71														
	10	.70/.81														
75	30	1	0.025	20	50	20	150	10	—6	1mA	4	R_L=100Ω	2	0	1N916B	118
75	50	1	0.05	50	50	50	150	10	—6	1mA	2	R_L=100Ω	2	0	1N3604	119
75	50	1	0.05	50	50	50	150	10	—6	1mA	2	R_L=100Ω	2	0	1N4151[1]	120
75	50	1	0.05	50	50	50	150	10	—6	1mA	2	R_L=100Ω	2	0	1N3607	121
75	5	.62/.72	0.025	20	50	20	150	10	—6	1mA	4	R_L=100Ω	4	0	1N4448[1]	122
	100	1.0														
75	5	.63/.73	0.025	20	50	20	150	10	—6	1mA	4	R_L=100Ω	2	0	1N4449[1]	123
	30	1.0														
75	100	1	0.025	20	50	20	150	10	—6	1mA	4	R_L=100Ω	4	0	1N914B	124
75	200	1	0.1	50	100	50	150	200	200mA[2]	0.1mA	6	R_L=100Ω	2.5	0	S403	125
80	10	1	1	10	100	50	100	5	—40	100kΩ	500		3	10	1N662	126
80	10	1	0.025	20	50	20	150	10	—6	1mA	4	R_L=100Ω	4	0	1N3206	127
80	30	1.5	0.25	60	20	60	100	20	—40		500	JAN 256			1N818	128
80	100	1	5	75	50	75	100	5	—40	200kΩ	500				1N663	129
80	400	1	0.25	60	50	60	150	500	—50	10kΩ	800	R_L=1kΩ			1N691	130
80	400	1	0.1	50				400	—30	10kΩ	15	R_L=100Ω	7	9	S400	131
80	500	1	0.25	60	50	60	150	500	—50	10kΩ	300	R_L=1kΩ			1N921	132
80	500	1	0.1	50				500	—30	10kΩ	15	R_L=100Ω	7	9	S500	133
80	500	1	0.1	50				500	—30	10kΩ	30	R_L=100Ω	7	9	S504	134
80	500	1	0.1	50				500	—30	10kΩ	50	R_L=100Ω	7	9	S507	135
80	500	0.9	0.2	60	45	60	150	500	—30	50mA	50	R_L=50Ω			1N3298	136
90	1.5	1	1	82	50	82	100						4.8	6	1N391	137
90	5	1	0.01	10	0.2	10	100						3	10	1N460	138
90	.15	1	0.01	10	0.2	10	100						4	10	1N460A	139
90	150	1	0.1	75				200	—20	5mA	50	R_L=100Ω	5	0	1N3872	140
100	4	1.5	1	75	30	75	100	30	—35	400kΩ	1000	IBM Y Mod			1N627	141
100	10	1	5	75	50	20	150	10			5	R_L=100Ω	2.8	1.5	1N914JAN	142
100	25	1	10	80	0.5	20	71	30	—35	400kΩ	100	R_L=2kΩ			S402	143
100	50	1	0.025	75	25	75	150	5	—6.5	1mA	4				1N3654	144
100	100	1	1	10	100	50	100	5	—40	100kΩ	300	JAN 256			1N662A	145
100	100	1	0.1	75	15	75	100	5	—40	200kΩ	300	JAN 256			1N663A	146
100	100	1	0.050	50	50	50	150	10	—6	1mA	3	R_L=100Ω	2	0	1N3731	147
100	100	1	0.050	50				10	—6	1mA	3	R_L=100Ω	2	0	WG141[1]	148
100	150	1	0.1	75	15	75	100	30	—35	400kΩ	500	JAN 256			1N837	149
100	150	1	0.1	80	15	80	100	30	—35	400kΩ	300	JAN 256			1N837A	150
100	200	1	0.1	80	15	80	100	30	—35	400kΩ	500	JAN 256			1N844	151
110	1.2	1	1	100	50	100	100						4.5	6	1N392	152
110	4	1	0.5	100	50	100	125	5	—40		300	JAN 256			1N806	153
110	100	1	1	100	50	100	125	30	—35		300	JAN 256 R_L=500Ω			1N808	154
112	10	1	0.5	100	30	100	125	5	—40	400kΩ	300	JAN 256			1N778	155
120	10	1	5	100	30	100	100	5	—40	200kΩ	250				1N798	156
120	10	1	1	100	30	100	100	5	—40	200kΩ	500				1N797	157
120	10	1	0.1	10	10	10	100	5	—10	20kΩ	150				1N928	158
120	50	1	5	100	30	100	100	5	—40	200kΩ	500				1N799	159
120	50	1	0.1	100	25	100	100			80kΩ	300	JAN 256			1N892	160
120	100	1	0.05	50	25	50	150	5	—40	80kΩ	300				1N658	161
120	100	1	0.025	50	10	50	150	5	—40	80kΩ	300	JAN 256			1N658A	162
120	250	1	1	50				100	—10	10mA	5		25	0	1N697	163
120	400	1	0.25	90	50	90	150	500	—50	10kΩ	800	R_L=1kΩ			1N692	164
120	500	1	0.25	90	100	90	150	500	—50	10kΩ	300	R_L=1kΩ			1N922	165
125	150	1						10	—6	1mA	4	R_L=100Ω			WG140[1]	166
125	20	1	0.1	100											1N931	167
135	0.9	1	1	120	50	120	100						4.2	6	1N393	168
150	3	1	0.5	125	30	120	150								1N464	169
150	150	1	0.1	125	15	125	100	30	—35	400kΩ	500	JAN 256			1N838	170
150	150	1	0.1	120	15	120	100	30	—35	400kΩ	300	JAN 256			1N841	171
175	10	1	0.025	10	15	100	100	5	—40	200kΩ	300				1N643	172
175	40	1	1.0	100	15	100	100						3	—10	1N643A	173

Notes: 2. I_RmA 1. Double plug diode package

SILICON EPITAXIAL PLANAR SWITCHING DIODE

DIMENSIONS



DO-7

ABSOLUTE MAXIMUM RATINGS

CHARACTERISTICS @ 25°C		UNITS
Peak Inverse Voltage	100	Volts
Power Dissipation	250	mW
Storage Temperature	−65 to +200	°C
Avg. Rect. Fwd. Current	75	mA
Surge Current, 1 sec.	500	mA

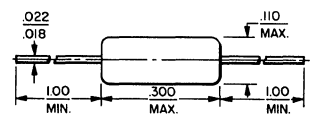
ELECTRICAL CHARACTERISTICS @ 25°C unless otherwise noted.

SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS
PIV	100			Vdc	$I_R = 100\mu A$
I_R			5.0 .025 50	μA μA μA	$V_R = 75V$ $V_R = 20V$ $V_R = 20V$, T = 150°C
V_F			1.0	Vdc	$I_F = 10$ mA
T_{rr}			4.0	nsec	$I_F = 10$ mA, $V_R = 6V$
C			4.0	pF	$V_R = 0V$
T_{fr}			2.5	Vdc	50 mA Peak Square Wave, 0.1μsec Pulse Width, 5 KC Rep. Rate, Max. Volt. Drop

SILICON EPITAXIAL PLANAR SWITCHING DIODE

The ITT JAN 1N914 diode meets MIL-S-19500/116B.

DIMENSIONS



DO-7

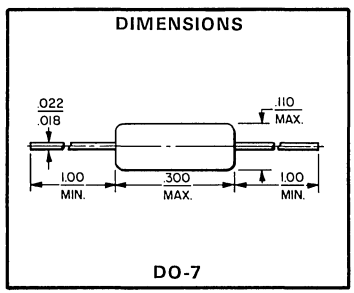
ABSOLUTE MAXIMUM RATINGS

CHARACTERISTICS @ 25°C		UNITS
Peak Inverse Voltage	100	Volts
Power Dissipation	250	mW
Storage Temperature	−65 to +200	°C
Avg. Rectified Fwd. Current	75	mA
Surge Current, 1 second	500	mA

ELECTRICAL CHARACTERISTICS @ 25°C unless otherwise noted.

SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS
PIV	100			Vdc	I_R=100μA
I_R			25 5.0 50 100	nA μA μA μA	V_R=20V V_R=75V V_R=20V, T=150°C V_R=75V, T=150°C
V_F			1.0	Vdc	I_F=10mA
C			4.0 2.8	pF pF	V_R=0V V_R=1.5V
T_{rr}			5.0	nsec	I_F=I_R=10mA, C=3pF, R_L=100Ω, Rec. to 1.0mA
T_{fr}			5.0	Vdc	50mA/20 nsec, Rep. Rate Less than 100 KC

SILICON EPITAXIAL PLANAR SWITCHING DIODE



ABSOLUTE MAXIMUM RATINGS

CHARACTERISTICS @ 25°C		UNITS
Peak Inverse Voltage	100	Volts
Power Dissipation	250	mW
Storage Temperature	−65 to +200	°C
Avg. Rect. Fwd. Current	75	mA
Surge Current, 1 sec.	500	mA

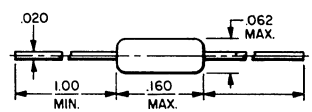
ELECTRICAL CHARACTERISTICS @ 25°C unless otherwise noted.

SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS
PIV	100			Vdc	I_R=100 μA
I_R			5.0 .025 50	μA μA μA	V_R=75V V_R=20V V_R=20V, T=150°C
V_F			1.0	Vdc	I_F=10 mA
T_{rr}			4.0	nsec	I_F=10 mA, V_R=6V
C			2.0	pF	V_R=0V
T_{fr}			2.5	Vdc	50 mA Peak Square Wave, 0.1μsec Pulse Width, 5KC Rep. Rate, Max. Volt. Drop.

SILICON EPITAXIAL PLANAR DIODE

ONE PIECE GLASS—HERMETICALLY SEALED

DIMENSIONS



DOUBLE PLUG DIODE

ABSOLUTE MAXIMUM RATINGS

CHARACTERISTICS @ 25°C:		UNITS
Storage Temperature Range	—65 to 200	°C
Lead Temperature 1/16 ± 1/32" from case for 10 sec	300	°C
Continuous Reverse Operating Voltage	75	Volts
Power Dissipation	500	mW
Derating Factor	2.85	MW/°C

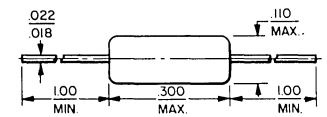
ELECTRICAL CHARACTERISTICS @25°C unless otherwise noted

CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	CONDITION
Peak Inverse Voltage	75			V	5μa
Peak Inverse Voltage	100			V	100μa
Forward Voltage			1.0	V	10mA
Reverse Current			25	na	20V
Reverse Current		150	50	μa	20V
Capacitance			4	pf	0V
Reverse Recovery Time		Note 1	4	nsec	1mA

Note 1. If=10 mA Vr=6 V R_1=100 ohms recover to 1. mA

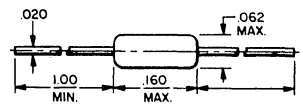
SILICON EPITAXIAL PLANAR SWITCHING DIODE

DIMENSIONS



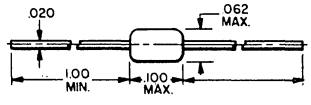
DO-7

DIMENSIONS



DOUBLE PLUG DIODE

DIMENSIONS



100 MIL PACKAGE

ABSOLUTE MAXIMUM RATINGS

CHARACTERISTICS @ 25°C		UNITS
Peak Inverse Voltage	75	Volts
Avg. Rect. Current	200	mA
Recurrent Peak Fwd. Current	900	mA
Surge Current, 1 sec.	1	Amp
Power Dissipation	500	mW
Operating Temperature	−65 to +150	°C
Storage Temperature	−65 to +175	°C

ELECTRICAL CHARACTERISTICS @ 25°C unless otherwise noted.

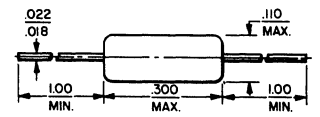
SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS
V_F	.87		1.0	Vdc	I_F=200 mA
	.82		.92	Vdc	I_F=100 mA
	.76		.86	Vdc	I_F=50 mA
	.66		.74	Vdc	I_F=10 mA
	.54		.62	Vdc	I_F=1 mA
I_R			100	nA	V_R=50V
			100	μA	V_R=50V, T=150°C
PIV	75			Vdc	I_R=5μA
C			2.5	pF	V_R=0V
T_{rr}			4.0	nsec	I_F=I_R=10 to 200 mA Rec. to 0.1 of I_F
			6.0	nsec	I_F=I_R=200 to 400 mA Rec. to 0.1 of I_F

ITT601 ITT601 DPD ITT601 MP

SILICON SWITCHING DIODE

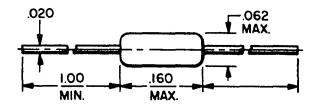
SILICON EPITAXIAL PLANAR SWITCHING DIODE

DIMENSIONS



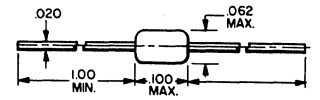
DO-7

DIMENSIONS



DOUBLE PLUG DIODE

DIMENSIONS



100 MIL PACKAGE

ABSOLUTE MAXIMUM RATINGS

CHARACTERISTICS @ 25°C		UNITS
Peak Inverse Voltage	50	Volts
Avg. Rect. Current	200	mA
Recurrent Peak Fwd. Current	900	mA
Surge Current, 1 sec.	1	Amp
Power Dissipation	500	mW
Operating Temperature	−65 to +150	°C
Storage Temperature	−65 to +175	°C

ELECTRICAL CHARACTERISTICS @ 25°C unless otherwise noted

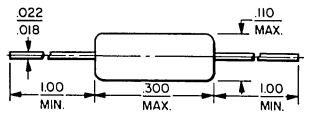
SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS
V_F			1.2	Vdc	I_F=500mA
			1.0	Vdc	I_F=400mA
	.80		.90	Vdc	I_F=200mA
	.75		.85	Vdc	I_F=100mA
	.62		.70	Vdc	I_F=10 mA
I_R			100	nA	V_R=30V
			100	μA	V_R=30V, T=150°C
PIV	50			Vdc	I_R=5μA
C			3.0	pF	V_R=0V
T_{rr}			6.0	nsec	I_F=I_R=10 mA, R_L=100Ω Rec. to 1.0 mA

SILICON EPITAXIAL PLANAR SWITCHING DIODE

ABSOLUTE MAXIMUM RATINGS

CHARACTERISTICS @ 25°C		UNITS
Peak Inverse Voltage	30	Volts
Avg. Rect. Current	50	mA
Recurrent Peak Fwd. Current	150	mA
Surge Current, 1 sec.	150	mA
Power Dissipation	250	mW
Power Derating Factor	2	mW/°C
Operating Temperature	−65 to +150	°C
Storage Temperature	−65 to +175	°C

DIMENSIONS



DO-7

ELECTRICAL CHARACTERISTICS @ 25°C unless otherwise noted.

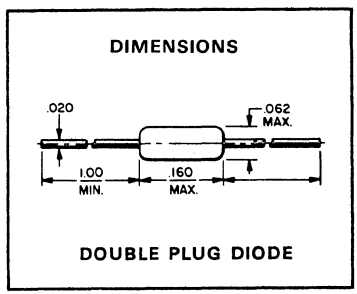
SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS
PIV	30			Vdc	$I_R = 5\mu A$
V_F	.89 .81 .76 .64 .52 .42		1.1 .95 .88 .74 .61 .50	Vdc Vdc Vdc Vdc Vdc Vdc	$I_F = 50$ mA $I_F = 20$ mA $I_F = 10$ mA $I_F = 1$ mA $I_F = 100\mu A$ $I_F = 10\mu A$
I_R			50 50	nA μA	$V_R = 15V$ $V_R = 15V$, T = 150°C
C			.75	pF	$V_R = 0V$
T_{rr}			700	psec	$I_F = I_R = 10$ mA, 100Ω Pulse Gen., .25 nsec Detector .1 nsec; Rec. to 1.0 mA

ITT2001 ITT2002 ITT2003

SILICON SWITCHING DIODE

SILICON EPITAXIAL PLANAR SWITCHING DIODE

For General Purpose High-Voltage Applications



MAXIMUM RATINGS @ 25°C (NOTE 1)

	ITT 2001	ITT 2002	ITT 2003
Peak Inverse Voltage	100 Volts	200 Volts	250 Volts
Average Rectified Current	150 ma	150 ma	150 ma
Forward Current Steady State D.C.	250 ma	250 ma	250 ma
Recurrent Peak Forward Current	400 ma	400 ma	400 ma
Peak Forward Surge Current Pulse Width of 1.0 Second	1.0 A	1.0 A	1.0 A
Power Dissipation	300 mw	300 mw	300 mw
Power Derating	3.3 mw/°C	3.3 mw/°C	3.3 mw/°C
Operating Temperature	−65°C to +175°C	−65°C to +175°C	−65°C to +175°C
Storage Temperature, Ambient	−65°C to +200°C	−65°C to +200°C	−65°C to +200°C

ITT2001 — ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
VF	Forward Voltage		1.0	Volts	IF=100 ma
IR_1	Reverse Current		0.1	ua	VR=50 V
IR_2	Reverse Current (150°C)		100	ua	VR=50 V
BV	Breakdown Voltage	100		Volts	IR=100 ua
Qs	Store Charge (Note 2)		500	pc	IF=10 ma
Co	Capacitance		5.0	pf	VR=0 V, f=1 MHz

NOTES: 1. The maximum ratings are limiting values above which life or satisfactory performance may be impaired.
2. This test is equivalent to Trr @ IF = IR = 30 ma, RL — 100 ohms, recovered to 3 ma to be less than 50 nsec.

ITT2002 — ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
VF	Forward Voltage		1.0	Volts	IF = 100 ma
IR_1	Reverse Current		0.1	ua	VR = 150 V
IR_2	Reverse Current (150°C)		100	ua	VR = 150 V
BV	Breakdown Voltage	200		Volts	IR = 100 ua
Qs	Storage Charge (Note 2)		500	pc	IF = 10 ma
Co	Capacitance		5.0	pf	VR = 0 V, f = 1 MHz

ITT2003 — ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

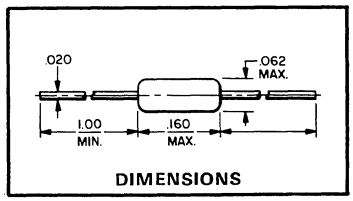
SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
VF	Forward Voltage		1.0	Volts	IF = 100 ma
IR_1	Reverse Current		0.1	ua	VR = 150 V
IR_2	Reverse Current (150°C)		100	ua	VR = 150 V
BV	Breakdown Voltage	250		Volts	IR = 100 ua
Qs	Store Charge (Note 2)		500	pc	IF = 10 ma
Co	Capacitance		5.0	pf	VR = 0 V, f = 1 MHz

ITT3001 ITT3002 ITT3003®

SILICON PLANAR DIODE

HIGH VOLTAGE HIGH TEMPERATURE DOUBLE PLUG DIODE

For General Purpose, High-Temperature, High-Voltage Applications



DIMENSIONS

MAXIMUM RATINGS (25°C) NOTE 1

	3001	3002	3003
Peak Inverse Voltage	70 Volts	150 Volts	200 Volts
Average Rectified Current	100 ma	100 ma	100 ma
Forward Current Steady State D.C.	200 ma	200 ma	200 ma
Recurrent Peak Forward Current	300 ma	300 ma	300 ma
Peak Forward Surge Current Pulse Width of 1.0 Second	1.0 A	1.0 A	1.0 A
Power Dissipation	250 mw	250 mw	250 mw
Power Derating	2.0 mw/°C	2.0 mw/°C	2.0 mw/°C
Operating Temperature	−65°C to +175°C	−65°C to +175°C	−65°C to +175°C
Storage Temperature, Ambient	−65°C to +200°C	−65°C to +200°C	−65°C to +200°C

ITT 3001 — ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
VF	Forward Voltage		1.0	Volts	IF = 100 ma
IR_1	Reverse Current		0.025	ua	VR = 60 V
IR_2	Reverse Current (150°C)		5	ua	VR = 60 V
BV	Breakdown Voltage	70		Volts	IR = 100 ua
Co	Capacitance		8	pf	VR = 0 V, f = 1 MHz

NOTES:
1. The maximum ratings are limited values above which life or satisfactory performance may be impaired.
2. All Diodes must have black body coat.

ITT3002 — ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
VF	Forward Voltage		1.0	Volts	IF = 200 ma
IR_1	Reverse Current		1.0	na	VR = 125 V
IR_2	Reverse Current (150°C)		3.0	ua	VR = 125 V
BV	Breakdown Voltage	150		Volts	IR = 100 ua
Co	Capacitance		6.0	pf	VR = 0 V, f = 1 MHz

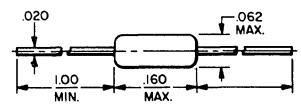
ITT3003 — ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
VF	Forward Voltage		1.0	Volts	IF = 100 ma
IR_1	Reverse Current		.025	ua	VR = 175 V
IR_2	Reverse Current (150°C)		5	ua	VR = 175 V
BV	Breakdown Voltage	200		Volts	IR = 100 ua

GENERAL PURPOSE SILICON DIODE

This device is a Silicon Double Plug Diode for general-purpose, high-temperature application in computer, industrial and military applications.

DIMENSIONS



DOUBLE PLUG DIODE

ABSOLUTE MAXIMUM RATINGS

Storage temperature range, T_{stg} ..... −55°C to +200°C

Lead or terminal temperature at a distance not less than 1/16" from the seated surface (or case) for 2 seconds ..... +275°C

	1N5194	1N5195	1N5196
Reverse voltage, 25°C free air	80 V	200 V	250 V
Maximum steady state power dissipation at 25°C, free air	250mw	250mw	250mw
Derating factor	1.43mw/°C	1.43mw/°C	1.43mw/°C

ELECTRICAL CHARACTERISTICS

	1N5194		1N5195		1N5196	
	MIN	MAX	MIN	MAX	MIN	MAX
Forward Voltage, Vf @ If = 100 ma		1.0 V		1.0 V		1.0 V†
Breakdown Voltage, Bvr Ir = 100 ua	80 V		200 V		250 V	
Reverse Current, Ir @ Vr = 70 V		25 na		25 na*		25 na*
Reverse Current, Ir @ Vr = 70 V @ 150°C		5 ua		5 ua*		5 ua*

† Pulsed—width 8.5 msec max duty cycle 2% or less

* Vr=180V

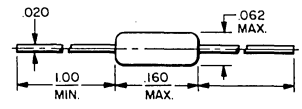
* Vr=225V

CROSS-REFERENCE TO ELECTRICAL EQUIVALENTS

DO-7 TYPES	DPD TYPES
IN483B	IN5194
IN485B	IN5195
IN486B	IN5196

GENERAL PURPOSE SILICON DIODES

This device is a Silicon Double Plug Diode for general purpose use in computer, industrial and military applications.



DIMENSIONS

ABSOLUTE MAXIMUM RATINGS

Storage temperature range, T_{stg} ..... −65°C to +200°C

Lead or terminal temperature at a distance not less than 1/16″ from the seated surface (or case) for 15 seconds ..... +275°C

	1N5605	1N5606	1N5607	1N5608/9
Reverse voltage, 25°C free air	70 V	150 V	200 V	120 V
Maximum steady state power dissipation at 25°C, free air	250mw	200mw	200mw	250mw
Derating factor				2mw/°C

ELECTRICAL CHARACTERISTICS

	1N5605		1N5606*		1N5607*	
	MIN	MAX	MIN	MAX	MIN	MAX
Forward Voltage, Vf @ If = 20 ma		1.0 V		1.0 V		1.0 V
Breakdown Voltage, Bvr Ir = 100 ua	70 V		150 V		200 V	
Reverse Current, Ir @ Vr = 60 V		25 na		25 na		25 na
Reverse Current, Ir @ Vr = 60 V @ 150°C ..		5 ua		5 ua		5 ua

* If = 7 ma, Vr = 125 V * If = 3 ma, Vr = 175 V

ELECTRICAL CHARACTERISTICS — 1N5608	MIN	MAX
Forward Voltage, Vf @ If = 100 ma		1.0 V
Breakdown Voltage, Bvr		
Ir — 100 ua	120 V	
Reverse Current, Ir @ 50 V		50 na
Reverse Current, Ir @ 50 V @ 150°C		25 ua
*Reverse Recovery Time, Trr		
If = 5 ma, Vr = 40 V		
R1 = 2 K, C1 = 10 pf		
Recover to 80K ohms		300 nsec

ELECTRICAL CHARACTERISTICS — 1N5609	MIN	MAX
Forward Voltage, Vf @ If = 6 ma		1.0 V
Breakdown Voltage, Bvr		
Ir = 100 ua	120 V	
Reverse Current, Ir @ 100 V		5 ua
Reverse Current, Ir @ 100 V @ 100°C		50 ua
Capacitance, C		
Vr = 10 V, f = 1 mc		2.7 pf
Reverse Recovery time, Trr		
If = 30 ma, Vr = 35 V,		
Recover to 400K ohms		300 nsec

CROSS-REFERENCE TO ELECTRICAL EQUIVALENTS

DO-7 TYPES	DPD TYPES
1N457	1N5605
1N458	1N5606
1N459	1N5607
1N658	1N5608
1N660	1N5609

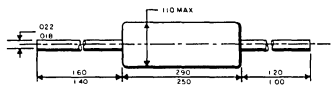
GOLD BOND GERMANIUM DIODES

HOW TO USE THIS BUYING GUIDE

Standard general purpose diodes are listed in numerical order below. Each diode has a line number referenced to the specification tables on pages 2, 3 and 4. Use this buying guide two ways: select the diode by type number, or locate the type number from the specification data.

ITT is the world's leading producer of diodes. Call your ITT sales engineer or distributor for quotation on all your diode needs.

Part No.	Line No.	Part No.	Line No.	Part No.	Line No.	Part No.	Line No.	Part No.	Line No.
1N34	107	1N87	37	1N198B	195	1N497	56	1N3125	69
1N34A	100	1N87A	38	1N265	180	1N498	116	1N3146	45
1N35	78	1N88	169	1N266	98	1N499	147	1N3287	2
1N38	201	1N89	189	1N267	41	1N500	158	1N3287W	3
1N38A	191	1N90	138	1N268	50	1N501	207	USN	
1N38B	192	1N95	140	1N270	166	1N502	219	1N3465	119
1N44	211	1N96	143	1N270JAN	167	1N527	11	1N3466	75
1N45	133	1N96A	111	1N273	55	1N541	76	1N3467	24
1N46	84	1N97	203	1N276	110	1N542	77	1N3468	25
1N47	212	1N98	206	1N276JAN	91	1N567	208	1N3469	63
1N48	172	1N98A	239	1N277	220	1N568	5	1N3470	64
1N49	85	1N99	202	1N277JAN	200	1N569	21	1N3483	9
1N50	86	1N100	205	1N278	108	1N571	20	1N3592	43
1N51	79	1N100A	156	1N279	58	1N616	32	1N3666	165
1N52	173	1N102	229	1N281	148	1N617	210	1N3666M	161
1N52A	171	1N103	15	1N283	47	1N618	213	USN	
1N54	60	1N104	16	1N287	109	1N631	186	1N3666M1	162
1N54A	87	1N107	14	1N288	177	1N632	184	USN	
1N55	234	1N108	93	1N289	175	1N633	222	1N3666M2	163
1N55A	235	1N111	129	1N290	215	1N634	214	USN	
1N55B	238	1N112	130	1N291	217	1N635	236	1N3769	185
1N56	51	1N113	122	1N292	149	1N636	97	1N3773	40
1N56A	72	1N114	123	1N294	126	1N695	34	1N4523	27
1N57	153	1N115	124	1N294A	127	1N695A	42	1N4524	12
1N58	199	1N116	137	1N297	151	1N770	31	G158	26
1N58A	197	1N117	139	1N297A	152	1N771	157	G159	62
1N60	88	1N118	142	1N298	131	1N771A	164	G198	46
1N60A	68	1N118A	146	1N298A	52	1N771B	168	G199	36
1N61	233	1N119	103	1N314	141	1N772	159	G200	29
1N62	209	1N120	105	1N355	193	1N772A	132	G766	35
1N63	227	1N126	136	1N367	23	1N773	120	G788	96
1N63A	196	1N126A	145	1N417	99	1N773A	121	G790	28
1N65	170	1N127	226	1N418	106	1N774	114	G814	19
1N66	101	1N127A	230	1N419	160	1N774A	118	G815	59
1N66A	102	1N128	82	1N447	144	1N775	115	G816	13
1N67	154	1N128A	83	1N448	216	1N776	33	G819	187
1N67A	190	1N133	1	1N449	92	1N777	117	G820	112
1N68	188	1N139	90	1N450	218	1N781	70	G821	65
1N68A	232	1N140	176	1N451	237	1N781A	71	G822	49
1N69	135	1N141	174	1N452	94	1N805	67	G823	39
1N69A	134	1N142	228	1N453	221	1N909	113	G824	30
1N70	224	1N143	231	1N454	150	1N910	74	G825	17
1N70A	225	1N144	57	1N455	95	1N911	54	G844	48
1N71	73	1N145	53	1N476	178	1N933	204	G846	61
1N75	223	1N191	182	1N477	179	1N946	89	G847	10
1N81	20	1N192	128	1N478	198	1N994	8	G868	4
1N81A	81	1N195	66	1N479	181	1N995	22	G869	6
1N84	18	1N198	155	1N480	104	1N996	44		
1N86	125	1N198A	194	1N490	183	1N3110	7		



DIMENSIONS DO-7 (Standard)

MECHANICAL DATA

Case:
Hermetically sealed glass

Finish:
All external surfaces corrosion resistant and leads readily solderable

Leads:
Dumet, tin plated

Weight:
0.135 grams (approx.)

Mounting Position:
Any

Marking:
Diodes carry ITT identification, and are EIA Color Coded. Bands 1, 2, 3 and 4 on the illustration above indicate the first, second, third and fourth digit respectively of the type designation, starting from the cathode end of the diode.

Black.....0	Green.....5
Brown.....1	Blue.....6
Red.....2	Violet.....7
Orange.....3	Gray.....8
Yellow.....4	White.....9

ELECTRICAL CHARACTERISTICS @ 25°C unless otherwise noted

PIV	I_F mA @ V		I_R μA @ V		Reverse Recovery Time I_FmA	V_R	Rec.to	nsec	Part No.	Line No.
5	3	0.5	300	0.6					1N133	1
6	1	0.3	15	2					1N3287	2
6	100	1	15	2					1N3287W USN	3
6	100	1	15	2					G868	4
7	5	0.32	100	5					1N568	5
7	10	0.5	5	2					G869	6
8	5	0.45	20	8					1N3110	7
			100	8@65°C						
8	10	1	30	6	10	−6	3mA	2	1N994	8
8	10	0.6	10	3					1N3483	9
9	50	0.9	10	5	10		3mA	8	G847	10
10	1	0.3	50	10					1N527	11
10	10	0.65	12	6	10	−6		3	1N4524	12
10	10	0.65	12	6	10		10mA	3	G816	13
10	150	1	200	10					1N107	14
12	30	1	100	5					1N103	15
12	30	1	100	5					1N104	16
12	50	0.7	6	5	10		3mA	6	G825	17
12	60	1	100	5					1N84	18
12	100	0.85	15	5					G814	19
12	200	1	100	10@55°C	100	−5	10kΩ	4	1N571	20
12	250	0.5	50	10					1N569	21
15	10	0.5	10	6	10	−6	3mA	6	1N995	22
15	20	1							1N367	23
15	20	0.5	15	10	10	−6	1Ω	2	1N3467	24
15	20	0.5	60	10	10	−6	1Ω	2	1N3468	25
15	25	0.5	40	15	10	−6	1Ω	2	G158	26
15	100	1	30	10	10	−6		8	1N4523	27
15	100	1	30	10	10		1mA	8	G790	28
15	100	0.65	20	10	2			40	G200	29
18	50	0.76	8	5	2		0V	100	G824	30
20	5	0.42	40	10	5	−10	15[1]	350	1N770	31
20	8	1	400	20					1N616	32
20	50	1	200	10					1N776	33
			500	30						
20	100	1	2	10	5	−20	25kΩ	300	1N695	34
			20	10@70°C						
20	100	0.85	25	10	10		1	50	G766	35
20	100	0.7	10	10	2			50	G199	36
22.5	0.1	0.25	30	1.5					1N87	37
22.5	0.1	0.25	(subminiature 1N87)						1N87A	38
24	50	0.65	5	5	2	2	0V	80	G823	39
25	2	0.35	4	3	2	2mA	0V	40	1N3773	40
25	3.5	1	12	10					1N267	41
25	10	1	2	10			0.2mA[3]	300	1N695A	42
			20	10@70°C						
25	15	0.5	4	4.5	2	0.2mA[2]		40	1N3592	43
25	40	0.8	15	5	5	−10	0.5mA	300	1N996	44
25	50	1	100	20	10	−6	3kΩ	2	1N3146	45
25	100	0.75	5	10	2			60	G198	46
25	200	1	20	10					1N283	47
25	300	1	20	6					G844	48
27	50	0.7	6	5	2		0V	350	G822	49
30	2.5	1	20	10					1N268	50
30	15	1	300	30					1N56	51
30	30	2	250	40					1N298A	52
30	40	1	100	10					1N145	53

PIV	I_F mA @ V		I_R μA @ V		Reverse Recovery Time I_FmA	V_R	Rec.to	nsec	Part No.	Line No.
30	100	1	10	10					1N911	54
30	100	1	20	20					1N273	55
30	100	1	20	20					1N497	56
30	100	1	200	100					1N144	57
30	100	1	200	20					1N279	58
30	100	0.85	30	20					G815	59
35	5	1	10	10					1N54	60
			100	50						
35	100	1	10	10	10		1mA	150	G846	61
35	600	1	60	20					G159	62
35	600	0.5	15	20					1N3469	63
35	600	0.5	30	20					1N3470	64
36	50	0.62	4	5	2		0V	250	G821	65
40	2	2	10	40				300	1N195	66
40	3	1	100	10					1N805	67
40	4	1	60	10					1N60A	68
40	5	0.4	100	40					1N3125	69
			125	20@71°C						
40	10	0.45	5	10	10	−10	0.1mA	500	1N781	70
			60	10@65°C						
40	10	0.45	5	10	10	−10	100μA	500	1N781A	71
			60	10@65°C						
40	15	1	300	30					1N56A	72
40	15	1	300	30					1N71	73
40	100	1	10	10					1N910	74
40	200	1	15	30					1N3466	75
45	10	2.2	18	10					1N541	76
			150	30						
45	10	2.2	18	10	(matched pair 1N541)				1N542	77
			150	30						
50			200	50	(matched pair)				1N35	78
50	2.5	1	1600	50					1N51	79
50	3	1	10	10					1N81	80
50	3	1	10	10					1N81A	81
50	3	1	10	10					1N128	82
50	3	1	10	10					1N128A	83
50	3	1	1500	50					1N46	84
50	4	1	200	20					1N49	85
50	4	1	80	20					1N50	86
50	5	1	7	10					1N54A	87
			100	50						
50	5	1	40	20					1N60	88
50	10	0.34	10	10					1N949	89
			50	10@55°C						
50	20	1	1500	50					1N139	90
50	40	1	20	10	5	−40		300	1N276JAN	91
			100	10@75°C						
50	50	1	30	30					1N449	92
50	50	1	200	50					1N108	93
50	100	1	30	30					1N452	94
50	300	1	30	30					1N455	95
55	150	1	5	10					G788	96
60	2.5	1	10	10					1N636	97
60	4	1	75	30					1N266	98
60	5	3.54			5	−40		300	1N417	99
60	5	1	30	10					1N34A	100
			500	50						

NOTES: 1. Modified IBM Test Circuit 2. I_R 3. JAN Test Circuit 4. @+55°C

PIV	I_F mA @ V		I_R μA @ V		Reverse Recovery Time I_FmA	V_R	Rec.to	nsec	Part No.	Line No.
60	5	1	50	10					1N66	101
			800	50						
60	5	1	50	10					1N66A	102
60	5	1	125	50@55°C	30	−35	50kΩ	500	1N119	103
60	5	1	125	50@55°C	(solder-in 1N119)				1N480	104
60	5	1	250	50@55°C	30	−35	50kΩ	500	1N120	105
60	7	1			5	−40	2kΩ	300	1N418	106
60	8.5	1	15	10					1N34	107
			800	50						
60	20	1	125	50@75°C					1N278	108
60	20	1	1500	50					1N287	109
60	40	1	100	50					1N276	110
			100	10@75°C						
60	40	1	500	50					1N96A	111
60	50	0.7	6	5					G820	112
60	100	1	10	10					1N909	113
60	100	1	15	10					1N774	114
			150	50						
60	100	1	20	10					1N775	115
			250	50						
60	100	1	25	40					1N498	116
60	100	1	25	10	30	−40	400Ω[1]		1N777	117
			125	50@55°C						
60	200	1	15	10					1N774A	118
			150	50						
60	200	1	20	45					1N3465	119
65	100	1	10	10					1N773	120
			100	50						
65	200	1	10	10					1N773A	121
			100	50						
70[3]	2.5	1	25	10@55°C					1N113	122
			125	50@55°C						
70[3]	2.5	1	50	10@55°C					1N114	123
			250	50@55°C						
70[3]	2.5	1	100	10@55°C					1N115	124
			500	50@55°C						
70	4	1	50	10					1N86	125
			833	50						
70	5	1	10	10					1N294	126
			800	50						
70	5	1	10	10					1N294A	127
70	5	1	20	10	30	−35	50kΩ	500	1N192	128
			50	70@50°C						
70[4]	5	1	25	10@55°C					1N111	129
			125	50@55°C						
70[4]	5	1	50	10@55°C					1N112	130
			250	50@55°C						
70	30	2	250	40					1N298	131
70	200	1	50	50					1N772A	132
75	3	1	410	50					1N45	133
75	5	1	30	10					1N69A	134
			500	50						
75	5	1	50	10					1N69	135
			850	50						
75	5	1	50	10					1N126	136
			800	50						
75	5	1	100	50					1N116	137
75	5	1	800	50					1N90	138

PIV	I_F mA @ V		I_R μA @ V		Reverse Recovery Time I_FmA	V_R	Rec.to	nsec	Part No.	Line No.
75	10	1	100	50					1N117	139
75	10	1	800	50					1N95	140
75	15	1	50	10					1N314	141
75	20	1	100	50					1N118	142
75	20	1	800	50					1N96	143
75	25	1	20	10					1N447	144
			60	30						
75	25	1	50	10					1N126A	145
			850	50						
75	40	1	100	50					1N118A	146
75	100	1	30	50					1N499	147
75	100	1	30	10	5	−40		300	1N281	148
			500	50						
75	100	1	200	50					1N292	149
75	200	1	50	50					1N454	150
80	3.5	1	10	5					1N297	151
			100	50						
80	3.5	1	10	5					1N297A	152
			100	50						
80	3.6	1	300	75					1N57	153
80	4	1	5	5					1N67	154
80	4	1	10	10					1N198	155
			250	50@75°C						
80	40	1	50	50					1N100A	156
80	100	1	25	50					1N771	157
80	100	1	40	60					1N500	158
80	100	1	50	50					1N772	159
80	125	1	180	90	5	−40		300	1N419	160
80	200	1	10	20	30	−10		300	1N3666M USN	161
			150	20@70°C						
80	200	1	10	20	30	−10		300	1N3666M1 USN	162
			150	20@70°C						
80	200	1	10	20	30	−10		300	1N3666M2 USN	163
			150	20@70°C						
80	200	1	25	50					1N771A	164
80	200	1	25	50	30	−10	500μA	300	1N3666	165
80	200	1	100	50	5	−40		300	1N270	166
80	200	1	100	50					1N270JAN	167
			75	10@75°C						
80	400	1	25	50					1N771B	168
85	2.5	1	100	50					1N88	169
85	2.5	1	200	50					1N65	170
85	4	1	150	50					1N52A	171
85	4	1	833	50					1N48	172
85	5	1	150	50					1N52	173
85	20	1	50	50					1N141	174
85	20	1	50	50					1N289	175
85	40	1	300	50					1N140	176
85	40	1	350	50					1N288	177
90	2.5	1	11	10					1N476	178
			60	10@60°C						
90	2.5	1	11	10					1N477	179
			60	10@60°C						
90	3.2	1	100	60					1N265	180
90	5	1	7	10					1N479	181
90	5	1	25	10	30	−35	50kΩ	500	1N191	182
			125	50@55°C						
90	5	1	250	50@55°C	(solder-in 1N120)				1N490	183

NOTES: 1. Modified IBM Test Circuit 2. I_R 3. JAN Test Circuit 4. @+55°C

ELECTRICAL CHARACTERISTICS, continued

PIV	I_F mA @ V		I_R μA @ V		Reverse Recovery Time I_FmA	V_R	Rec.to	nsec	Part No.	Line No.
90	7	1	120	60	5	−40	0.5mA	300	1N632	184
90	25	0.5	5	5					1N3769	185
			20	65						
90	50	3.5	120	60	5	−40	0.5mA	300	1N631	186
90	50	0.62	4	5					G819	187
100	3	1	625	100					1N68	188
100	3.5	1	8	5					1N89	189
100	4	1	5	5					1N67A	190
			50	50						
100	4	1	6	3					1N38A	191
			500	100						
100	4	1	6	3					1N38B	192
			500	100						
100	4	1	10	10					1N355	193
			50	50						
100	4	1	10	10					1N198A	194
			75	10@75°C						
100	4	1	50	50	2	−6	50k	300	1N198B	195
			250	50@75°C						
100	4	1	50	50					1N63A	196
100	4	1	600	100					1N58A	197
100	5	1	7	10					1N478	198
100	5	1	800	100					1N58	199
100	5	0.5	10	10					1N277JAN	200
			250	50@75°C						
100	7.5	1	25	10					1N38	201
100	10	1	50	50					1N99	202
100	10	1	100	50					1N97	203
100	14	1	10	10	5	−40	0.5mA[3]	400	1N933	204
			75	10@75°C						
100	20	1	5	50					1N100	205
100	20	1	100	50					1N98	206
100	100	1	40	80					1N501	207
100	150	1	150	100					1N567	208
110	5	1	700	125					1N62	209
115	3	1	11	10					1N617	210
			35	75@60°C						

PIV	I_F mA @ V		I_R μA @ V		Reverse Recovery Time I_FmA	V_R	Rec.to	nsec	Part No.	Line No.
115	3	1	410	50					1N44	211
115	5	1	4	3					1N47	212
			400	50						
115	5	1	70	10					1N618	213
115	50	1	45	45					1N634	214
			100	100						
120	5	1	100	100					1N290	215
120	25	1	30	30					1N448	216
120	40	1	100	100					1N291	217
120	50	1	30	30					1N450	218
			100	100						
120	100	1	50	100					1N502	219
120	100	1	75	10@75°C					1N277	220
120	100	1	100	100					1N453	221
120	125	1	180	90	5	−40	0.5mA[3]	300	1N633	222
125	2.5	1	50	50					1N75	223
125	3	1	25	10					1N70	224
			300	50						
125	3	1	25	10					1N70A	225
			300	50						
125	3	1	25	10					1N127	226
			300	50						
125	4	1	50	50					1N63	227
125	5	1	100	100					1N142	228
125	15	1	3	25					1N102	229
125	25	1	25	10					1N127A	230
			300	50						
125	40	1	100	100					1N143	231
130	3	1	625	100					1N68A	232
130	5	1	300	100					1N61	233
			700	125						
150	3	1	800	150					1N55	234
150	4	1	500	150					1N55A	235
165	50	1	175	150					1N635	236
170	50	1	150	150					1N451	237
190	5	1	500	150					1N55B	238
250	40	1	100	50					1N98A	239

NOTES: 1. Modified IBM Test Circuit 2. I_R 3. JAN Test Circuit 4. @+55°C

INTRODUCTION

ITT has a wide selection of planar transistor chips and wafers available for those who require devices in this form. Since the large number of JEDEC specifications are derived from a few chip types, many differing applications can be satisfied with a relatively small quantity of basic chip families.

SPECIFICATIONS

The accompanying DC parameters identifying each family are tested on each chip in the wafer. These are the probe specifications. As shipped from our factory, THE PROBE PARAMETERS ARE GUARANTEED TO AN AQL = 2.5%.

The design parameters such as $V_{CE(SAT)}$, t_{on}, t_{off}, C_{ob}, etc. are not probed. These characteristics can best be tested after the chip is suitably mounted; and, therefore, have little significance in chip form.

The chips will have a high yield to the specified limits. The actual yield will vary with the mechanical techniques used to assemble the device, and the type of package used.

In all cases, the lowest useable voltage and the lowest useable h_{FE} should be chosen in specifying chip parameters. This will provide the highest possible yield and the most economical design.

USE

The entire wafer is manufactured with approximately 3000 A° of gold for die attach to a suitable substrate or base. Recommended die attach temperature for all families is 450°C, maximum. 9,000 to 12,000 angstroms of aluminum are deposited on the chip for metalization purposes. ITT recommends aluminum wire for connection to the aluminum base and emitter bonding pads. Ultrasonic techniques may be used for the wire-bond operation.

PACKAGING FOR SHIPMENT

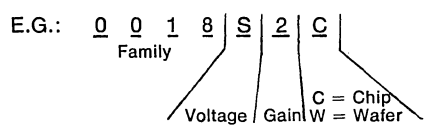
Chips will be shipped in appropriate containers, with the devices packaged to protect them from damage in shipment. Wafers will be shipped in a similar manner. Unless otherwise specified, wafers will not be scribed prior to shipment.

CROSS REFERENCE CHART

The list of JEDEC specifications, together with the respective chip specification, will provide a means of ordering the proper chip required in an application. This chart is not exhaustive, and is provided as a guide. Specific requirements may necessitate a different chip specification from available JEDEC "2N" numbers. In such cases, the accompanying list of chip parameters will provide the necessary information.

ORDERING

All chips and wafers should be ordered according to the alpha-numeric coding system referred to in the specification chart. The four-digit geometry family, together with the voltage letter and DC gain number (from the accompanying geometry parameter chart) will completely determine the specification which ITT will provide. A third letter specifies in which form, chip or wafer, the product is to be shipped.



IDENTIFICATION

All small-signal transistor dice will be identified by the appropriate four-digit family number together with the particular classification code for voltage and current gain.

By way of example:

The 2N2222 is a "0018" chip. The voltage class is "M," the current gain is "A." Therefore, when ordering a 2N2222 in chip or wafer form, the correct part would be a "0018MA" chip. This method applies to dice and to a wafer which has been tested 100%.

If a wafer is needed which does not require all the chips to be tested, then the alpha-numeric suffix will apply. For a 2N2222 device, in wafer form, sample probe-tested only, the proper part number will be a "0018S1."

TRANSISTOR WAFER INSPECTION CRITERIA

MECHANICAL INSPECTION

Measure overall thickness of one (1) wafer if run contains five (5) or less wafers. Measure two (2) wafers if run size is greater than six (6) wafers. Reject the run if any of the measured wafers are not per limits specified in Table I.

Q.C. will 100% measure overall thickness of each wafer in a rejected run.

VISUAL INSPECTION

Inspect ten (10) randomly selected devices on each wafer with no more than three (3) die in any one quadrent using 100X magnification.

TABLE I

UNAIDED EYE INSPECTION

1. Backside gold — the backside gold must cover 90% of the wafer surface. The gold must exhibit a gold, orange, or yellow cast. The gold must show no evidence of peeling or blistering.

MECHANICAL INSPECTION

1. The wafer thickness must be per the following:

   1250 2.6—3.2 mils (67-82 microns)—1½" wafer
   1243
   1718 4.0—4.6 mils (117-133 microns) —2" wafer 1250, 1243
   0016
   1211
   1312
   1913
   All others 4.6—5.2 mils (117-133 microns)

Microscope Inspection (100X) — Combined 1.0% AQL

1. Aluminum bridging—the base metal, emitter metal, and EQR ring metal may not be connected or bridged by unetched or smeared aluminum.
2. Aluminum adherance—the aluminum may show no evidence of peeling, blistering, or flaking.
3. Aluminum color — the aluminum may not be dark brown or black.
4. Aluminum reduction — aluminum fingers must be continuous along 75% of the oxide cutout length nearest the bond pad on metal over oxide devices. Aluminum fingers may not be reduced more than 50% of the oxide cutout width on metal over oxide devices, nor more than 25% in width at an oxide step-down point. Bond pads must not be reduced more than 25% of their intended area. EQR rings may not be discontinuous at more than one place.
5. Oxide holes—silicon may not be exposed within .0002 in. of any junction.
6. Mask misalignment — the outline of one oxide mask definition may not cross over the outline of another mask definition. Aluminum mask outlines must cover more than 50% of the intended oxide cutouts.

TRANSISTOR DIE INSPECTION CRITERIA

Inspect per Table II using 100X to combined 2.5% AQL.

TABLE II

1. Broken die — broken corners, edges, or shell chips may not extend closer than .001" to a junction or bond pad.
2. Cracks—cracks which are not terminated at each end at the periphery of the die may not extend toward a junction or bond pad.

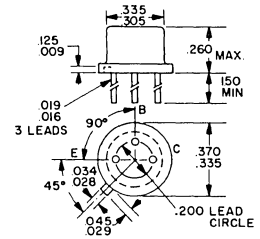
GENERAL PURPOSE NPN SILICON PLANAR EPITAXIAL TRANSISTOR

For Improved Performance See ITT 2N2217.

ABSOLUTE MAXIMUM RATINGS

CHARACTERISTICS		UNITS
Collector-to-Base Voltage	60	Volts
Collector-to-Emitter Voltage	35	Volts
Emitter-to-Base Voltage	5	Volts
Operating Junction Temperature . . 2N697	200	°C
Operating Junction Temperature . . 2N696	175	°C
Storage Temperature	−65 to +200	°C
P_D @ T_C = 25°C	2.0	Watts
P_D @ T_A = 25°C	0.6	Watt

DIMENSIONS



TO-5

ELECTRICAL CHARACTERISTICS (25°C free air unless otherwise noted)

SYMBOL	MIN.	MAX.	UNIT	CONDITIONS
BV_{CBO}	60		Vdc	I_C=100μA
LV_{CER}	40		Vdc	I_C=30mA, R_{BE}=10Ω pulsed
BV_{EBO}	5		Vdc	I_E=100μA
h_{FE} 2N697	40	120		I_C=150mA, V_{CE}=10V pulsed
h_{FE} 2N696	20	60		I_C=150mA, V_{CE}=10V pulsed
V_{CE}(sat)		1.5	Vdc	I_C=150mA, I_B=15mA pulsed
V_{BE}(sat)		1.3	Vdc	I_C=150mA, I_B=15mA pulsed
I_{CBO}		1.0	μA	V_{CB}=30V
I_{CBO}		100	μA	V_{CB}=30V, T_A=+150°C
C_{ob}		35	pF	V_{CB}=10V
h_{fe}	2			I_C=50mA, V_{CE}=10V, f=20MHz

NOTES: Pulse width ≤ 300 μsec, duty cycle ≤ 2%.

2N707

NPN SILICON EPITAXIAL TRANSISTOR

Package: TO-18

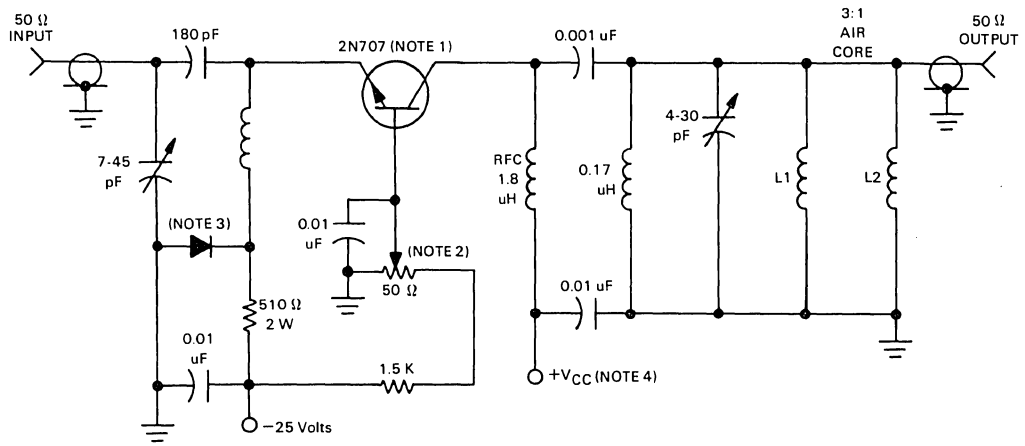
ABSOLUTE MAXIMUM RATINGS

Characteristics	Unit
Collector-Emitter Voltage	
$R_{BE} \leq 10$ ohms	28 Volts
Collector-Base Voltage	56 Volts
Emitter-Base Voltage	4 Volts
Total Device Dissipation @ $T_A = 25°C$	0.3 Watt
Derate above 25°C	2 mW/°C
Total Device Dissipation @ $T_C = 25°C$	1.0 Watt
Derate above 25°C	6.67 mW/°C
Operating and Storage Junction Temperature Range	−65 to +175°C

ELECTRICAL CHARACTERISTICS ($T_A = 25°C$ unless otherwise noted)

Symbol	Min	Typ	Max	Unit	Conditions
BV_{CER}	28	–	–	Volts	$I_C = 10$ mA, $R_{BE} = 10$ ohms
BV_{CBO}	56	–	–	Volts	$I_C = 10\,\mu A$, $I_E = 0$
I_{CBO}	–	0.005	5.0	μA	$V_{CB} = 15$ Volts, $I_E = 0$
I_{CBO}	–	3.0	–	μA	$V_{CB} = 15$ Volts, $I_E = 0$, $T_A = 150°C$
I_{EBO}	–	–	10	μA	$V_{BE} = 4$ Volts, $I_C = 0$
h_{FE}	9	12	–	–	$I_C = 10$ mA, $V_{CE} = 1$ Volt
$V_{CE(sat)}$	–	0.18	0.6	Volt	$I_C = 10$ mA, $I_B = 1$ mA
$V_{BE(sat)}$	–	0.75	0.9	Volt	$I_C = 10$ mA, $I_B = 1$ mA
f_T	70	350	–	MHz	$I_E = 15$ mA, $V_{CE} = 10$ Volts
f_{max}	–	600	–	MHz	Maximum Frequency of Oscillation
C_{ob}	–	4.0	10.0	pF	$V_{CB} = 10$ Volts, $I_E = 0$
$r_b'C_c$	–	80	–	ps	$I_C = 10$ mA, $V_{CB} = 10$ Volts, f = 4 MHz
P_{out}	200	300	–	mW	$V_{CE} = 20$ Volts, $P_{in} = 50$ mW
n	–	38	–	%	$V_{CE} = 28$ Volts, $I_C = 40$ mA

SCHEMATIC



L1 5 TURNS NO. 14 WIRE WOUND ON 1/2 IN DIAMETER
L2 2 TURNS NO. 14 WIRE WOUND ON L1.

NOTE 1 HEAT SINK IS REQUIRED.
NOTE 2 ADJUCT FOR CLASS C OPERATION.
NOTE 3 VERY HIGH CONDUCTANCE SILICON DIODE.
NOTE 4 ADJUST V_{CC} FOR PROPER V_{CE}

FIGURE 1 — 100 MHz, CLASS C, COMMON BASE AMPLIFIER

2N915 Ⓕ

NPN SILICON HIGH FREQUENCY AMPLIFIER TRANSISTOR

Package : TO-18

The ITT 2N915 is a NPN double-diffused silicon planar transistor. This unit is designed for low-power non-saturating switching circuits and low-noise VHF amplifier and oscillator applications.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Characteristics	Unit
Collector-Base Voltage	70 Volts
Collector-Emitter Voltage (Note 4)	50 Volts
Emitter-Base Voltage	5.0 Volts
Total Device Dissipation @:	
T_C = 25°C (Notes 2 and 3)	1.2 Watts
T_C = 100°C (Notes 2 and 3)	0.68 Watt
T_A = 25°C (Notes 2 and 3)	0.36 Watt
Storage Temperature	−65°C to +300°C
Operating Junction Temperature	200°C Maximum
Lead Temperature (Soldering, No Time Limit)	300°C Maximum

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Min	Typ	Max	Unit	Conditions
h_{FE}	50	110	200	–	I_C = 10 mA, V_{CE} = 5.0 Volts (Note 5)
$V_{BE(sat)}$	–	0.77	0.9	Volt	I_C = 10 mA, I_B = 1.0 mA
$V_{CE(sat)}$	–	0.45	1.0	Volt	I_C = 10 mA, I_B = 1.0 mA
h_{fe}	2.5	3.6	–	–	I_C = 10 mA, V_{CE} = 15 Volts
C_{ob}	–	3.0	3.5	pf	I_E = 0, V_{CB} = 10
K_{TE}	–	6.5	10	pf	I_C = 0, V_{EB} = 0.5 Volt
I_{CBO}	–	0.8	10	nA	I_E = 0, V_{CB} = 60 Volts
$I_{CBO(150°C)}$	–	0.5	30	μA	I_E = 0, V_{CB} = 60 Volts
BV_{CBO}	70	–	–	Volts	I_E = 0, I_C = 100 μA
$V_{CEO(sust)}$	50	–	–	Volts	I_C = 10 mA (pulsed), I_B = 0 (Notes 4 and 5)
BV_{EBO}	5.0	–	–	Volts	I_E = 10 μA, I_C = 0
r_bC_c	–	170	300	psec	I_C = 10 mA, V_{CB} = 10 Volts

SMALL SIGNAL CHARACTERISTICS (f = 1 kc)

Symbol	Min	Typ	Max	Unit	Conditions
h_{fe}	40	115	200	–	I_C = 1.0 mA, V_{CE} = 5.0 Volts
	50	140	250	–	I_C = 5.0 mA, V_{CE} = 5.0 Volts
h_{ie}	–	3.0	6.0	Kohms	I_C = 1.0 mA, V_{CE} = 5.0 Volts
	–	0.7	2.0	Kohms	I_C = 5.0 mA, V_{CE} = 5.0 Volts
h_{oe}	–	12	75	μmho	I_C = 1.0 mA, V_{CE} = 5.0 Volts
	–	45	125	μmho	I_C = 5.0 mA, V_{CE} = 5.0 Volts

NOTES:

(1) These ratings are limiting values above which the serviceability of any individual semiconductor device may be impaired.

(2) These are steady state limits. The factory should be consulted on applications involving pulsed or low duty cycle operation.

(3) These ratings give a maximum junction temperature of 200°C and junction-to-case thermal resistance of 145°C/watt (derating factor of 6.9 mW/°C); junction-to-ambient thermal resistance of 486°C/watt (derating factor of 2.06 mW/°C).

(4) Rating refers to a high-current point where collector-to-emitter voltage is lowest.

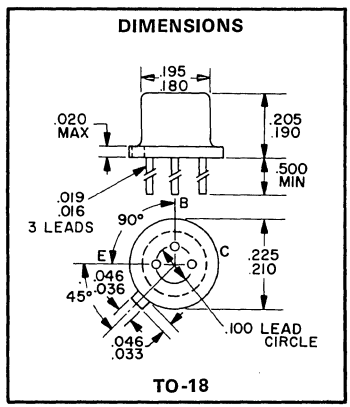
(5) Pulse Conditions: length = 300 μsec; duty cycle = 1%.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Min	Typ	Max	Unit	Conditions
*I_{CBO}	–	0.1	10	nA	I_E = 0, V_{CB} = 30 Volts
I_{CBO}(150°C)	–	0.2	10	μA	I_E = 0, V_{CB} = 30 Volts
BV_{CBO}	45	–	–	Volts	I_C = 10 μA, I_E = 0
V_{CEO} (sust)	25	–	–	Volts	I_C = 10 mA (pulsed), I_B = 0 (Notes 4 and 5)
$r_b'C_c$	–	200	300	psec	I_C = 10 mA, V_{CB} = 10 Volts

LOW LEVEL LOW NOISE NPN SILICON PLANAR TRANSISTORS

- **High Gain; 100 min. @ I_C=10 μA**
- **Low Noise; 3dB max. @ I_C=10 μA**
- **High V_{CEO}; 45 Vdc min.**



The ITT 2N929 and 2N930 are NPN silicon planar transistors designed for application in low noise, low level amplifiers in the audio through high frequency range.

ABSOLUTE MAXIMUM RATINGS

CHARACTERISTICS		UNITS
Collector-to-Base Voltage	45	Volts
Collector-to-Emitter Voltage (open base)	45	Volts
Emitter-to-Base Voltage	5.0	Volts
Collector Current (continuous)	30	mA
Junction Temperature (operating)	−65 to +175	°C
(storage)	−65 to +200	°C
Total Power Dissipation @ T_C=25°C (derate 4.0 mW/°C above 25°C)	0.6	Watts
Total Power Dissipation @ T_A=25°C (derate 2.0 mW/°C above 25°C)	0.3	Watts

ELECTRICAL CHARACTERISTICS @ 25°C unless otherwise noted

SYMBOL	MIN.	MAX.	UNIT	CONDITIONS
LV_{CEO}	**45**		**Vdc**	**I_C=10mA**
BV_{EBO}	5.0		Vdc	I_E=10nA
h_{FE}	**40** **100**	**120** **300**		**I_C=10μA V_{CE}=5.0V** **2N929** **2N930**
	60 150			I_C=500μA V_{CE}=5.0V 2N929 2N930
		350 600		I_C=10mA V_{CE}=5.0V 2N929 2N930
	10 20			I_C=10μA V_{CE}=5.0V T_A=−55°C 2N929 2N930
$V_{CE}(sat)$[1]		1.0	Vdc	I_C=10mA I_B=0.5mA
$V_{BE}(sat)$[1]	0.6	1.0	Vdc	I_C=10mA I_B=0.5mA
I_{CBO}		10	nA	V_{CB}=45V
I_{CEO}		2	nA	V_{CE}=5V
I_{EBO}		10	nA	V_{EB}=5V
I_{CES}		10	nA	V_{CE}=45V
I_{CES}		10	μA	V_{CE}=45V T_A=170°C
C_{ob}		8	pF	V_{CB}=5V
h_{fe}	60 150	350 600		I_C=1.0mA V_{CE}=5V f=1KHz 2N929 2N930
	1.0	1.0		I_C=500μA V_{CE}=5V f=30mHz
h_{ib}	25	32	ohms	I_C=1.0mA V_{CB}=5V f=1mHz
h_{ob}		1.0	μmho	I_C=1.0mA V_{CB}=5V f=1mHz
h_{rb}		600	X10^{-6}	I_C=1.0mA V_{CB}=5V f=1mHz
NF		**4** **3**	**dB** **dB**	**I_C=10μA V_{CE}=5V R_G=10KΩ** **B.W.=200Hz f=1KHz** **2N929** **2N930**

Notes: 1. Pulse width ≤300 μsec; duty cycle ≤2%.
2. Lowest emitter to collector voltage.

HIGH-SPEED NPN SILICON, HIGH-CURRENT SWITCHING TRANSISTORS

ABSOLUTE MAXIMUM RATINGS (Note 1)

Characteristics	Unit
Collector-Base Voltage	60 Volts
Collector-Emitter Voltage (Note 4)	40 Volts
Emitter-Base Voltage	5.0 Volts
Collector Current	1.0 Amp
Total Dissipation @:	
T_C = 25°C (Notes 2 and 3)	2.8 Watts
T_C = 100°C (Notes 2 and 3)	1.6 Watts
T_A = 25°C (Notes 2 and 3)	0.8 Watt
Storage Temperature	−65°C to +300°C
Operating Junction Temperature	−65°C to +200°C
Lead Temperature (Soldering, No Time Limit)	300°C Maximum

NOTES:

(1) These ratings are limiting values above which the serviceability of any individual semiconductor may be impaired.

(2) These are steady state limits. The factory should be consulted on applications involving pulsed or low duty cycle operations.

(3) These ratings give a maximum junction temperature of 200°C and junction-to-case thermal resistance of 62.5°C/watt (derating factor of 16mW/°C), junction-to-ambient thermal resistance of 219°C/watt (derating factor of 4.56mW/°C).

(4) Rating refers to a high-current point where collector-to-emitter voltage is lowest.

(5) Pulse Conditions: length ≤ 300 μsec, duty cycle ≤ 2%.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Min	Max	Unit	Conditions
h_{FE}	100	300	–	I_C = 150 mA, V_{CE} = 10 Volts (Note 5)
h_{FE}	75	–	–	I_C = 10 mA, V_{CE} = 10 Volts
h_{FE}	70	–	–	I_C = 150 mA, V_{CE} = 1.0 Volt (Note 5)
h_{FE}	35	–	–	I_C = 500 mA, V_{CE} = 10 Volts (Note 5)
$h_{FE(-55°C)}$	35	–	–	I_C = 10 mA, V_{CE} = 10 Volts
h_{FE}	15	–	–	I_C = 1.0 A, V_{CE} = 10 Volts (Note 5)
h_{FE}	15	–	–	I_C = 0.1 mA, V_{CE} = 10 Volts
$V_{CE(sat)}$	–	0.35	Volt	I_C = 150 mA, I_B = 15 mA (2N2192)
$V_{CE(sat)}$	–	0.25	Volt	I_C = 150 mA, I_B = 15 mA (2N2192A)
$V_{CE(sat)}$	–	0.18	Volt	I_C = 150 mA, I_B = 15 mA (2N2192B)
$V_{BE(sat)}$	–	1.3	Volts	I_C = 150 mA, I_B = 15 mA
h_{fe}	2.5	–	–	I_C = 50 mA, V_{CE} = 10 Volts f=20 MHz
C_{ob}	–	20	pF	I_E = 0, V_{CB} = 10 Volts
I_{CBO}	–	10	nA	I_E = 0, V_{CB} = 30 Volts

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Min	Max	Unit	Conditions
$I_{CBO(150°C)}$	–	15	μA	I_E = 0, V_{CB} = 30 Volts
I_{EBO}	–	50	nA	I_C = 0, V_{EB} = 3.0 Volts
BV_{CBO}	60	–	Volts	I_C = 100 μA, I_E = 0
$V_{CEO(sust)}$	40	–	Volts	I_C = 25 mA (pulsed), I_B = 0 (Notes 4 and 5)
BV_{EBO}	5.0	–	Volts	I_E = 100 μA, I_C = 0
t_f	–	50	nsec	See Figure 1
t_r	–	70	nsec	See Figure 1
t_s	–	150	nsec	See Figure 1

CIRCUIT DIAGRAM

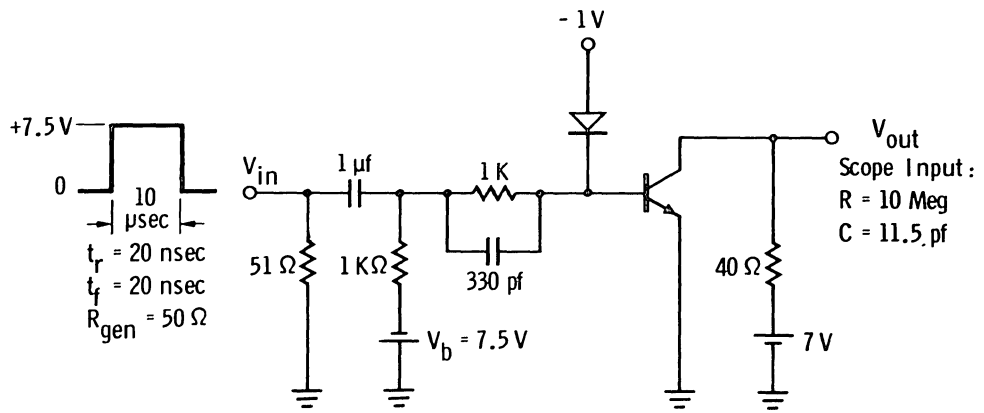


FIGURE 1

HIGH-SPEED NPN SILICON, HIGH-CURRENT SWITCHING TRANSISTORS

ABSOLUTE MAXIMUM RATINGS (Note 1)

Characteristics	Units
Collector-Base Voltage	80 Volts
Collector-Emitter Voltage (Note 4)	50 Volts
Emitter-Base Voltage	8.0 Volts
Collector Current	1.0 Amp
Total Dissipation @:	
T_C = 25°C (Notes 2 and 3)	2.8 Watts
T_C = 100°C (Notes 2 and 3)	1.6 Watts
T_A = 25°C (Notes 2 and 3)	0.8 Watt
Storage Temperature	−65°C to +300°C
Operating Junction Temperature	−65°C to +200°C
Lead Temperature (Soldering, No Time Limit)	300°C Maximum

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Min	Max	Unit	Conditions
h_{FE}	40	120	–	I_C = 150 mA, V_{CE} = 10 Volts
h_{FE}	30	–	–	I_C = 10 mA, V_{CE} = 10 Volts
h_{FE}	30	–	–	I_C = 150 mA, V_{CE} = 1.0 Volt
$h_{FE(-55°C)}$	20	–	–	I_C = 10 mA, V_{CE} = 10 Volts
h_{FE}	20	–	–	I_C = 500 mA, V_{CE} = 10 Volts
h_{FE}	15	–	–	I_C = 1.0 A, V_{CE} = 10 Volts
h_{FE}	15	–	–	I_C = 0.1 mA, V_{CE} = 10 Volts
$V_{CE(sat)}$	–	0.35	Volt	I_C = 150 mA, I_B = 15 mA (2N2193)
$V_{CE(sat)}$	–	0.25	Volt	I_C = 150 mA, I_B = 15 mA (2N2193A)
$V_{CE(sat)}$	–	0.18	Volt	I_C = 150 mA, I_B = 15 mA (2N2193B)
$V_{BE(sat)}$	–	1.3	Volts	I_C = 150 mA, I_B = 15 mA
h_{fe}	2.5	–	–	I_C = 50 mA, V_{CE} = 10 Volts f=20 MHz
C_{ob}	–	20	pF	I_E = 0, V_{CB} = 10 Volts f=1 MHz
I_{CBO}	–	10	nA	I_E = 0, V_{CB} = 60 Volts

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Min	Max	Unit	Conditions
$I_{CBO(150°C)}$	–	25	μA	I_E = 0, V_{CB} = 60 Volts
I_{EBO}	–	50	nA	I_C = 0, V_{EB} = 5.0 Volts
BV_{CBO}	80	–	Volts	I_C = 100μA, I_E = 0
$V_{CEO(sust)}$	50	–	Volts	I_C = 25 mA (pulsed), I_B = 0 (Notes 4 and 5)
BV_{EBO}	8.0	–	Volts	I_E = 100μA, I_C = 0
t_f	–	50	nsec	See Figure 1
t_r	–	70	nsec	See Figure 1
t_s	–	150	nsec	See Figure 1

NOTES:

(1) These ratings are limiting values above which the serviceability of any individual device may be impaired.

(2) These are steady state limits. The factory should be consulted on applications involving pulsed or low duty cycle operations.

(3) These ratings give a maximum junction temperature of 200°C and junction-to-case thermal resistance of 62.5°C/watt (derating factor of 16 mW/°C); junction-to-ambient thermal resistance of 219°C/watt (derating factor of 4.56 mW/°C).

(4) Rating refers to a high-current point where collector-to-emitter voltage is lowest.

(5) Pulse Conditions: length ≤ 300 usec; duty cycle ≤ 2%.

CIRCUIT DIAGRAM

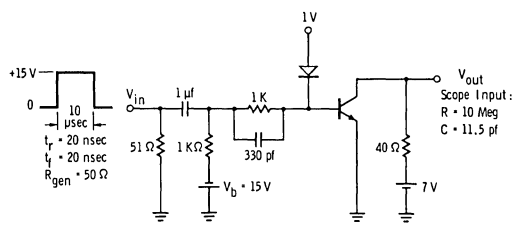


FIGURE 1

HIGH-SPEED NPN SILICON, HIGH-CURRENT SWITCHING TRANSISTORS

ABSOLUTE MAXIMUM RATINGS (Note 1)

Characteristics	Unit
Collector-Base Voltage	60 Volts
Collector-Emitter Voltage (Note 4)	40 Volts
Emitter-Base Voltage	5.0 Volts
Collector Current	1.0 Amp
Total Dissipation @:	
T_C = 25°C (Notes 2 and 3)	2.8 Watts
T_C = 100°C (Notes 2 and 3)	1.6 Watts
T_A = 25°C (Notes 2 and 3)	0.8 Watt
Storage Temperature	−65°C to +300°C
Operating Junction Temperature	−65°C to +200°C
Lead Temperature (Soldering, No Time Limit)	300°C Maximum

NOTES:

(1) These ratings are limiting values above which the serviceability of any individual device may be impaired.

(2) These are steady state limits. The factory should be consulted on applications involving pulsed or low duty cycle operations.

(3) These ratings give a maximum junction temperature of 200°C and junction-to-case thermal resistance of 62.5°C/watt (derating factor of 16 mW/°C); junction-to-ambient thermal resistance of 219°C/watt (derating factor of 4.56 mW/°C).

(4) Rating refers to a high-current point where collector-to-emitter voltage is lowest.

(5) Pulse Conditions: length ≤ 300 μsec; duty cycle ≤ 2%.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Min	Max	Unit	Conditions
h_{FE}	20	60	–	I_C = 150 mA, V_{CE} = 10 Volts (Note 5)
h_{FE}	15	–	–	I_C = 150 mA, V_{CE} = 1.0 Volt (Note 5)
h_{FE}	15	–	–	I_C = 10 mA, V_{CE} = 10 Volts
h_{FE}	12	–	–	I_C = 500 mA, V_{CE} = 10 Volts (Note 5)
$V_{CE(sat)}$	–	0.35	Volt	I_C = 150 mA, I_B = 15 mA (2N2194)
$V_{CE(sat)}$	–	0.25	Volt	I_C = 150 mA, I_B = 15 mA (2N2194A)
$V_{CE(sat)}$	–	0.18	Volt	I_C = 150 mA, I_B = 15 mA (2N2194B)
$V_{BE(sat)}$	–	1.3	Volts	I_C = 150 mA, I_B = 15 mA
h_{fe}	2.5	–	–	I_C = 50 mA, V_{CE} = 10 Volts
C_{ob}	–	20	pF	I_E = 0, V_{CB} = 10 Volts
I_{CBO}	–	10	nA	I_E = 0, V_{CB} = 30 Volts
$I_{CBO(150°C)}$	–	25	μA	I_E = 0, V_{CB} = 30 Volts
I_{EBO}	–	50	nA	I_C = 0, V_{EB} = 3.0 Volts
BV_{CBO}	60	–	Volts	I_C = 100μA, I_E = 0

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Min	Max	Unit	Conditions
$V_{CEO(sust)}$	40	–	Volts	I_C = 25 mA (pulsed), I_B = 0 (Notes 4 and 5)
BV_{EBO}	5.0	–	Volts	I_E = 100 μA, I_C = 0
t_f	–	50	nsec	See Figure 1
t_r	–	70	nsec	See Figure 1
t_s	–	150	nsec	See Figure 1

CIRCUIT DIAGRAM

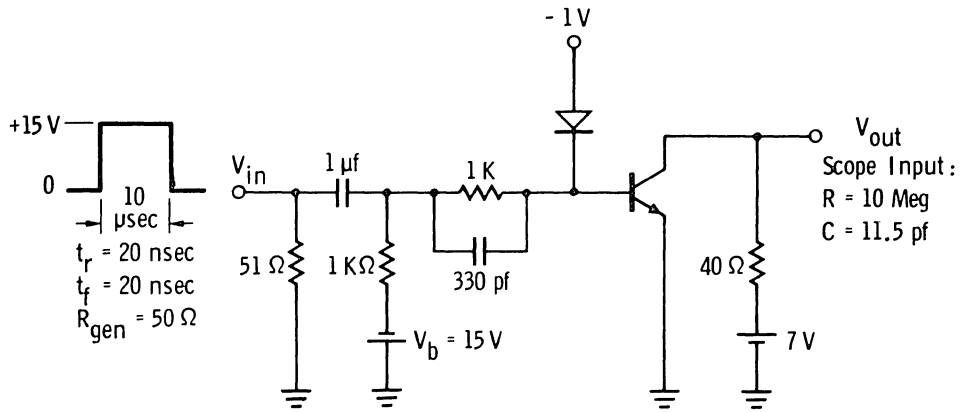


FIGURE 1

HIGH-SPEED NPN SILICON, HIGH-CURRENT SWITCHING TRANSISTORS

ABSOLUTE MAXIMUM RATINGS (Note 1)

Characteristics	Unit
Collector-Base Voltage	45 Volts
Collector-Emitter Voltage (Note 4)	25 Volts
Emitter-Base Voltage	5.0 Volts
Collector Current	1.0 Amp
Total Dissipation @:	
T_C = 25°C (Notes 2 and 3)	2.8 Watts
T_C = 100°C (Notes 2 and 3)	1.6 Watts
T_A = 25°C (Notes 2 and 3)	0.6 Watt
Storage Temperature	−65°C to +300°C
Operating Junction Temperature	−65 to +200 °C
Lead Temperature (Soldering, No Time Limit)	300°C Maximum

NOTES:

(1) These ratings are limiting values above which the serviceability of any individual semiconductor device may be impaired.

(2) These are steady state limits. The factory should be consulted on applications involving pulsed or low duty cycle operations.

(3) These ratings give a maximum junction temperature of 200°C and junction-to-case thermal resistance of 62.5°C/watt (derating factor of 16 mW/°C); junction-to-ambient thermal resistance of 292°C/watt (derating factor of 3.42 mW/°C).

(4) Rating refers to a high-current point where collector-to-emitter voltage is lowest.

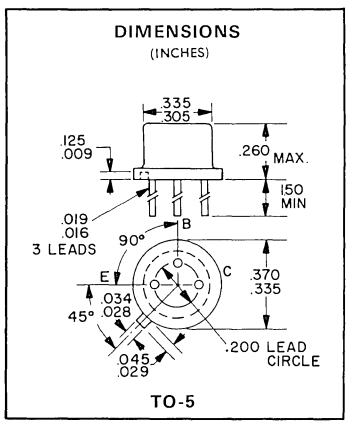
(5) Pulse Conditions: length ≤ 300 μsec, duty cycle ≤ 2%.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Min	Max	Unit	Conditions
h_{FE}	20	–	–	I_C = 150 mA, V_{CE} = 10 Volts
h_{FE}	10	–	–	I_C = 150 mA, V_{CE} = 1.0 Volt
$V_{CE(sat)}$	–	0.35	Volt	I_C = 150 mA, I_B = 15 mA (2N2195)
$V_{CE(sat)}$	–	0.25	Volt	I_C = 150 mA, I_B = 15 mA (2N2195A
$V_{CE(sat)}$	–	0.18	Volt	I_C = 150 mA, I_B = 15 mA (2N2195B)
$V_{BE(sat)}$	–	1.3	Volts	I_C = 150 mA, I_B = 15 mA
h_{fe}	2.5	–	–	I_C = 50 mA, V_{CE} = 10 Volts
C_{ob}	–	20	pF	I_E = 0, V_{CB} = 10 Volts
I_{CBO}	–	100	nA	I_E = 0, V_{CB} = 30 Volts
$I_{CBO(150°C)}$	–	50	μA	I_E = 0, V_{CB} = 30 Volts
I_{EBO}	–	100	nA	I_C = 0, V_{EB} = 3.0 Volts
BV_{CBO}	45	–	Volts	I_C = 100 μA, I_E = 0
$V_{CEO(sust)}$	25	–	Volts	I_C = 25 mA (pulsed), I_B = 0 (Notes 4 and 5)
BV_{EBO}	5.0	–	Volts	I_E = 100 μA, I_C = 0

GENERAL PURPOSE NPN SILICON PLANAR EPITAXIAL TRANSISTORS

- Low V_{CE} (sat), < 0.4 V @ I_C = 150mA
- High Frequency, f_T = 250 MHz @ I_C = 20mA
- Wide Useful Current Range, 0.1 to 500mA



TO-5

The ITT 2N2218-19 are NPN silicon planar epitaxial general purpose transistors for applications at current ranges from 0.1 to 500 mA. Low saturation voltage and fast switching times make the 2N2218-19 ideal for core driving. The flat gain over a wide current range gives good linearity in amplifier circuits. High breakdown voltage allows large signal swing in switching and amplifier circuits.

ABSOLUTE MAXIMUM RATINGS

CHARACTERISTICS		UNITS
Collector-to-Base Voltage	60	Volts
Collector-to-Emitter Voltage (open base)	30	Volts
Emitter-to-Base Voltage	5.0	Volts
Collector Current (continuous)	800	mA
Junction Temperature (operating)	−65 to +175	°C
(storage)	−65 to +200	°C
Total Power Dissipation @ T_C = 25°C (derate 20mW/°C above 25°C)	3.0	Watts
Total Power Dissipation @ T_A = 25°C (derate 5.33 mW/°C above 25°C)	0.8	Watts

ELECTRICAL CHARACTERISTICS @ 25°C unless otherwise noted

SYMBOL	MIN.	MAX.	UNIT	CONDITIONS
h_{FE} (1)				I_C=150mA, V_{CE}=10V
	40	120		2N2218
	100	300		2N2219
				I_C=150mA, V_{CE}=IV
	20			2N2218
	50			2N2219
				I_C=500mA, V_{CE}=10V
	20			2N2218
	30			2N2219
h_{FE}				I_C=10mA, V_{CE}=10V
	35			2N2218
	75			2N2219
				I_C=1mA, V_{CE}=10V
	25			2N2218
	50			2N2219
				I_C=0.1mA, V_{CE}=10V
	20			2N2218
	35			2N2219
V_{CE}(sat)(1)		**0.4**	**Vdc**	**I_C=150mA, I_B=15mA**
		1.6	Vdc	I_C=500mA, I_B=50mA
V_{BE}(sat) (1)		1.3	Vdc	I_C=150mA, I_B=15mA
		2.6	Vdc	I_C=500mA, I_B=50mA
I_{CBO}		10	nA	V_{CB}=50V, I_E=0
		10	μA	V_{CB}=50V, I_E=0, T=150°C
I_{EBO}		10	nA	V_{EB}=3V, I_C=0
f_T	**250**		**MHz**	**I_C=20mA, V_{CE}=20V**
C_{ob}		8	pf	V_{CB}=10V, I_E=0
$R_{e(hie)}$ (2)		60	Ohms	I_C=20mA, V_{CE}=20V, f=300 MHz
BV_{CBO}	60		Vdc	I_C=10μA, I_E=0
V_{CEO}(sust) (1)	30		Vdc	I_C=10mA, I_B=0
BV_{EBO}	5		Vdc	I_E=10μA, I_C=0

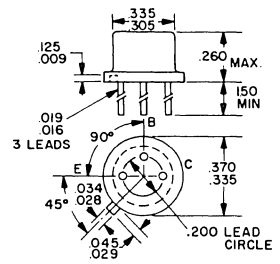
NOTES: 1. Pulse Measurement: width $\leq$ 300μsec, duty cycle $\leq$ 2%.
2. Real part of Common-Emitter high frequency input impedance..

HIGH-SPEED NPN SILICON PLANAR EPITAXIAL SATURATED SWITCHING TRANSISTOR

ABSOLUTE MAXIMUM RATINGS

CHARACTERISTICS		UNITS
Collector-to-Base Voltage	75	Volts
Collector-to-Emitter Voltage	40	Volts
Emitter-to-Base Voltage	6	Volts
Operating Junction Temperature	175	°C
Storage Temperature	−65 to +200	°C
P_D @ T_C = 25°C	3.0	Watts
P_D @ T_A = 25°C	0.8	Watts

DIMENSIONS



TO-5

ELECTRICAL CHARACTERISTICS (25°C free air unless otherwise noted)

SYMBOL	MIN.	MAX.	UNIT	CONDITIONS
BV_{CBO}	75		Vdc	I_C = 10μA
LV_{EBO}	40		Vdc	I_C = 10mA pulsed
BV_{EBO}	6		Vdc	I_E = 10μA
h_{FE}	35			I_C = 100μA, V_{CE} = 10V
h_{FE}	50			I_C = 1mA, V_{CE} = 10V
h_{FE}	75			I_C = 10mA, V_{CE} = 10V
h_{FE}	100	300		I_C = 150mA, V_{CE} = 10V pulsed
h_{FE}	40			I_C = 500mA, V_{CE} = 10V pulsed
h_{FE}	50			I_C = 150mA, V_{CE} = 1V pulsed
h_{FE}	35			I_C = 10mA, V_{CE} = 10V, T_A = −55°C
V_{CE}(sat)		0.3	Vdc	I_C = 150mA, I_B = 15mA pulsed
V_{CE}(sat)		1.0	Vdc	I_C = 500mA, I_B = 50mA pulsed
V_{BE}(sat)	0.6	1.2	Vdc	I_C = 150mA, I_B = 15mA pulsed
V_{BE}(sat)		2.0	Vdc	I_C = 500mA, I_B = 50mA pulsed
I_{CBO}		10	nA	V_{CB} = 60V
I_{CBO}		10	μA	V_{CB} = 60V, T_A = 150°C

ELECTRICAL CHARACTERISTICS continued

PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
I_{CEX}		10	nA	$V_{CE}=60V$, $V_{EB}=3V$
I_{EBX}		20	nA	$V_{EB}=3V$, $V_{CB}=60V$
I_{EBO}		10	nA	$V_{EB}=3V$
C_{ob}		8	pF	$V_{CB}=10V$
C_{ib}		25	pF	$V_{EB}=0.5V$
h_{fe}	50	300		$I_C=1mA$, $V_{CE}=10V$, f=1KHz
h_{fe}	75	375		$I_C=10mA$, $V_{CE}=10V$, f=1KHz
h_{fe}	3			$I_C=20mA$, $V_{CE}=20V$, f=100MHz
h_{ie}	2	8	K ohms	$I_C=1mA$, $V_{CE}=10V$, f=1KHz
h_{ie}	0.25	1.25	K ohms	$I_C=10mA$, $V_{CE}=10V$, f=1KHz
h_{re}		8	$x10^{-4}$	$I_C=1mA$, $V_{CE}=10V$, f=1KHz
h_{re}		4	$x10^{-4}$	$I_C=10mA$, $V_{CE}=10V$, f=1KHz
h_{oe}	5	35	μmho	$I_C=1mA$, $V_{CE}=10V$, f=1KHz
h_{oe}	25	200	μmho	$I_C=10mA$, $V_{CE}=10V$, 1f=KHz
$R_{e(hie)}$		60	omhs	$I_C=20mA$, $V_{CE}=20V$, f=300MHz
$r_b'C_C$		150	ps	$I_C=20mA$, $V_{CE}=20V$, f=31.8MHz
N.F.		4	db	$I_C=100\mu A$, $V_{CE}=10V$, $R_G=1K\Omega$, f=1KHz
T_s		2.5	ns	$I_C=150mA$, $I_{B1}=15mA$, $V_{CC}=30V$, $V_{EB}=0.5V$
t_d		10	ns	$I_C=150mA$, $I_{B1}=15mA$, $V_{CC}=30V$, $V_{EB}=0.5V$
t_r		25	ns	$I_C=150mA$, $I_{B1}=15mA$, $V_{CC}=30V$, $V_{EB}=0.5V$
t_s		225	ns	$I_C=150mA$, $I_{B1}=I_{B2}=15mA$, $V_{CC}=30V$
t_f		60	ns	$I_C=150mA$, $I_{B1}=I_{B2}=15mA$, $V_{CC}=30V$

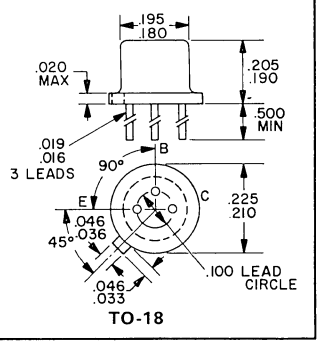
NOTE: Pulse width $\leq$ 30 μsec, duty cycle $\leq$ 2%.

GENERAL PURPOSE NPN SILICON PLANAR EPITAXIAL TRANSISTORS

- Low V_{CE} (sat), < 0.4 V @ I_C = 150mA
- High Frequency, f_T = 250 MHz @ I_C = 20mA
- Wide Useful Current Range, 0.1 to 500mA

The ITT 2N2221-22 are NPN silicon planar epitaxial general purpose transistors for applications at current ranges from 0.1 to 500 mA. Low saturation voltage and fast switching times make the 2N2221-22 ideal for core driving. The flat gain over a wide current range gives good linearity in amplifier circuits. High breakdown voltage allows large signal swing in switching and amplifier circuits.

DIMENSIONS



TO-18

ABSOLUTE MAXIMUM RATINGS

CHARACTERISTICS		UNITS
Collector-to-Base Voltage	60	Volts
Collector-to-Emitter Voltage (open base)	30	Volts
Emitter-to-Base Voltage	5.0	Volts
Collector Current (continuous)	800	mA
Junction Temperature (operating)	−65 to +175	°C
(storage)	−65 to +300	°C
Total Power Dissipation @ T_C = 25°C (derate 12mW/°C above 25°C)	1.8	Watts
Total Power Dissipation @ T_A = 25°C (derate 3.33 mW/°C above 25°C)	0.5	Watts

ELECTRICAL CHARACTERISTICS @ 25°C unless otherwise noted

SYMBOL	MIN.	MAX.	UNIT	CONDITIONS
h_{FE} (1)				I_C=150mA, V_{CE}=10V
	40	120		2N2221
	100	300		2N2222
				I_C=150mA, V_{CE}=1V
	20			2N2221
	50			2N2222
h_{FE}				I_C=500mA, V_{CE}=10V
	20			2N2221
	30			2N2222
				I_C=10mA, V_{CE}=10V
	35			2N2221
	75			2N2222
				I_C=1mA, V_{CE}=10V
	25			2N2221
	50			2N2222
				I_C=0.1mA, V_{CE}=10V
	20			2N2221
	35			2N2222
V_{CE}(sat)(1)		**0.4**	**Vdc**	**I_C=150mA, I_B=15mA**
		1.6	Vdc	I_C=500mA, I_B=50mA
V_{BE}(sat) (1)		1.3	Vdc	I_C=150mA, I_B=15mA
		2.6	Vdc	I_C=500mA, I_B=50mA
I_{CBO}		10	nA	V_{CB}=50V, I_E=0
		10	μA	V_{CB}=50V, I_E=0, T=150°C
I_{EBO}		10	nA	V_{EB}=3V, I_C=0
f_T	**250**		**MHz**	**I_C=20mA, V_{CE}=20V**
C_{ob}		8	pf	V_{CB}=10V, I_E=0
$R_{e(hie)}$ (2)		60	Ohms	I_C=20mA, V_{CE}=20V, f=300 MHz
BV_{CBO}	60		Vdc	I_C=10μA, I_E=0
V_{CEO}(sust) (1)	30		Vdc	I_C=10mA, I_B=0
BV_{EBO}	5		Vdc	I_E=10μA, I_C=0

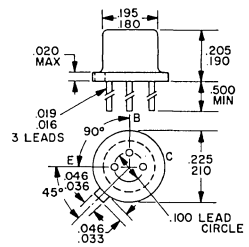
NOTES: 1. Pulse Measurement: width $\leq$ 300μsec, duty cycle $\leq$ 2%.
2. Real part of Common-Emitter high frequency input impedance.

HIGH-SPEED NPN SILICON PLANAR EPITAXIAL SATURATED SWITCHING TRANSISTOR

ABSOLUTE MAXIMUM RATINGS

CHARACTERISTICS		UNITS
Collector-to-Base Voltage	75	Volts
Collector-to-Emitter Voltage	40	Volts
Emitter-to-Base Voltage	6	Volts
Operating Junction Temperature	175	°C
Storage Temperature	−65 to +200	°C
P_D @ T_C = 25°C	1.8	Watts
P_D @ T_A = 25°C	0.5	Watt

DIMENSIONS



TO-18

ELECTRICAL CHARACTERISTICS (25°C free air unless otherwise noted)

SYMBOL	MIN.	MAX.	UNIT	CONDITIONS
BV_{CBO}	75		Vdc	I_C=10μA
LV_{CEO}	40		Vdc	I_C=10mA pulsed
BV_{EBO}	6		Vdc	I_E=10μA
h_{FE}	20			I_C=100μA, V_{CE}=10V
h_{FE}	25			I_C=1mA, V_{CE}=10V
h_{FE}	35			I_C=10mA, V_{CE}=10V
h_{FE}	40	120		I_C=150mA, V_{CE}=10V pulsed
h_{FE}	25			I_C=500mA, V_{CE}=10V pulsed
h_{FE}	20			I_C=150mA, V_{CE}=1V pulsed
h_{FE}	15			I_C=10mA, V_{CE}=10V, T_A=−55°C
V_{CE}(sat)		0.3	Vdc	I_C=150mA, I_B=15mA pulsed
V_{CE}(sat)		1.0	Vdc	I_C=500mA, I_B=50mA pulsed
V_{BE}(sat)	0.6	1.2	Vdc	I_C=150mA, I_B=15mA pulsed
V_{BE}(sat)		2.0	Vdc	I_C=500mA, I_B=50mA pulsed
I_{CBO}		10	nA	V_{CB}=60V
I_{CBO}		10	μA	V_{CB}=60V, T_A=150°C

ELECTRICAL CHARACTERISTICS continued

PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
I_{CEX}		10	nA	$V_{CE}=60V$, $V_{EB}=3V$
I_{EBX}		20	nA	$V_{EB}=3V$, $V_{CB}=60V$
I_{EBO}		10	nA	$V_{EB}=3V$
C_{ob}		8	pF	$V_{CB}=10V$
C_{ib}		25	pF	$V_{EB}=0.5V$
h_{fe}	30	150		$I_C=1mA$, $V_{CE}=10V$, f=1KHz
h_{fe}	50	300		$I_C=10mA$, $V_{CE}=10V$, f=1KHz
h_{fe}	2.5			$I_C=20mA$, $V_{CE}=20V$, f=100MHz
h_{ie}	1	3.5	K ohms	$I_C=1mA$, $V_{CE}=10V$, f=1KHz
h_{ie}	0.2	1.0	K ohms	$I_C=10mA$, $V_{CE}=10V$, f=1KHz
h_{re}		5	$x10^{-4}$	$I_C=1mA$, $V_{CE}=10V$, f=1KHz
h_{re}		2.5	$x10^{-4}$	$I_C=10mA$, $V_{CE}=10V$, f=1KHz
h_{oe}	3	15	μmho	$I_C=1mA$, $V_{CE}=10V$, f=1KHz
h_{oe}	10	100	μmho	$I_C=10mA$, $V_{CE}=10V$, f=1KHz
$R_{e(hie)}$		60	ohms	$I_C=20mA$, $V_{CE}=20V$, f=300MHz
$r_b'C_C$		150	ps	$I_C=20mA$, $V_{CE}=20V$, f=31.8MHz
τ_s		2.5	ns	$I_C=150mA$, $I_{B1}=15mA$, $V_{CC}=30V$, $V_{EB}=0.5V$
t_d		10	ns	$I_C=150mA$, $I_{B1}=15mA$, $V_{CC}=30V$, $V_{EB}=0.5V$
t_r		25	ns	$I_C=150mA$, $I_{B1}=15mA$, $V_{CC}=30V$, $V_{EB}=0.5V$
t_s		225	ns	$I_C=150mA$, $I_{B1}=I_{B2}=15mA$, $V_{CC}=30V$
t_f		60	ns	$I_C=150mA$, $I_{B1}=I_{B2}=15mA$, $V_{CC}=30V$

NOTES: Pulse width $\leq$ 300 μsec, duty cycle $\leq$ 2%.

Package: TO-18

2N2242
HIGH-SPEED SILICON SATURATED SWITCHING TRANSISTOR

ABSOLUTE MAXIMUM RATINGS

Characteristics	Unit
Collector-Emitter Voltage	15 Volts
Collector-Base Voltage	40 Volts
Emitter-Base Voltage	5.0 Volts
Collector Current — Continuous	225 mA
Total Device Dissipation @ T_A = 25°C	360 mW
Derate above 25°C	2.0 mW/°C
Junction Temperature — Operating	−65 to +200° C
Storage Temperature Range	−65 to +200° C

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

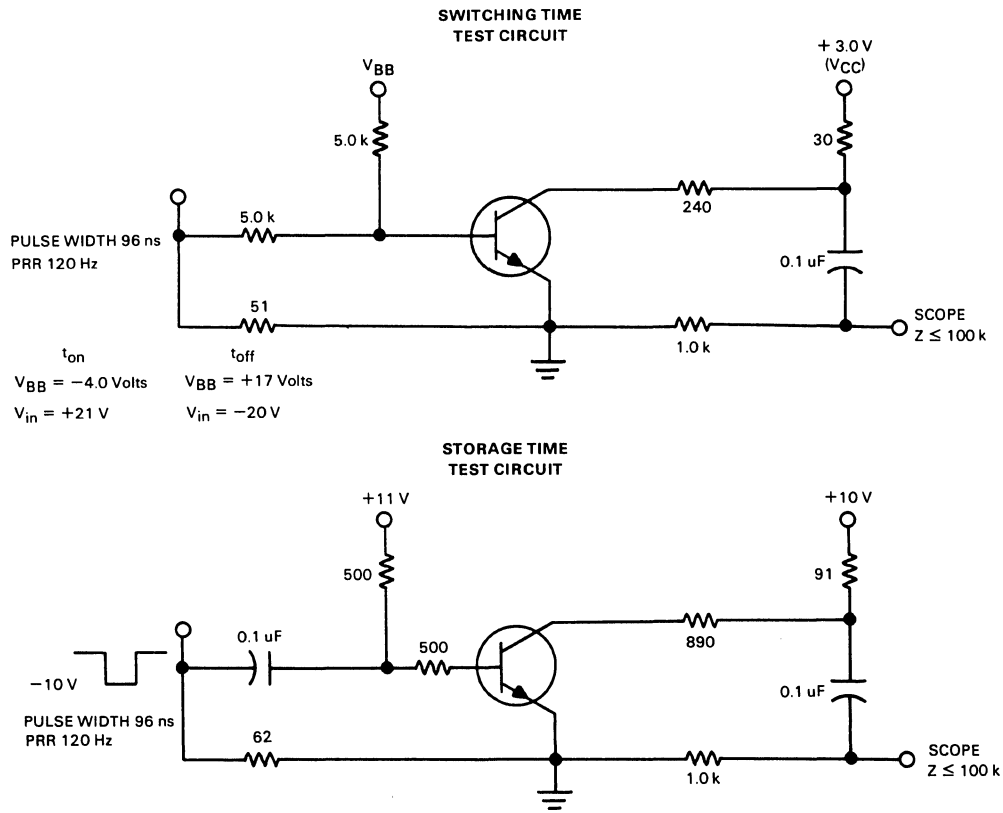
Symbol	Min	Max	Unit	Conditions
BV_{CEO}*	15	–	Volts	I_C = 30 mA, I_E = 0*
BV_{CER}*	20	–	Volts	I_C = 30 mA, R_{BE} = ≤ 10 ohms*
BV_{CBO}	40	–	Volts	I_C = 1.0 μA, I_E = 0
BV_{EBO}	5.0	–	Volts	I_E = 10 μA, I_C = 0
I_{CEX}	–	10	μA	V_{CE} = 20 Volts, $V_{EB(off)}$ = 0.25 Volt, T_A = 125°C
I_{CBO}	–	0.1	μA	V_{CB} = 20 Volts, I_C = 0
I_{CBO}	–	15	μA	V_{CB} = 20 Volts, I_E = 0, T_A = 150°C
I_{EBO}	–	0.1	μA	$V_{EB(off)}$ = 4.0 Volts, I_C = 0
h_{FE}*	40	120	–	I_C = 10 mA, V_{CE} = 1.0 Volt*
h_{FE}*	20	–	–	I_C = 10 mA, V_{CE} = 1.0 Volt, T_A = -55°C
$V_{CE(sat)}$	–	0.7	Volt	I_C = 100 mA, I_B = 10 mA
$V_{CE(sat)}$	–	0.3	Volt	I_C = 10 mA, I_B = 1.0 mA, T_A = -55 to +125°C
$V_{BE(sat)}$	–	1.5	Volts	I_C = 100 mA, I_B = 10 mA
$V_{BE(sat)}$	–	0.8	Volt	I_C = 10 mA, I_B = 1.0 mA, T_A = 125°C
f_T	250	–	MHz	I_C = 20 mA, V_{CE} = 10 Volts, f = 100 MHz
C_{ob}	–	6.0	pF	V_{CB} = 10 Volts, I_E = 0, f = 1.0 MHz

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Min	Max	Unit	Conditions
t_{on}	–	30	ns	V_{CC} = 3.0 Volts, $V_{BE(off)}$ = +2.0 Volts, I_{B1} = 3.0 mA, I_C = 10 mA
t_{off}	–	50	ns	V_{CC} = 3.0 Volts, I_C = 10 mA, I_{B1} = 3.0 mA, I_{B2} = 1.0 mA
t_s	–	25	ns	I_C = 10 mA, I_{B1} = I_{B2} = 10 mA

* Pulse Test: Pulse Width = 300 μs; Duty Cycle = ≤ 2%

CIRCUIT DIAGRAM



Package: TO-5

NPN HIGH-CURRENT GENERAL PURPOSE SILICON PLANAR TRANSISTOR

The ITT 2N2297 is an NPN double-diffused silicon planar epitaxial transistor with very low saturation resistance, high-current capabilities, typical gain-bandwidth product of 90 megacycles, low C_{ob} and low leakage currents.

This transistor is designed for use in high-performance dc-dc converters, oscillators, high-current memory drivers and computer clock distribution circuits. The 2N2297 is suitable in particular for output stages of servo amplifiers and transceivers where several watts output at high effiency is required.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Characteristics	Unit
Collector-Base Voltage	80 Volts
Collector-Emitter Voltage (Note 4)	35 Volts
Emitter-Base Voltage	7.0 Volts
Total Dissipation @:	
T_C = 25°C (Notes 2 and 3)	5.0 Watts
T_C = 100°C (Notes 2 and 3)	2.8 Watts
T_A = 25°C (Notes 2 and 3)	0.8 Watt
Storage Temperature	−65°C to +300°C
Operating Junction Temperature	200°C Maximum
Lead Temperature (Soldering, No Time Limit)	300°C Maximum

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Min	Typ	Max	Unit	Conditions
h_{FE}	40	55	120	–	I_C = 150 mA, V_{CE} = 10 Volts (Note 5)
$V_{CE(sat)}$	–	0.15	0.2	Volt	I_C = 150 mA, I_B = 15 mA
$V_{CE(sat)}$	–	0.8	1.0	Volt	I_C = 1000 mA, I_B = 100 mA (Note 6)
$V_{CE(sat)}$	–	1.4	1.6	Volts	I_C = 1000 mA, I_B = 100 mA
I_{CBO}	–	0.1	10	nA	I_E = 0, V_{CB} = 60 Volts
I_{EBO}	–	–	10	nA	I_C = 0, V_{EB} = 5.0 Volts
BV_{CBO}	80	–	–	Volts	I_E = 0, I_C = 100 μA
$V_{CEO(sust)}$	35	–	–	Volts	I_B = 0 (pulsed) I_C = 30 mA (Notes 4 and 5)

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Min	Typ	Max	Unit	Conditions
h_{FE}	30	50	–	–	I_C = 10 mA, V_{CE} = 10 Volts (Note 5)
h_{FE}	15	30	–	–	I_C = 1.0 A, V_{CE} = 10 Volts (Note 5)
I_{CBO}(150°C)	–	0.2	10	μA	V_{CB} = 60 Volts, I_E = 0
f_T	60	95	–	mc	I_C = 50 mA, V_{CE} = 10 Volts
C_{ob}	–	8.0	12	pf	V_{CB} = 10 Volts, I_E = 0
C_{TE}	–	53	80	pf	V_{EB} = 0.5 Volt, I_C = 0
BV_{EBO}	7.0	–	–	Volts	I_E = 100 μA, I_C = 0
$r_b'C_c$	–	–	800	psec	I_C = 10 mA, V_{CB} = 10 Volts

NOTES:

(1) These ratings are limiting values above which the serviceability of any individual semiconductor device may be impaired.

(2) These are steady state limits. The factory should be consulted on applications involving pulsed or low duty cycle operations.

(3) These ratings give a maximum junction temperature of 200°C and junction-to-case thermal resistance of 35°C/watt (derating factor of 28.6 mW/°C); junction-to-ambient thermal resistance of 218°C/watt (derating factor of 4.6 mW/°C).

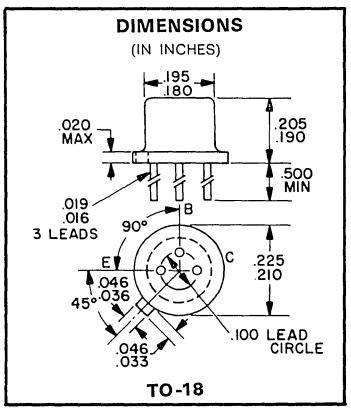
(4) Rating refers to a high-current point where collector-to-emitter voltage is lowest.

(5) Pulse Conditions: length = 300 μsec; duty cycle ≤ 1%.

(6) Measured at a point on the leads ≤ 1/2 inch from the seating plane of transistor case.

LOW LEVEL LOW NOISE NPN SILICON PLANAR TRANSISTORS

- **High Gain; 100 Min. @ I_c=10μA (2N2484)**
- **Low noise; 3dB Max. @ I_c=10μA**
- **High V_{CEO}; 60 Vdc Min.**



TO-18

The ITT 2N2483 and 2N2484 are NPN silicon planar transistors designed for application in low-noise, low-level, high-gain amplifiers in the audio through high frequency range.

ABSOLUTE MAXIMUM RATINGS

CHARACTERISTICS		UNITS
Collector-to-Base Voltage	60	Volts
Collector-to-Emitter Voltage (open base)	60	Volts
Emitter-to-Base Voltage	6	Volts
Collector Current	50	mA
Junction Temperature (op. and stg.)	−65 to +200	°C
Total Power Dissipation @ T_C=25°C	1.2	Watts
(derate 6.9 mW/°C above 25°C)		
@ T_C=100°C	0.68	Watts
Total Power Dissipation @ T_A=25°C	0.36	Watts
(derate 2.1 mW/°C above 25°C)		

ELECTRICAL CHARACTERISTICS @ 25°C unless otherwise noted.

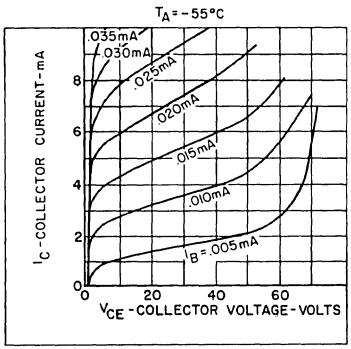
SYMBOL	2N2483 MIN.	2N2483 TYP.	2N2483 MAX.	2N2484 MIN.	2N2484 TYP.	2N2484 MAX.	UNIT	CONDITIONS
BV_{CBO}	60			60			Vdc	$I_C=10\mu A$
LV_{CEO}[1,2]	**60**			**60**			**Vdc**	**$I_C=10mA$**
BV_{EBO}	6.0			6.0			Vdc	$I_C=10\mu A$
h_{FE}				30	200			$I_C=1\mu A$ $V_{CE}=5V$
	40	**80**	**120**	**100**	**290**	**500**		**$I_C=10\mu A$ $V_{CE}=5V$**
	75	140		175	375			$I_C=100\mu A$ $V_{CE}=5V$
	100	200		200	430			$I_C=500\mu A$ $V_{CE}=5V$
	175	230		250	450			$I_C=1mA$ $V_{CE}=5V$
		280	500		430	800		$I_C=10mA$ $V_{CE}=5V$
	10			20				$I_C=10\mu A$ $V_{CE}=5V$ $T_A=-55°C$
$V_{CE}(sat)$		0.2	0.35		0.2	0.35	Vdc	$I_C=1mA$ $I_B=0.1mA$
$V_{BE}(on)$	0.5	0.57	0.7	0.5	0.57	0.7	Vdc	$I_C=100\mu A$ $V_{CE}=5V$
I_{CBO}		0.1	10		0.1	10	nA	$V_{CB}=45V$
		0.2	10		0.2	10	μA	$V_{CB}=45V$ $T_A=150°C$
I_{CEO}		0.1	2.0		0.1	2.0	nA	$V_{CE}=5V$
I_{EBO}		0.1	10		0.1	10	nA	$V_{EB}=5V$
C_{ob}		3.5	6.0		3.5	6.0	pF	$V_{CB}=5V$ f=1mHz
C_{ib}		3.5	6.0		3.5	6.0	pF	$V_{EB}=0.5V$ f=1mHz
h_{fe}	2.4	4.0		3.0	4.0			$I_C=50\mu A$ $V_{CE}=5V$ f=5mHz
	2.0	2.3		2.0	2.6			$I_C=500\mu A$ $V_{CE}=5V$ f=30mHz
	80	280	450	150	400	900		$I_C=1mA$ $V_{CE}=5V$ f=1KHz
h_{ie}	1.5	7.5	13	3.5	15	24	Kohms	$I_C=1mA$ $V_{CE}=5V$ f=1KHz
h_{oe}		11	30		15	40	μmho	$I_C=1mA$ $V_{CE}=5V$ f=1KHz
h_{re}		300	800		425	800	$X10^{-6}$	$I_C=1mA$ $V_{CE}=5V$ f=1KHz
h_{ib}	25	27	32	25	27	32	ohms	$I_C=1mA$ $V_{CE}=5V$ f=1KHz
NF		**1.9**	**4.0**		**1.8**	**3.0**	**dB**	**$I_C=10\mu A$ $V_{CE}=5V$ $R_G=10K\Omega$ B.W.=15.7KHz 3dB @ 10Hz & 10KHz**
		1.9	**4.0**		**1.8**	**3.0**	**dB**	**$I_C=10\mu A$ $V_{CE}=5V$ $R_G=10K\Omega$ f=1KHz B.W.=200Hz (Note 3)**
		0.7	**3.0**		**0.6**	**2.0**	**dB**	**$I_C=10\mu A$ $V_{CE}=5V$ $R_G=10K\Omega$ f=10KHz B.W.=2KHz (Note 3)**
		4.0	**15**		**4.0**	**10**	**dB**	**$I_C=10\mu A$ $V_{CE}=5V$ $R_G=10K\Omega$ f=100Hz B.W.=20Hz (Note 3)**

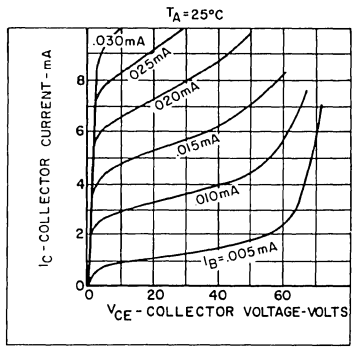
Notes: 1. Pulsed width ≤300 μsec; duty cycle ≤2%.
2. Lowest emitter to collector voltage.
3. Narrow band noise.

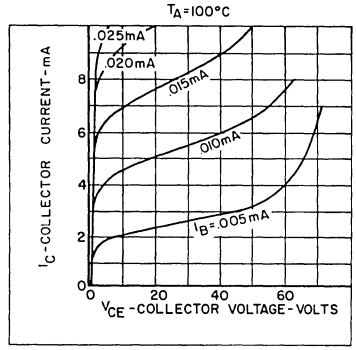
TYPICAL CHARACTERISTICS

2N2483

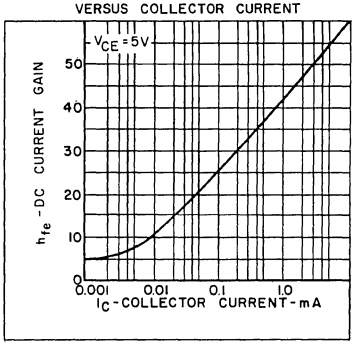
COLLECTOR CHARACTERISTICS



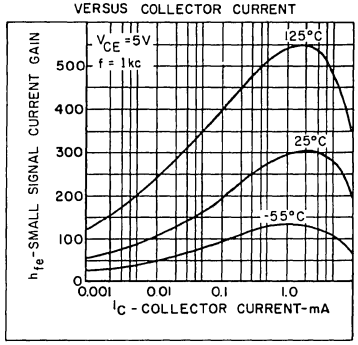




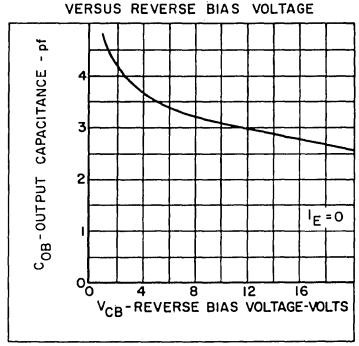
MINIMUM DC CURRENT GAIN AT -55°C
VERSUS COLLECTOR CURRENT



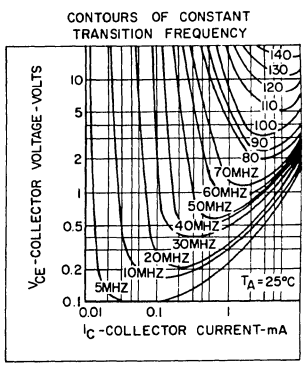
SMALL SIGNAL CURRENT GAIN
VERSUS COLLECTOR CURRENT



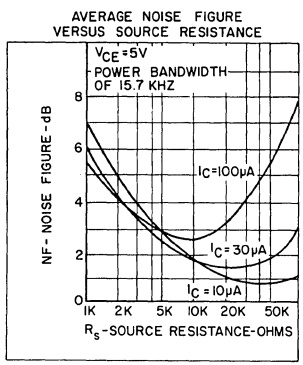
OUTPUT CAPACITANCE
VERSUS REVERSE BIAS VOLTAGE



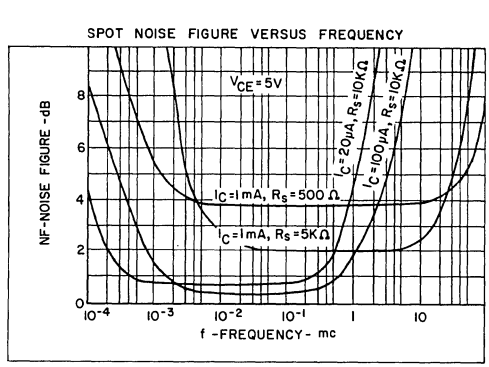
CONTOURS OF CONSTANT
TRANSITION FREQUENCY



AVERAGE NOISE FIGURE
VERSUS SOURCE RESISTANCE



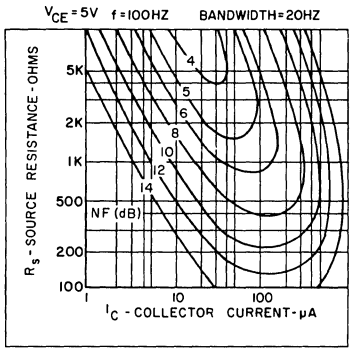
SPOT NOISE FIGURE VERSUS FREQUENCY

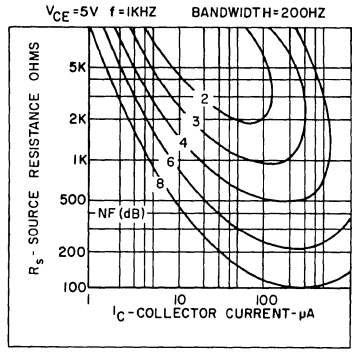


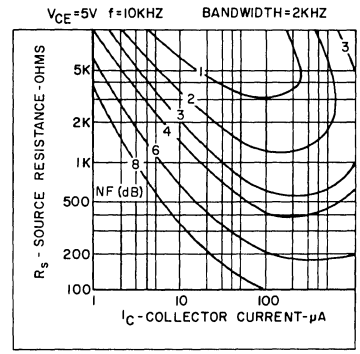
TYPICAL CHARACTERISTICS, continued

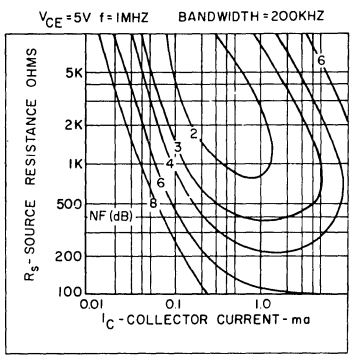
2N2483

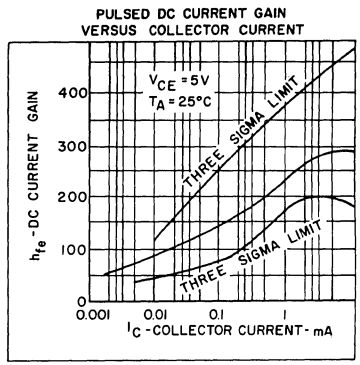
CONSTANT NOISE FIGURE CONTOURS

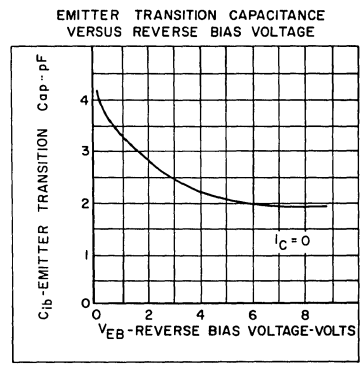




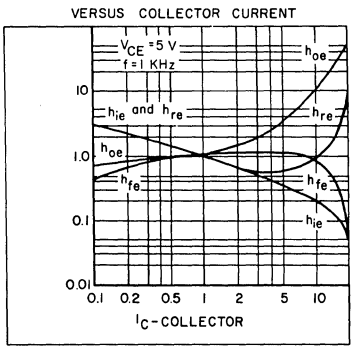


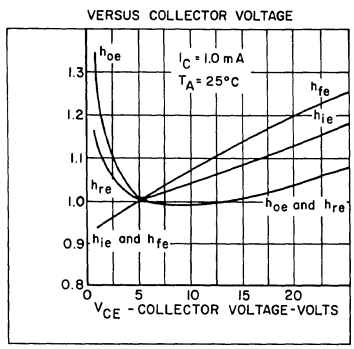


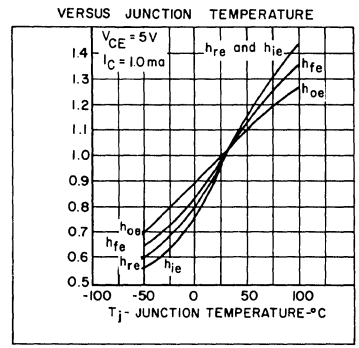




NORMALIZED COMMON EMITTER TRANSFER CHARACTERISTICS



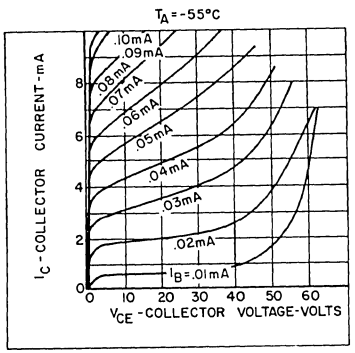


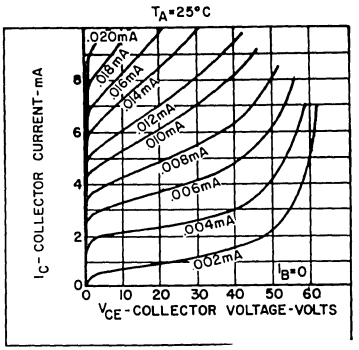


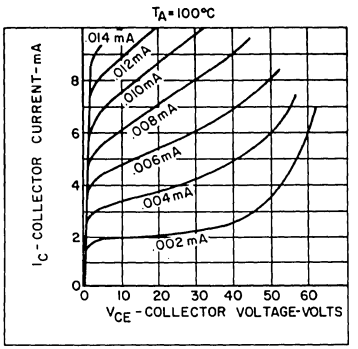
TYPICAL CHARACTERISTICS

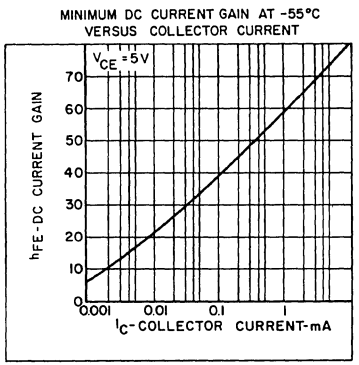
2N2484

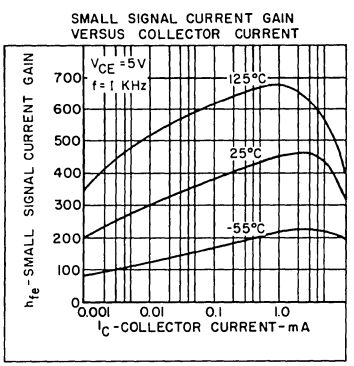
COLLECTOR CHARACTERISTICS

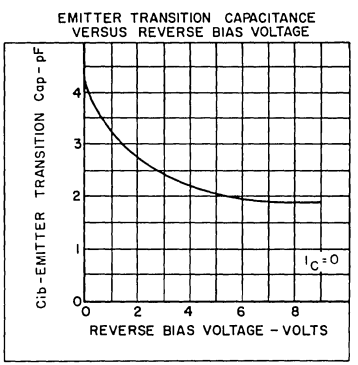


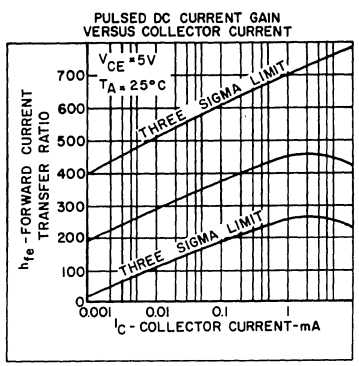


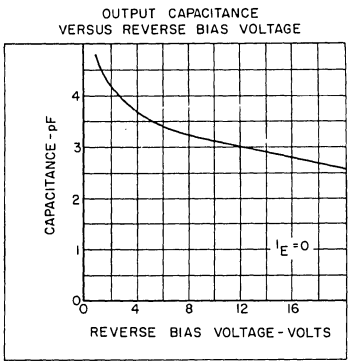


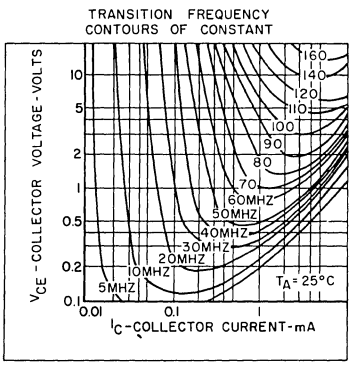








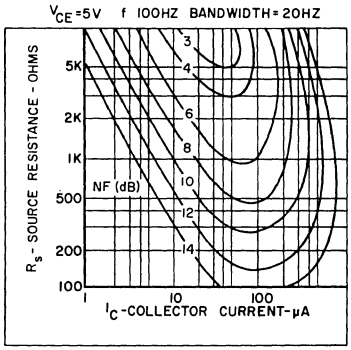


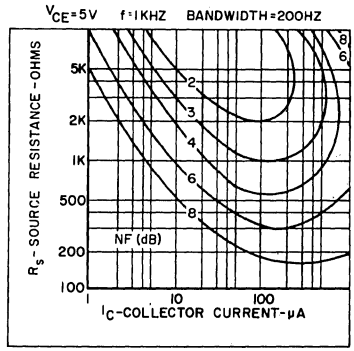


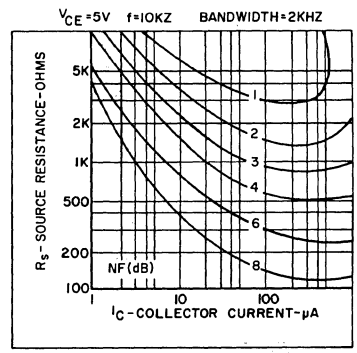
TYPICAL CHARACTERISTICS, continued

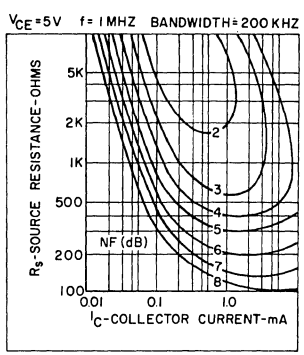
2N2484

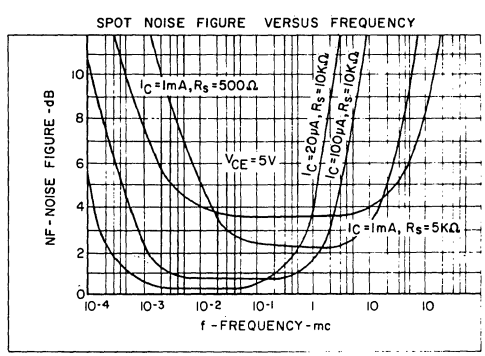
CONTOURS OF CONSTANT NARROW BAND NOISE FIGURE

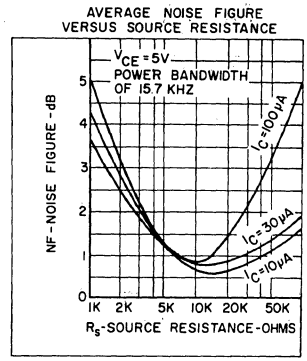




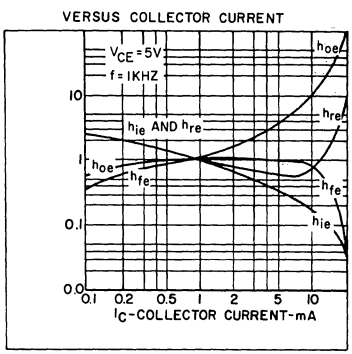


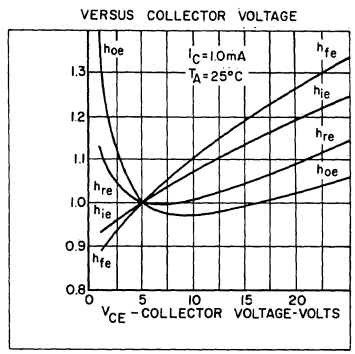


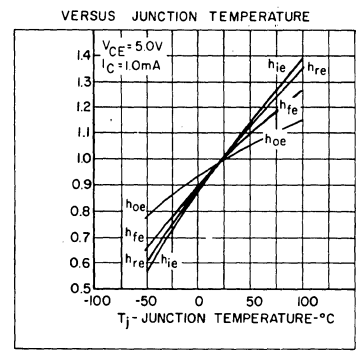




NORMALIZED COMMON EMITTER TRANSFER CHARACTERISTICS







2N2509®
NPN LOW-LEVEL, LOW-NOISE DIFFUSED SILICON PLANAR TRANSISTOR

ABSOLUTE MAXIMUM RATINGS (Note 1)

Characteristics	Unit
Collector-Base Voltage	125 Volts
Collector-Emitter Voltage (Note 4)	80 Volts
Emitter-Base Voltage	7.0 Volts
Total Dissipation @:	
T_C = 25°C (Notes 2 and 3)	1.2 Watts
T_C = 100°C (Notes 2 and 3)	0.68 Watt
T_A = 25°C (Notes 2 and 3)	0.36 Watt
Storage Temperature	−65°C to +300°C
Operating Junction Temperature	+200°C

NOTES:

(1) These ratings are limiting values above which the serviceability of any individual semiconductor device may be impaired.

(2) These are steady state limits. The factory should be consulted on applications involving pulsed or low duty cycle operations.

(3) These ratings give a maximum junction temperature of 200°C and junction to case thermal resistance of 145°C/watt (derating factor of 6.85 mW/°C); junction-to-ambient thermal resistance of 486°C/watt (derating factor of 2.06 mW/°C).

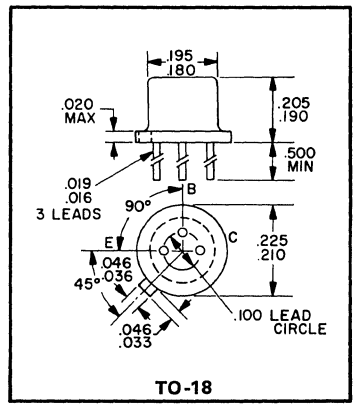
(4) Rating refers to a high-current point where collector-to-emitter voltage is lowest.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Min	Max	Unit	Conditions
h_{FE}	40	–	–	I_C = 10 mA, V_{CE} = 5.0 Volts
h_{FE}	25	–	–	I_C = 10 μA, V_{CE} = 5.0 Volts
$h_{FE(-55°C)}$	20	–	–	I_C = 10 mA, V_{CE} = 5.0 Volts
$V_{CE(sat)}$	–	1.0	Volt	I_C = 5.0 mA, I_B = 0.5 mA
$V_{BE(sat)}$	–	0.9	Volt	I_C = 5.0 mA, I_B = 0.5 mA
h_{fe}	1.5	–	–	I_C = 5.0 mA, V_{CE} = 10 Volts f=30MHz
I_{CBO}	–	5.0	nA	I_E = 0, V_{CB} = 100 Volts
$I_{CBO(150°C)}$	–	10	μA	I_E = 0, V_{CB} = 100 Volts
I_{EBO}	–	2.0	nA	I_C = 0, V_{EB} = 5.0 Volts
C_{ob}	–	6.0	pF	I_E = 0, V_{CB} = 5.0 Volts
C_{ib}	–	10	pF	I_C = 0, V_{EB} = 0.5 Volt
NF	–	7.0	dB	I_C = 10 μA, V_{CE} = 5.0 Volts BW = 200 Hz, R_{GT} = 10 kohms
r_bC_C	–	800	ps	I_C = 10 mA, V_{CB} = 10 Volts
BV_{CBO}	125	–	Volts	I_C = 10 μA, I_E = 0
$V_{CEO(sus)}$	80	–	Volts	I_C = 10 mA, I_B = 0 (Note 4)
BV_{EBO}	7.0	–	Volts	I_E = 0.1 μA, I_C = 0

LOW LEVEL LOW NOISE NPN SILICON PLANAR TRANSISTORS

- **High Gain; 75 min. @ I_C=10μA**
- **Low Noise; 4dB max. @ I_C=10μA**
- **High V_{CEO}; 65 Vdc min.**



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The ITT 2N2510 is an NPN silicon planar transistor designed for application in low noise, low level amplifiers in the audio through high frequency range.

ABSOLUTE MAXIMUM RATINGS

CHARACTERISTICS		UNITS
Collector-to-Base Voltage	100	Volts
Collector-to-Emitter Voltage (open base)	65	Volts
Emitter-to-Base Voltage	7	Volts
Collector Current (continuous)	30	mA
Junction Temperature (operating)	−65 to +175	°C
(storage)	−65 to +200	°C
Total Power Dissipation @ T_C=25°C (derate 6.85 mW/°C above 25°C)	1.2	Watts
Total Power Dissipation @ T_A=25°C (derate 2.06 mW/°C above 25°C)	0.36	Watts

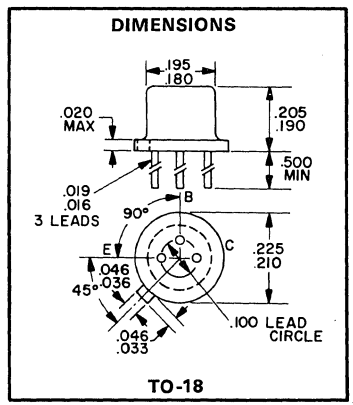
ELECTRICAL CHARACTERISTICS @ 25°C unless otherwise noted

SYMBOL	MIN.	MAX.	UNITS	CONDITIONS
BV_{CBO}	100		Vdc	I_C= 10μA
LV_{CEO}[1,2]	**65**		**Vdc**	**I_C=10mA**
BV_{EBO}	7.0		Vdc	I_E=100nA
h_{FE}	**75**			**I_C=10μA, V_{CE}=5V**
	150	500		I_C=10mA, V_{CE}=5V
	25			I_C=10μA, V_{CE}=5V, T_A=−55°C
	60			I_C=10mA, V_{CE}=5V, T_A=−55°C
V_{CF} (sat)		1.0	Vdc	I_C=5mA, I_B=0.5mA
V_{BE} (sat)		0.9	Vdc	I_C=5mA, I_B=0.5mA
I_{CBO}		5.0	nA	V_{CB}=80V
I_{CBO}		10	μA	V_{CB}=80V, T_A=150°C
I_{EBO}		2.0	nA	V_{EB}=5V
C_{ob}		6.0	pF	V_{CB}=5V, f=1.0 mHz
C_{ib}		10	pF	V_{EB}=0.5V, f=1.0 mHz
h_{fe}	1.5			I_C=5mA, V_{CE}=10V, f=30mHz
		800	psec	I_C=10mA, V_{CB}=10V, f=4mHz
N.F.		**4**	**dB**	**I_C=10μA, V_{CE}=5V, f=1kHz, R=10kΩ Bandwidth=200Hz**

Notes: 1. Pulse width ≤ 300 μsec; duty cycle ≤ 2%.
2. Lowest emitter to collector voltage.

LOW LEVEL LOW NOISE NPN SILICON PLANAR TRANSISTORS

- **High Gain; 80 min @ I_C=1μA**
- **Low Noise; 4 dB max. @ I_C=10μA**
- **High V_{CEO}; 50 Vdc min.**



The ITT 2N2511 is an NPN silicon planar transistor designed for application in low noise, low level amplifiers in the audio through high frequency range.

ABSOLUTE MAXIMUM RATINGS

CHARACTERISTICS		UNITS
Collector-to-Base Voltage	80	Volts
Collector-to-Emitter Voltage (open base)	50	Volts
Emitter-to-Base Voltage	7	Volts
Collector Current (continuous)	30	mA
Junction Temperature (operating)	−65 to +175	°C
(storage)	−65 to +200	°C
Total Power Dissipation @ T_C=25°C (derate 6.85 mW/°C above 25°C)	1.2	Watts
Total Power Dissipation @ T_A=25°C (derate 2.06 mW/°C above 25°C)	0.36	Watts

ELECTRICAL CHARACTERISTICS @ 25°C unless otherwise noted

SYMBOL	MIN.	MAX.	UNITS	CONDITIONS
BV_{CBO}	80		Vdc	$I_C=10\mu A$
LV_{CEO}[1,2]	**50**		**Vdc**	**$I_C=10mA$**
BV_{EBO}	7.0		Vdc	$I_E=100nA$
h_{FE}	**80**			**$I_C=1\mu A$ $V_{CE}=5V$**
	120			$I_C=10\mu A$ $V_{CE}=5V$
	240	750		$I_C=10mA$ $V_{CE}=5V$
	40			$I_C=10\mu A$ $V_{CE}=5V$ $T_A=-55°C$
	100			$I_C=10mA$ $V_{CE}=5V$ $T_A=-55°C$
$V_{CE}(sat)$		1.0	Vdc	$I_C=5mA$ $I_B=0.5mA$
$V_{BE}(sat)$		0.9	Vdc	$I_C=5mA$ $I_B=0.5mA$
I_{CBO}		5.0	nA	$V_{CB}=60V$
I_{CBO}		10	μA	$V_{CB}=60V$ $T_A=150°C$
I_{EBO}		2.0	nA	$V_{EB}=5V$
C_{ob}		6	pF	$V_{CB}=5V$ $f=1mHz$
		10	pF	$V_{EB}=0.5V$ $f=1mHz$
h_{fe}	1.5			$I_C=5mA$ $V_{CE}=10V$ $f=30mHz$
$r_b{}'C_c$		800	psec	$I_C=10mA$ $V_{CB}=10V$ $f=4mHz$
N.F.		**4**	**dB**	**$I_C=10\mu A$ $V_{CE}=5V$ $f=1kHz$ $R_G=10K\Omega$ Bandwidth=200Hz**

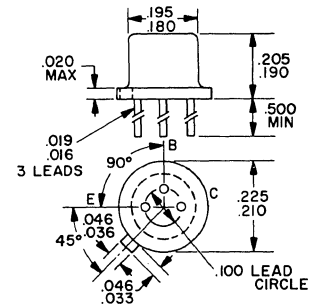
Notes: 1. Pulse width $\leq$ 300 μsec; duty cycle $\leq$ 2%.
2. Lowest emitter to collector voltage.

LOW LEVEL LOW NOISE NPN SILICON PLANAR TRANSISTORS

- **High Gain: 80 min @ $I_C = 1\mu A$**
- **Low Noise; 2dB max. @ $I_C = 1\mu A$**
- **High V_{CEO}; 45 Vdc min.**

The ITT 2N2586 is a NPN silicon planar transistor designed for application in low noise, low level amplifiers in the audio through high frequency range.

DIMENSIONS



TO-18

ABSOLUTE MAXIMUM RATINGS

CHARACTERISTICS		UNITS
Collector-to-Base Voltage	60	Volts
Collector-to-Emitter Voltage (open base)	45	Volts
Emitter-to-Base Voltage	6	Volts
Collector Current (continuous)	30	mA
Junction Temperature (operating)	−65 to +175	°C
(storage)	−65 to +200	°C
Total Power Dissipation @ T_C=25°C (derate 4.0 mW/°C above 25°C)	0.6	Watts
Total Power Dissipation @ T_A=25°C (derate 2.0 mW/°C above 25°C)	0.3	Watts

2H

ELECTRICAL CHARACTERISTICS @ 25°C unless otherwise noted

SYMBOL	MIN.	MAX.	UNITS	CONDITIONS
BV_{CBO}	60		Vdc	$I_C = 10\mu A$
LV_{CEO}[1,2]	**45**		**Vdc**	**$I_C = 10mA$**
BV_{EBO}	6.0		Vdc	$I_E = 10\mu A$
h_{FE}	**80**			**$I_C = 1\mu A$ $V_{CE} = 5V$**
	120	360		$I_C = 10\mu A$ $V_{CE} = 5V$
	150			$I_C = 500\mu A$ $V_{CE} = 5V$
		600		$I_C = 10mA$ $V_{CE} = 5V$
	40			$I_C = 10\mu A$ $V_{CE} = 5V$ $T_A = -55°C$
$V_{CE}(sat)$		0.5	Vdc	$I_C = 10mA$ $I_B = 0.5mA$
$V_{BE}(sat)$	0.7	0.9	Vdc	$I_C = 10mA$ $I_B = 0.5mA$
I_{CBO}		2.0	nA	$V_{CB} = 45V$
I_{CES}		2.0	nA	$V_{CE} = 45V$
I_{CES}		10	μA	$V_{CE} = 45V$ $T_A = 170°C$
I_{CEO}		2.0	nA	$V_{CE} = 5V$
I_{EBO}		2.0	nA	$V_{EB} = 5V$
C_{ob}		7.0	pF	$V_{CB} = 5V$ $f = 1mHz$
h_{fe}	150	600		$I_C = 1mA$ $V_{CE} = 5V$ $f = 1KHz$
	1.5			$I_C = 500\mu A$ $V_{CE} = 5V$ $f = 30mHz$
h_{ie}	4.5	18	kohms	$I_C = 1mA$ $V_{CE} = 5V$ $f = 1KHz$
h_{oe}		100	μmhos	$I_C = 1mA$ $V_{CE} = 5V$ $f = 1KHz$
NF		**2.0**	**dB**	**$I_C = 1\mu A$ $V_{CE} = 5V$ $R_G = 1M\Omega$ $f = 10KHz$**
		2.0	**dB**	**$I_C = 10\mu A$ $V_{CE} = 5V$ $R_G = 10K\Omega$ $f = 10KHz$**
		3.0	**dB**	**$I_C = 10\mu A$ $V_{CE} = 5V$ $R_G = 10K\Omega$ $f = 1KHz$**
		3.5	**dB**	**$I_C = 1\mu A$ $V_{CE} = 5V$ $R_G = 1M\Omega$ $f = 1KHz$**

Notes: 1. Pulse width $\leq 300\ \mu$sec; duty cycle $\leq 2\%$.
2. Lowest emitter to collector voltage.

2N3019, 2N3020Ⓕ

NPN SILICON HIGH VOLTAGE SWITCHING AND AMPLIFIER TRANSISTORS

Package: TO-5

The ITT 2N3019 and 2N3020 are NPN silicon planar epitaxial transistors designed primarily for amplifier and switching applications. These devices feature high breakdown voltages, low leakage currents, low capacity and a beta useful over an extremely wide current range. Switching operation at 1.0 ampere is permissible due to the low saturation voltage.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Characteristics	Unit
Storage Temperature	−65°C to +300°C
Operating Junction Temperature	+200°C
Lead Temperature (Soldering, No Time Limit)	+300°C
Total Device Dissipation	
@ T_C = 25°C (Notes 2 and 3)	5.0 Watts
@ T_A = 25°C (Notes 2 and 3)	0.8 Watt
Collector-Base Voltage	140 Volts
Collector-Emitter Voltage (Note 4)	80 Volts
Emitter-Base Voltage	7.0 Volts

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Min	Max	Unit	Conditions
h_{FE}	90	–	–	(2N3019) I_C = 10 mA, V_{CE} = 10 Volts
	40	120	–	(2N3020) (Note 5)
h_{FE}	100	300	–	(2N3019) I_C = 150 mA, V_{CE} = 10 Volts
	40	120	–	(2N3020) (Note 5)
h_{FE}	50	–	–	(2N3019) I_C = 0.1 mA, V_{CE} = 10 Volts
	30	100	–	(2N3020)
h_{FE}	50	–	–	(2N3019) I_C = 500 mA, V_{CE} = 10 Volts
	30	100	–	(2N3020) (Note 5)
h_{FE}	15	–	–	(2N3019) I_C = 1.0 A, V_{CE} = 10 Volts
	15	–	–	(2N3020) (Note 5)
h_{FE}(−55°C)	40	–	–	(2N3019) I_C = 150 mA, V_{CE} = 10 Volts (Note 5)
$V_{CE(sat)}$	–	0.2	Volt	(2N3019) I_C = 150 mA, I_B = 15 mA
	–	0.2	Volt	(2N3020) (Note 5)
$V_{CE(sat)}$	–	0.5	Volt	(2N3019) I_C = 500 mA, I_B = 15 mA
	–	0.5	Volt	(2N3020) (Note 5)

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Min	Max	Unit	Conditions
$V_{BE(sat)}$	–	1.1	Volts	(2N3019) I_C = 150 mA, I_B = 15 mA
	–	1.1	Volts	(2N3020) (Note 5)
h_{fe}	5.0	–	–	(2N3019) I_C = 50 mA, V_{CE} = 10 Volts
	4.0	–	–	(2N3020)
C_{obo}	–	12	pf	(2N3019) I_E = 0, V_{CB} = 10 Volts
	–	12	pf	(2N3020)
C_{ibo}	–	60	pf	(2N3019) I_C = 0, V_{EB} = 0.5 Volt
	–	60	pf	(2N3020)
I_{CBO}	–	10	nA	(2N3019) I_E = 0, V_{CB} = 90 Volts
	–	10	nA	(2N3020)
$I_{CBO(150°C)}$	–	10	μA	2N3019) I_E = 0, V_{CB} = 90 Volts
	–	10	μA	(2N3020)
I_{EBO}	–	10	nA	(2N3019) I_C = 0, V_{EB} = 5.0 Volts
	–	10	nA	(2N3020)
BV_{CBO}	140	–	Volts	(2N3019) I_C = 100 μA, I_E = 0
	140	–	Volts	(2N3020)
$V_{CEO(sust)}$	80	–	Volts	(2N3019) I_C = 30 mA, I_B = 0
	80	–	Volts	(2N3020) (pulsed) (Notes 4 and 5)
BV_{EBO}	7.0	–	Volts	(2N3019) I_C = 0, I_E = 100 μA
	7.0	–	Volts	(2N3020)
$r_b'C_c$	–	400	psec	(2N3019) I_C = 10 mA, V_{CB} = 10 Volts
	–	400	psec	(2N3020)
NF	–	4	dB	(2N3019) I_C = 100 μA, V_{CE} = 10 Volts (Note 6)

NOTES:

(1) These ratings are limiting values above which the serviceability of any individual semiconductor device may be impaired.

(2) These are steady state limits. The factory should be consulted on applications involving pulsed or low duty cycle operations.

(3) These ratings give a maximum junction temperature of 200°C and junction-to-case thermal resistance of 350°C/Watt (derating factor of 28.6 mW/°C); junction-to-ambient thermal resistance of 218°C/Watt (derating factor of 4.6 mW/°C).

(4) Rating refers to a high-current point where collector-to-emitter voltage is lowest.

(5) Pulse Conditions: length = 300 μsec; duty cycle ≤1%.

(6) f = 1.0 kc; R_S = 1 KΩ.

2N3053

NPN SILICON SWITCHING AND AMPLIFIER TRANSISTOR

Package: TO-5

ABSOLUTE MAXIMUM RATINGS

Characteristics	Unit
Collector-Emitter Voltage	40 Volts
Collector-Base Voltage	60 Volts
Emitter-Base Voltage	5 Volts
Collector Current — Continuous	700 mA
Total Device Dissipation @ T_C = 25°C	5 Watts
Derate above 25°C	28.6 mW/°C
Operating Junction Temperature Range	200 °C
Storage Temperature Range	−65 to +200 °C

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Min	Max	Unit	Conditions
BV_{CEO}	40	–	Volts	I_C = 100 μA, I_E = 0
BV_{CER}	50	–	Volts	I_C = 100 mA, R_{BE} = 10 ohms
BV_{CBO}	60	–	Volts	I_C = 100 μA, I_E = 0
BV_{EBO}	5	–	Volts	I_E = 100 μA, I_C = 0
I_{CEX}	–	0.25	μA	V_{CE} = 60 Volts, $V_{EB(off)}$ = 1.5 Volts
I_{BL}	–	0.25	μA	V_{CE} = 60 Volts, $V_{EB(off)}$ = 1.5 Volts
h_{FE}	25	–	–	I_C = 150 mA, V_{CE} = 2.5 Volts
h_{FE}	50	250	–	I_C = 150 mA, V_{CE} = 10 Volts*
$V_{CE(sat)}$	–	1.4	Volts	I_C = 150 mA, I_B = 15 mA
$V_{BE(sat)}$	–	1.7	Volts	I_C = 150 mA, I_B = 15 mA
$V_{BE(on)}$	–	1.7	Volts	I_C = 150 mA, V_{CE} = 2.5 Volts
f_T	100	–	MHz	I_C = 50 mA, V_{CE} = 10 Volts, f = 20 MHz
C_{ob}	–	15	pF	V_{CB} = 10 Volts, I_E = 0, f = 140 kHz
C_{ib}	–	80	pF	V_{BE} = 0.5 Volt, I_C = 0, f = 100 kHz

* Pulse Test: Pulse Width = 300 μs, Duty Cycle = 2%

Package: TO-5

HIGH VOLTAGE NPN SILICON AMPLIFIER AND SATURATED SWITCHING TRANSISTORS

- **High Voltage** ..... LV_{CEO} = 40 Volts (min) (2N3109/10); 60 Volts (min) (2N3107/8)
- **Low Saturation Voltage** ..... $V_{CE(sat)}$ = 1.0 Volt (max) at 1.0 A
- **Low Noise** ..... NF = 7.0 dB (max) at 1.0 kHz
- **Medium Switching Speed** ..... t_{on} = 200 ns (max at 150 mA
  t_{off} = 600 ns (max) at 150 mA
- **High Gain** ..... h_{FE} = 100 - 300 at 150 mA
  h_{FE} = 40 (min) at 500 mA

ABSOLUTE MAXIMUM RATINGS (Note 1)

Characteristics	Unit
Storage Temperature	−65°C to +200°C
Operating Junction Temperature	200°C Maximum
Lead Temperature (Soldering, 60 second time limit)	300°C Maximum
Total Device Dissipation (Notes 2 and 3) @:	
T_C = 25°C	5.0 Watts
T_A = 25°C	0.8 Watt
Collector-Base Voltage	
(2N3107, 2N3108)	100 Volts
(2N3109, 2N3110)	80 Volts
Collector-Emitter Voltage (Note 4)	
(2N3107, 2N3108)	60 Volts
(2N3109, 2N3110)	40 Volts
Emitter-Base Voltage	
(2N3107, 2N3108)	7.0 Volts
(2N3109, 2N3110)	7.0 Volts

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol		Min	Typ	Max	Unit	Conditions
h_{FE}	2N3107, 2N3109	100	190	300	–	I_C = 150 mA, V_{CE} = 1.0 Volt
	2N3108, 2N3110	40	70	120	–	(Note 5)
h_{FE}	2N3107, 2N3109	40	90	–	–	I_C = 500 mA, V_{CE} = 10 Volts
	2N3108, 2N3110	25	50	–	–	(Note 5)
h_{FE}	2N3107, 2N3109	35	75	–	–	I_C = 0.1 mA, V_{CE} = 10 Volts
	2N3108, 2N3110	20	40	–	–	
$h_{FE(-55°C)}$	2N3107, 2N3109	30	120	–	–	I_C = 150 mA, V_{CE} = 10 Volts
	2N3108, 2N3110	15	26	–	–	(Note 5)
$V_{BE(sat)}$	2N3107, 2N3109	–	0.86	1.1	Volts	I_C = 150 mA, I_B = 15 mA
	2N3108, 2N3110	–	0.86	1.1	Volts	(Note 5)

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol		Min	Typ	Max	Unit	Conditions
$V_{BE(sat)}$	2N3107, 2N3109	–	1.5	2.0	Volts	I_C = 1.0 A, I_B = 100 mA
	2N3108, 2N3110	–	1.5	2.0	Volts	(Notes 5 and 6)
$V_{CE(sat)}$	2N3107, 2N3109	–	0.16	0.25	Volt	I_C = 150 mA, I_B = 15 mA
	2N3108, 2N3110	–	0.16	0.25	Volt	(Note 5)
$V_{CE(sat)}$	2N3107, 2N3109	–	0.76	1.0	Volt	I_C = 1000 mA, I_B = 100 mA
	2N3108, 2N3110	–	0.76	1.0	Volt	(Notes 5 and 6)
h_{fe}	2N3107, 2N3109	3.5	10	–	–	I_C = 50 mA, V_{CE} = 10 Volts
	2N3108, 2N3110	3.0	4.3	–	–	
C_{obo}	2N3107	–	–	20	pF	I_E = 0, V_{CB} = 10 Volts
	2N3108	–	–	20	pF	
C_{obo}	2N3109	–	–	25	pF	I_E = 0, V_{CB} = 10 Volts
	2N3110	–	–	25	pF	
C_{ibo}	2N3107, 2N3109	–	62	80	pF	I_E = 0, V_{EB} = 0.5 Volt
	2N3108, 2N3110	–	62	80	pF	
I_{CES}	2N3107, 2N3109	–	0.4	10	nA	V_{CE} = 60 Volts, V_{EB} = 0
	2N3108, 2N3110	–	0.4	10	nA	
$I_{CBO(150°C)}$	2N3107, 2N3109	–	0.5	10	μA	V_{CB} = 60 Volts, I_E = 0
	2N3108, 2N3110	–	0.5	10	μA	
I_{EBO}	2N3107, 2N3109	–	0.05	10	nA	I_C = 0, V_{EB} = 5.0 Volts
	2N3108, 2N3110	–	0.05	10	nA	
BV_{CBO}	2N3107	100	–	–	Volts	I_E = 0, I_C = 100μA
	2N3108	100	–	–	Volts	
BV_{CBO}	2N3109	80	–	–	Volts	I_E = 0, I_C = 100μA
	2N3110	80	–	–	Volts	
$V_{CEO(sust)}$	2N3107	60	–	–	Volts	I_B = 0, I_C = 30 mA
	2N3108	60	–	–	Volts	(Notes 4 and 5)
$V_{CEO(sust)}$	2N3109	40	–	–	Volts	I_B = 0, I_C = 30 mA
	2N3110	40	–	–	Volts	(Notes 4 and 5)
BV_{EBO}	2N3107, 2N3109	7.0	–	–	Volts	I_C = 0, I_E = 100μA
	2N3108, 2N3110	7.0	–	–	Volts	
NF	2N3107, 2N3109	–	3.5	7.0	dB	I_C = 30μA, V_{CE} = 10 Volts,
	2N3108, 2N3110	–	3.5	7.0	dB	BW = 200 Hz, R_S = 1.0 k ohm

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol		Min	Typ	Max	Unit	Conditions
t_{on}	2N3107, 2N3109	–	120	200	ns	$I_C \approx 150$ mA, $I_{B1} \approx 7.5$ mA,
	2N3108, 2N3110	–	120	200	ns	$I_{B2} \approx -7.5$ mA (Note 7)
t_{off}	2N3107, 2N3109	–	–	1000	ns	$I_C \approx 150$ mA, $I_{B1} \approx 7.5$ mA,
	2N3108, 2N3110	–	350	600	ns	$I_{B2} \approx -7.5$ mA (Note 7)

TYPICAL SMALL SIGNAL CHARACTERISTICS (f = 1 kHz)

Symbol	2N3107 2N3109	2N3108 2N3110	Units	Conditions
h_{ib}	27	27	ohms	I_C = 1.0 mA, V_{CB} = 5.0 Volts
h_{ob}	0.12	0.12	μmhos	I_C = 1.0 mA, V_{CB} = 5.0 Volts
h_{rb}	1.8	0.5	X10^{-4}	I_C = 1.0 mA, V_{CB} = 5.0 Volts
h_{ie}	5000	1800	ohms	I_C = 1.0 mA, V_{CE} = 5.0 Volts
h_{oe}	20	8.0	μmhos	I_C = 1.0 mA, V_{CE} = 5.0 Volts
h_{re}	6.0	2.1	X10^{-4}	I_C = 1.0 mA, V_{CE} = 5.0 Volts
h_{fe}	170	60	–	I_C = 1.0 mA, V_{CE} = 5.0 Volts

NOTES:

(1) These ratings are limiting values above which the serviceability of any individual semiconductor device may be impaired.

(2) These are steady state limits. The factory should be consulted on applications involving pulsed or low-duty cycle operations.

(3) These ratings give a maximum junction temperature of 200°C and junction-to-case thermal resistance of 35°C/Watt (derating factor of 28.6 mW/°C); junction-to-ambient thermal resistance of 218°C/Watt (derating factor of 4.57 mW/°C).

(4) This rating refers to a high-current point where collector to emitter voltage is lowest.

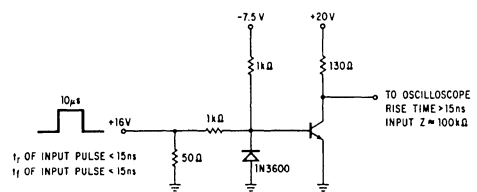
(5) Pulse Conditions: length = 300μs; duty cycle = 1%.

(6) Saturation voltage measured with 1/4" lead length.

(7) See test circuit for exact values of I_C, I_{B1}, and I_{B2}.

SCHEMATIC

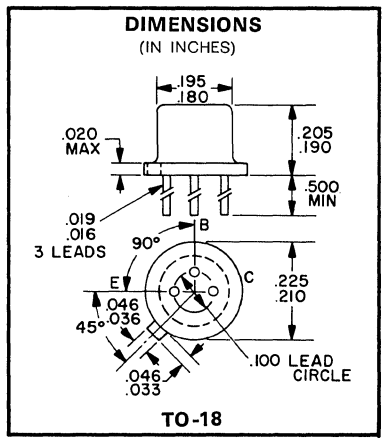
FIGURE 1 – SWITCHING CIRCUIT



LOW LEVEL LOW NOISE NPN SILICON PLANAR TRANSISTORS

- **High Gain; 100 Min. @ I_c=1μA**
- **Low noise; 1dB @ I_c=5μA**
- **High V_{CEO}; 60 Vdc min.**

The ITT 2N3117 is a double-diffused silicon planar transistor designed for application in low level, low noise amplifier from dc to 60 Hz. Low noise and high gain at 1μA permits microwatt operation where power supply drain is a factor.



TO-18

ABSOLUTE MAXIMUM RATINGS

CHARACTERISTICS		UNITS
Collector-to-Base Voltage	60	Volts
Collector-to-Emitter Voltage (open base)	60	Volts
Emitter-to-Base Voltage	6	Volts
Collector Current	50	mA
Junction Temperature (op. and stg.)	−65 to +200	°C
Total Power Dissipation @ T_C=25°C	1.2	Watts
(derate 6.8 mW/°C above 25°C)		
@ T_C=100°C	0.68	Watts
Total Power Dissipation @ T_A=25°C	0.36	Watts
(derate 2.06 mW/°C above 25°C)		

ELECTRICAL CHARACTERISTICS @ 25°C unless otherwise noted.

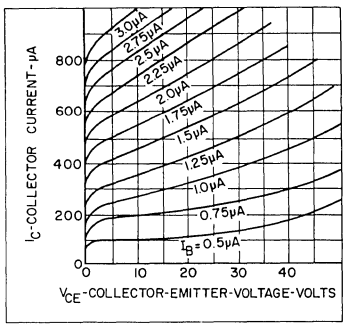
SYMBOL	MIN.	MAX.	UNIT	CONDITION
BV_{CBO}	60		Vdc	$I_C = 10\mu A$
LV_{CEO}[1,2]	**60**		**Vdc**	**$I_C = 10mA$**
BV_{EBO}	6.0		Vdc	$I_C = 10\mu A$
h_{FE}	**100**			**$I_C = 1\mu A$ $V_{CE} = 5V$**
	250	500		$I_C = 10\mu A$ $V_{CE} = 5V$
	300			$I_C = 100\mu A$ $V_{CE} = 5V$
	400			$I_C = 1mA$ $V_{CE} = 5V$
	50			$I_C = 10\mu A$ $V_{CE} = 5V$ $T_A = -55°C$
V_{CE}(sat)		0.35	Vdc	$I_C = 1mA$ $I_B = 0.1mA$
V_{BE}		0.7	Vdc	$I_C = 100\mu A$ $V_{CE} = 5.0V$
I_{CBO}		10	nA	$V_{CB} = 45V$
I_{CBO}		10	μA	$V_{CE} = 45V$ $T_A = 150°C$
I_{EBO}		10	nA	$V_{EB} = 5V$
C_{ob}		4.5	pF	$V_{CB} = 5V$ f = 1mHz
C_{ib}		6.0	pF	$V_{EB} = 0.5V$ f = 1mHz
h_{fe}	2			$I_C = 0.5mA$ $V_{CE} = 5V$ f = 30mHz
	400	900		$I_C = 1mA$ $V_{CE} = 5V$ f = 1KHz
h_{ie}	10	24	kohms	$I_C = 1mA$ $V_{CE} = 5V$ f = 1KHz
h_{oe}		40	μmho	$I_C = 1mA$ $V_{CE} = 5V$
h_{re}		800	$X10^{-6}$	$I_C = 1mA$ $V_{CE} = 5V$
NF		**1.0**	**dB**	**$I_C = 5\mu A$ $V_{CE} = 5V$ $R_S = 50K\Omega$ f = 10KHz Bandwidth = 1.0KHz**
		1.0	**dB**	**$I_C = 5\mu A$ $V_{CE} = 5V$ $R_S = 50K\Omega$ f = 1.0KHz Bandwidth = 200Hz**
		4.0	**dB**	**$I_C = 30\mu A$ $V_{CE} = 5V$ $R_S = 10K\Omega$ f = 100Hz Bandwidth = 20Hz**
		15	**dB**	**$I_C = 30\mu A$ $V_{CE} = 5V$ $R_S = 10K\Omega$ f = 10Hz Bandwidth = 2Hz**

Notes: 1. Pulse width ≤300 μsec; duty cycle ≤2%.
2. Lowest emitter to collector voltage.

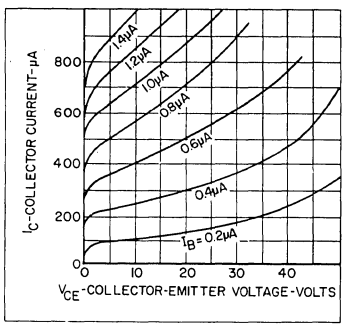
TYPICAL CHARACTERISTICS

COLLECTOR CHARACTERISTICS

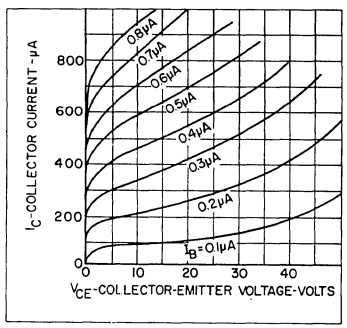
$T_A = -55°C$



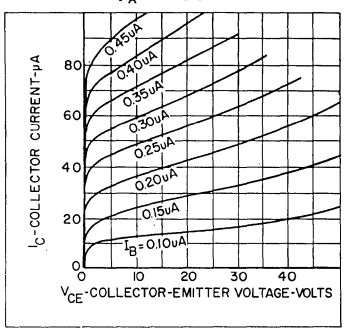
$T_A = 25°C$



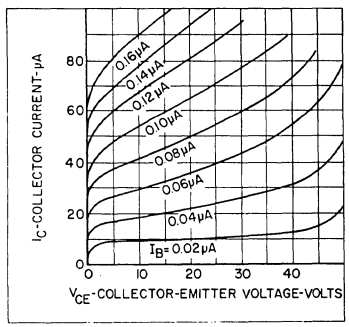
$T_A = 100°C$



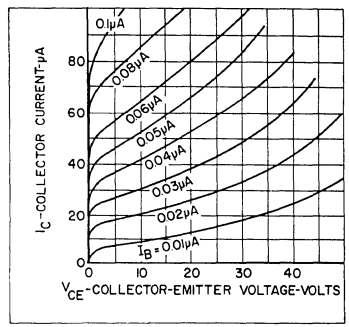
$T_A = -55°C$



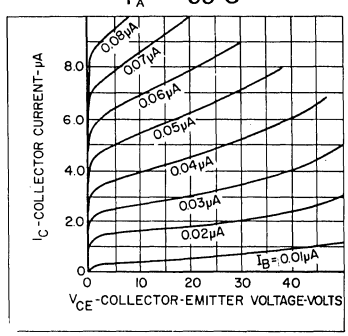
$T_A = 25°C$



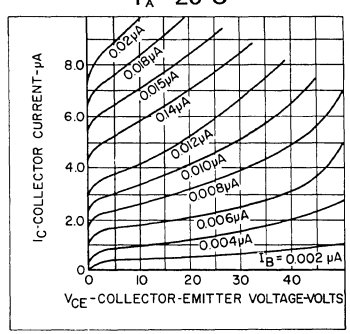
$T_A = 100°C$



$T_A = -55°C$

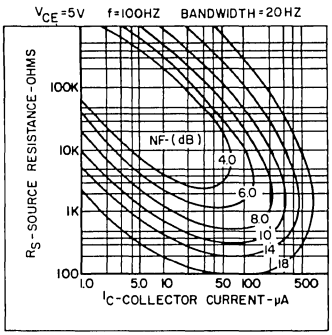


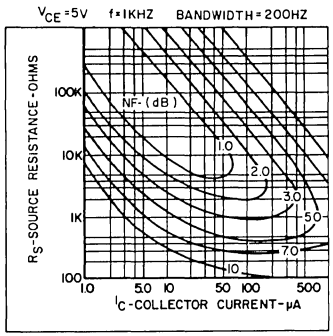
$T_A = 25°C$

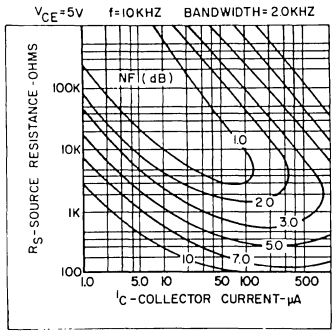


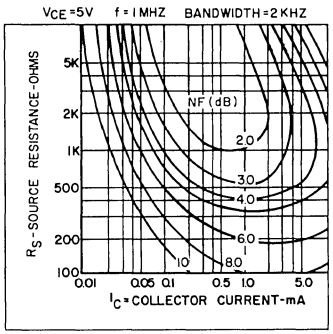
TYPICAL CHARACTERISTICS, continued

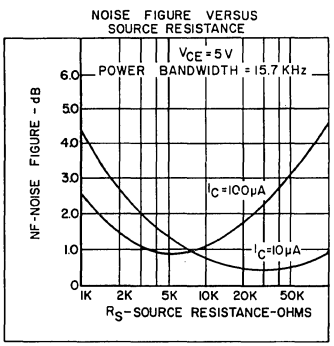
Contours of Constant Narrow Band Noise Figure

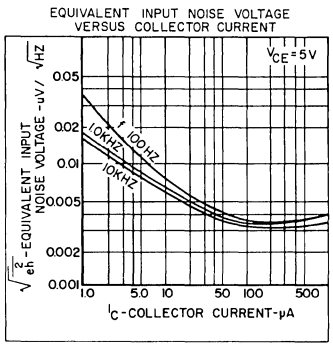


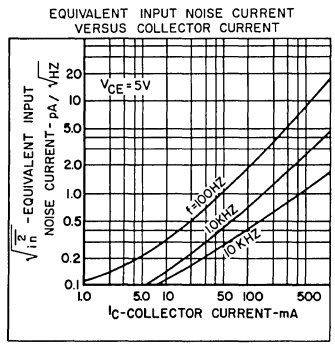






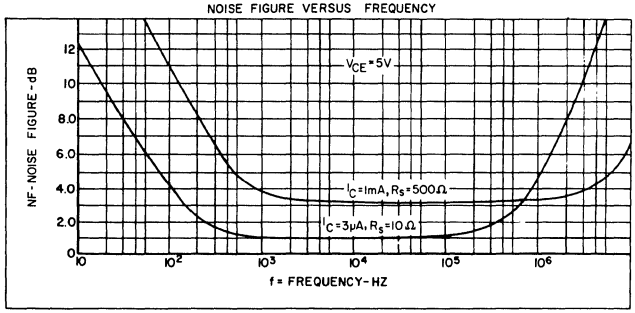




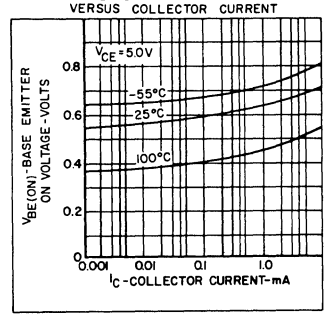


TYPICAL CHARACTERISTICS, continued

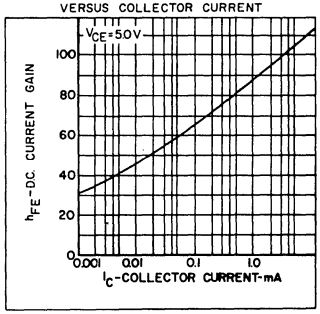
NOISE FIGURE VERSUS FREQUENCY



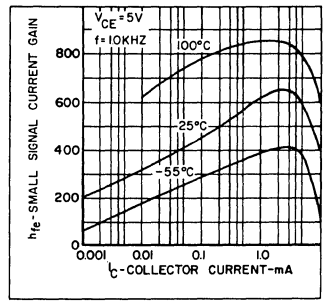
BASE EMITTER ON VOLTAGE VERSUS COLLECTOR CURRENT



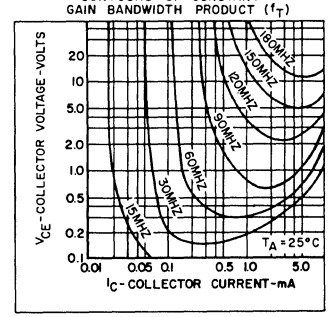
MINIMUM DC CURRENT GAIN AT -55°C VERSUS COLLECTOR CURRENT



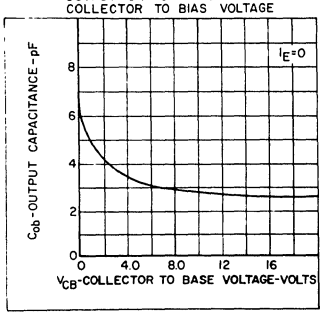
SMALL SIGNAL CURRENT GAIN VERSUS COLLECTOR CURRENT



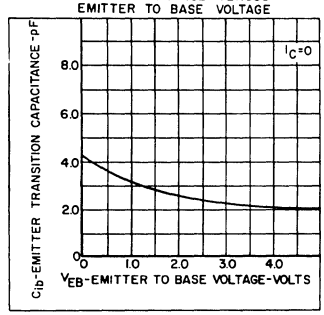
CONTOURS OF CONSTANT GAIN BANDWIDTH PRODUCT (f_T)



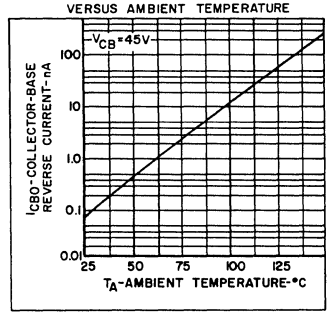
OUTPUT CAPACITANCE VERSUS COLLECTOR TO BIAS VOLTAGE



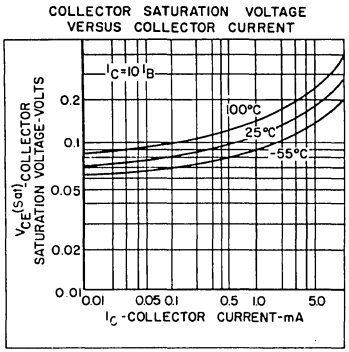
INPUT CAPACITANCE VERSUS EMITTER TO BASE VOLTAGE

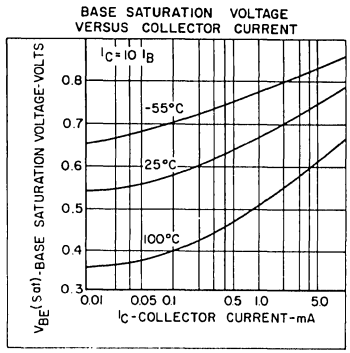


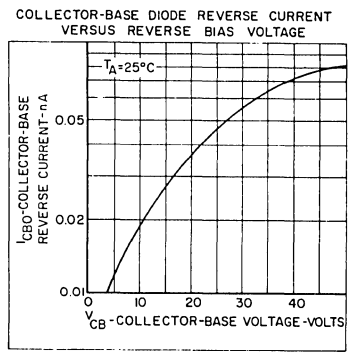
COLLECTOR-BASE REVERSE CURRENT VERSUS AMBIENT TEMPERATURE



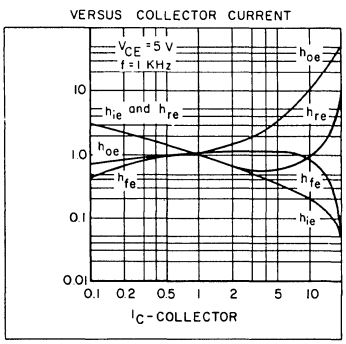
TYPICAL CHARACTERISTICS, continued

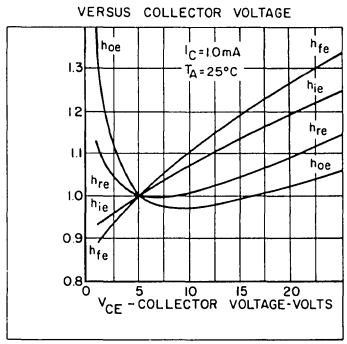


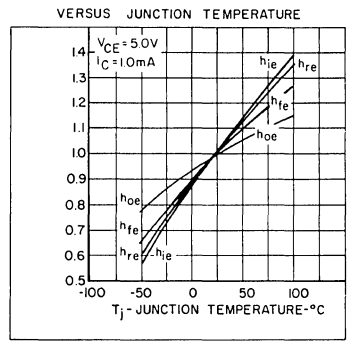




NORMALIZED COMMON EMITTER TRANSFER CHARACTERISTICS







2N3299, 2N3300, 2N3301, 2N3302®
HIGH-SPEED NPN SILICON RF TRANSISTOR AND SWITCHING TRANSISTOR

Packages:
2N3299, 2N3300 TO-18
2N3301, 2N3302 TO-5

The ITT 2N3299 through 2N3302 are NPN silicon planar epitaxial transistors designed to cover a wide range of RF amplifier and high-speed switching applications. These devices feature a minimum LV_{CEO} of 30 volts, a minimum f_T of 250 Mc at I_C = 50 mA, V_{CE} = 10 volts, together with a maximum $V_{CE(sat)}$ of 0.6 volt at 500 mA and h_{FE} specified from 100 μA to 500 mA collector current.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Characteristics	Unit
Collector-Base Voltage	60 Volts
Collector-Emitter Voltage (Note 4)	30 Volts
Emitter-Base Voltage	5.0 Volts
Total Device Dissipation @:	
T_C = 25°C (2N3299 and 2N3300)	3.0 Watts
T_A = 25°C (Notes 2 and 3)	
T_C = 25°C (2N3301 and 2N3302)	1.8 Watts
T_A = 25°C (Notes 2 and 3)	
Storage Temperature	−65°C to +300°C
Operating Junction Temperature	200°C Maximum
Lead Temperature (Soldering, No Time Limit)	300°C Maximum

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol		Min	Typ	Max	Unit	Conditions
h_{FE}	2N3299, 2N3301	40	75	120	–	I_C = 150 mA, V_{CE} = 10 Volts*
	2N3300, 2N3302	100	220	300	–	(Note 5)
h_{FE}	2N3299, 2N3301	20	40	–	–	I_C = 100 μA, V_{CE} = 10 Volts
	2N3300, 2N3302	35	80	–	–	
$V_{CE(sat)}$	2N3299, 2N3301	–	0.4	0.6	Volt	I_C = 500 mA, I_B = 50 mA
	2N3300, 2N3302					
$V_{BE(sat)}$	2N3299, 2N3301	–	1.1	1.5	Volts	I_C = 500 mA, I_B = 50 mA
	2N3300, 2N3302					
$V_{CEO(sust)}$	2N3299, 2N3301	30	–	–	Volts	I_C = 10 mA (pulsed), I_B = 0 (Notes 4 and 5)
	2N3300, 2N3302					
I_{CES}	2N3299, 2N3301	–	0.2	10	nA	V_{CE} = 50 Volts, V_{EB} = 0
	2N3300, 2N3302					
h_{FE}	2N3299, 2N3301	35	70	–	–	I_C = 10 mA, V_{CE} = 10 Volts (Note 5)
	2N3300, 2N3302	75	205	–	–	
h_{FE}	2N3299, 2N3301	25	58	–	–	I_C = 1.0 mA, V_{CE} = 10 Volts
	2N3300, 2N3302	50	140	–	–	
h_{FE}	2N3299, 2N3301	20	62	–	–	I_C = 500 mA, V_{CE} = 10 Volts (Note 5)
	2N3300, 2N3302	50	125	–	–	

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol		Min	Typ	Max	Unit	Conditions
h_{FE}	2N3299, 2N3301	20	50	-	-	I_C = 150 mA, V_{CE} = 1.0 Volt (Note 5)
	2N3300, 2N3302	50	75	-	-	
$V_{CE(sat)}$	2N3299, 2N3301	-	0.14	0.22	Volt	I_C = 150 mA, I_B = 15 mA
	2N3300, 2N3302					
$V_{BE(sat)}$	2N3300, 2N3301	-	0.9	1.1	Volts	I_C = 150 mA, I_B = 15 mA
	2N3300, 2N3302					
$I_{CES(150°C)}$	2N3299, 2N3301	-	0.2	10	μA	V_{CE} = 50 Volts, V_{EB} = 0
	2N3300, 2N3302					
I_{EBO}	2N3299, 2N3301	-	0.1	10	nA	I_C = 0, V_{EB} = 3.0 Volts
	2N3300, 2N3302					
h_{fe}	2N3299, 2N3301	2.5	4.0	-	-	I_C = 50 mA, V_{CE} = 10 Volts
	2N3300, 2N3302					
C_{obo}	2N3299, 2N3301	-	6.0	8.0	pf	I_E = 0, V_{CB} = 10 Volts
	2N3300, 2N3302					
C_{ibo}	2N3299, 2N3301	-	14	20	pf	I_C = 0, V_{EB} = 2.0 Volts
	2N3300, 2N3302					
t_{on}	2N3299, 2N3301	-	14	60	nsec	I_C = 300 mA, I_{B1} = 30 mA (Note 6)
	2N3300, 2N3302					
t_{off}	2N3299, 2N3301	-	80	150	nsec	I_C = 300 mA, I_{B1} = 30 mA (Note 6)
	2N3300, 2N3302					
BV_{CBO}	2N3299, 2N3301	60	-	-	Volts	I_C = 10 μA, I_E = 0
	2N3300, 2N3302					
BV_{EBO}	2N3299, 2N3301	5.0	-	-	Volts	I_E = 10 μA, I_C = 0
	2N3300, 2N3302					

NOTES:

(1) These ratings are limiting values above which the serviceability of any individual semiconductor device may be impaired.

(2) These are steady state limits. The factory should be consulted on applications involving pulsed or low duty cycle operations.

(3) These ratings give a maximum junction temperature of 200°C and junction-to-case thermal resistance for the 2N3299 and 2N300 of 58.3°C/watt (derating factor of 17.2 mW/°C); for the 2N3301 and 2N3302 97.3°C/watt (derating factor of 10.3 mW/°C). Junction-to-ambient thermal resistance for the 2N3299 and 2N3300 of 219°C/watt (derating factor of 4.56 mW/°C); for the 2N3301 and 2N3302 486°C/watt (derating factor of 2.06 mW/°C).

(4) This rating refers to a high-current point where collector-to-emitter voltage is lowest.

(5) Pulse Conditions: length = 300 μsec; duty cycle ≤ 2%.

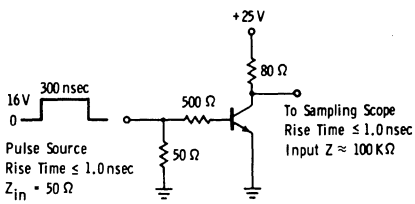
(6) See switching circuit for exact values of I_C, I_{B1}, and I_{B2}.

TYPICAL SMALL SIGNAL CHARACTERISTICS (f = 1 kc)

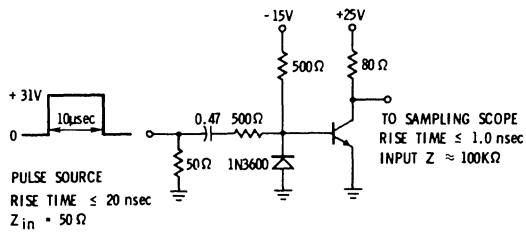
Symbol	V_{CE} = 1.0V, I_C = 10 mA	V_{CE} = 10V, I_C = 10 mA	V_{CE} = 1.0V, I_C = 50 mA	V_{CE} = 10V, I_C = 50 mA	Units
			2N3299 • 2N3301		
h_{ie}	380	460	170	350	Ohms
h_{oe}	410	55	950	405	μmhos
h_{re}	2250	130	2650	500	X 10^{-4}
h_{fe}	72	90	48	97	–
			2N3300 • 2N3302		
h_{ie}	780	950	190	880	Ohms
h_{oe}	440	83	1300	660	μmhos
h_{re}	1900	205	5400	1500	X 10^{-6}
h_{fe}	140	170	53	220	–

SCHEMATIC

t_{on} TEST CIRCUIT



t_{off} TEST CIRCUIT



Package: TO-52

HIGH-SPEED NPN SILICON SATURATED SWITCHING TRANSISTOR

ABSOLUTE MAXIMUM RATINGS

Characteristics	Unit
Collector-Base Voltage	40 Volts
Collector-Emitter Voltage	10 Volts
Emitter-Base Voltage	6 Volts
Collector Current	500 mA
Total Device Dissipation @ T_A = 25°C	360 mW
Derate above 25°C	2.06 mW/°C
Total Device Dissipation @ T_C = 25°C	1.2 Watts
Derate above 25°C	6.9 mW/°C
Junction Temperature, Operating	+200 °C
Storage Temperature Range	−65 to +200 °C

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Min	Max	Unit	Conditions
I_{CEX}	–	0.025	μA	V_{CE} = 10 Volts, $V_{EB(off)}$ = 1 Volt
I_{CEX}	–	50	μA	V_{CE} = 10 Volts, $V_{EB(off)}$ = 1 Volt, T_A = 150°C
I_{BL}	–	0.025	μA	V_{CE} = 10 Volts, V_{OB} = 1 Volt
BV_{CBO}	40	–	Volts	I_C = 10 μA, I_E = 0
BV_{CEO}*	10	–	Volts	I_C = 10 mA, I_B = 0*
BV_{EBO}	6	–	Volts	I_E = 10 μA, I_C = 0
$V_{CE(sat)}$*	–	0.25	Volt	I_C = 10 mA, I_B = 1 mA*
$V_{CE(sat)}$*	–	0.4	Volt	I_C = 150 mA, I_B = 15 mA
$V_{CE(sat)}$*	–	0.6	Volt	I_C = 300 mA, I_B = 30 mA
$V_{BE(sat)}$*	–	0.8	Volt	I_C = 10 mA, I_B = 1 mA
$V_{BE(sat)}$*	0.8	1.0	Volt	I_C = 150 mA, I_B = 15 mA
$V_{BE(sat)}$*	–	1.15	Volts	I_C = 300 mA, I_B = 30 mA
h_{FE}*	12	–	–	I_C = 1.0 mA, V_{CE} = 1 Volt
h_{FE}*	20	–	–	I_C = 10 mA, V_{CE} = 1 Volt
h_{FE}*	25	150	–	I_C = 150 mA, V_{CE} = 1 Volt
h_{FE}*	15	–	–	I_C = 300 mA, V_{CE} = 1 Volt

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Min	Max	Unit	Conditions
C_{ob}	–	4	pF	V_{CB} = 10 Volts, I_E = 0, f = 100 kHz
C_{ib}	–	8	pF	V_{BE} = 0.5 Volt, I_C = 0, f = 100 kHz
h_{fe}	3.5	–	–	I_C = 15 mA, V_{CE} = 10 Volts, f = 100 MHz
t_d	–	10	ns	I_C = 150 mA, I_{B1} = 15 mA, V_{EB} = 0.5 Volt, V_{CC} = 6 Volts
t_r	–	12	ns	
t_{on}	–	20	ns	
t_s	–	16	ns	I_C = 150 mA, $I_{B1} = -I_{B2}$ = 15 mA, V_{CC} = 6 Volts
t_f	–	12	ns	
t_{off}	–	25	ns	
Q_T	–	300	pC	I_C = 150 mA, I_B = 15 mA, V_{CC} = 6 Volts
h_{fe}	20	150	–	I_C = 1 mA, V_{CE} = 10 Volts, f = 1 kHz
h_{re}	–	25	$X10^{-4}$	I_C = 1 mA, V_{CE} = 10 Volts, f = 1 kHz
h_{ie}	0.6	4.5	kohms	I_C = 1 mA, V_{CE} = 10 Volts, f = 1 kHz
h_{oe}	10	100	μmhos	I_C = 1 mA, V_{CE} = 10 Volts, f = 1 kHz

* Pulse Test: PW $\leq$ 300μs, Duty Cycle $\leq$ 2%

Package: TO-5

NPN SILICON GENERAL PURPOSE AMPLIFIER AND SWITCHING TRANSISTORS

The ITT 2N3665 and 2N3666 are NPN diffused silicon planar epitaxial transistors designed primarily for general purpose amplifier and switching applications. They feature high voltage, low output capacity and a useful beta over a wide current range.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Characteristics	Unit
Collector-Base Voltage	120 Volts
Collector-Emitter Voltage (Note 4)	80 Volts
Emitter-Base Voltage	10 Volts
Collector Current	1.0 Amp
Total Device Dissipation @ T_C = 25°C	5.0 Watts
Storage Temperature	−65°C to +200°C
Operating Junction Temperature	200°C Maximum
Lead Temperature (Soldering, 10 sec Time Limit)	300°C Maximum

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Min	Max	Unit	Conditions
h_{FE}	40	120	–	(2N3665) I_C = 150 mA, V_{CE} = 10 Volts (Note 5)
	100	300	–	(2N3666)
h_{FE}	30	–	–	(2N3665) I_C = 10 mA, V_{CE} = 10 Volts (Note 5)
	70	–	–	(2N3666)
h_{FE}	25	–	–	(2N3665) I_C = 500 mA, V_{CE} = 10 Volts (Note 5)
	50	–	–	(2N3666)
$h_{FE(-55°C)}$	16	–	–	(2N3665) I_C = 150 mA, V_{CE} = 10 Volts (Note 5)
	40	–	–	(2N3666)
$V_{BE(sat)}$	–	1.8	Volts	(2N3665) I_C = 500 mA, I_B = 50 mA (Note 5)
	–	1.8	Volts	(2N3666)
$V_{BE(sat)}$	–	1.2	Volts	(2N3665) I_C = 150 mA, I_B = 15 mA (Note 5)
	–	1.2	Volts	(2N3666)
$V_{CE(sat)}$	–	1.2	Volts	(2N3665) I_C = 500 mA, I_B = 50 mA (Note 5)
	–	1.2	Volts	(2N3666)
$V_{CE(sat)}$	–	0.5	Volt	(2N3665) I_C = 150 mA, I_B = 15 mA (Note 5)
	–	0.5	Volt	(2N3666)
h_{fe}	3.0	–	–	(2N3665) I_C = 50 mA, V_{CE} = 10 Volts
	3.0	–	–	(2N3666)

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Min	Max	Unit	Conditions
C_{obo}	–	12	pf	(2N3665) $I_E = 0, V_{CB} = 10$ Volts
	–	12	pf	(2N3666)
C_{ibo}	–	60	pf	(2N3665) $I_C = 0, V_{EB} = 0.5$ Volt
	–	60	pf	(2N3666)
I_{CEX}	–	50	nA	$V_{CE} = 80$ Volts, $V_{EB} = 0.5$ Volt
I_{CBO}	–	50	nA	$V_{CB} = 60$ Volts, $I_E = 0$
$I_{CBO(150°C)}$	–	50	μA	$V_{CB} = 60$ Volts, $I_E = 0$
I_{BEX}	–	50	nA	$V_{CE} = 80$ Volts, $V_{EB} = 0.5$ Volt
I_{EBO}	–	50	nA	$I_C = 0, V_{EB} = 5.0$ Volts
BV_{CBO}	120	–	Volts	$I_C = 100\mu A, I_E = 0$
$V_{CEO(sust)}$	80	–	Volts	$I_C = 10$ mA, $I_B = 0$ (Notes 4 and 5)
BV_{EBO}	10	–	Volts	$I_C = 0, I_E = 100$ uA
BV_{CER}	90	–	Volts	$I_C = 10$ mA, $R_{BE} = 10$ ohms (Notes 4 and 5)
$t_{on} + t_{off}$	–	4.0	μsec	(2N3665) (See Figure 1)
	–	5.0	μsec	(2N3666)

NOTES:

(1) These ratings are limiting values above which the serviceability of any individual semiconductor device may be impaired.

(2) These are steady state limits. The factory should be consulted on applications involving pulsed or low duty cycle operations.

(3) These ratings give a maximum junction temperature of 200°C and junction-to-case thermal resistance of 35°C/watt (derating factor of 28.6 mW/°C).

(4) Rating refers to a high-current point where collector-to-emitter voltage is lowest.

(5) Pulse Conditions: length = 300 μsec; duty cycle = 1%.

SCHEMATIC

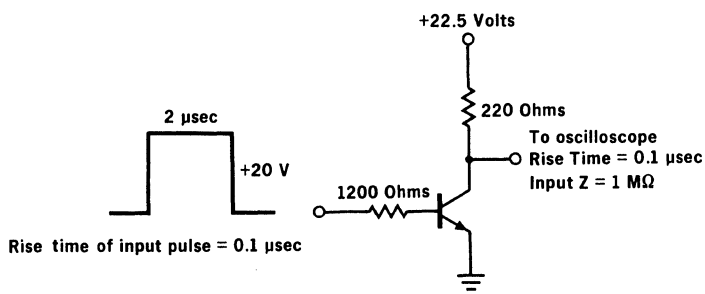


FIGURE 1 – SWITCHING CIRCUIT

Package: TO-18

NPN SILICON HIGH FREQUENCY IF-RF AMPLIFIER TRANSISTORS

The ITT 2N3700 and 2N3701 are NPN diffused silicon planar epitaxial transistors designed primarily for high frequency applications in IF-RF amplifier circuits. The planar structure provides low saturation voltage at high collector currents and low leakage current over a wide range of temperature and bias conditions. Useful frequency range: DC to 100 MHz.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Characteristics	Unit
Storage Temperature	−65°C to +200°C
Operating Junction Temperature	200°C Maximum
Lead Temperature (Soldering, 60 sec. time limit)	300°C Maximum
Total Device Dissipation	
@ T_C = 25°C (Notes 2 and 3)	1.8 Watts
@ T_C = 100°C (Notes 2 and 3)	1.0 Watt
@ T_A = 25°C (Notes 2 and 3)	0.5 Watt
Collector-Base Voltage	140 Volts
Collector-Emitter Voltage (Note 4)	80 Volts
Emitter-Base Voltage	7.0 Volts
Collector Current	1.0 Amp.

NOTES:

(1) These ratings are limiting values above which the serviceability of any individual semiconductor device may be impaired.

(2) These are steady state limits. The factory should be consulted on applications involving pulsed or low duty cycle operations.

(3) These ratings give a maximum junction temperature of 200°C and junction-to-case thermal resistance of 97°C/watt (derating factor of 10.3 mW/°C); junction-to-ambient thermal resistance of 350°C/watt (derating factor of 2.85 mW/°C).

(4) Rating refers to a high-current point where collector-to-emitter voltage is lowest.

(5) Pulse Conditions: length = 300 μsec; duty cycle ≤ 1%.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Min	Max	Unit	Conditions
h_{FE}	100	300	–	(2N3700) I_C = 150 mA, V_{CE} = 10 Volts
	40	120	–	(2N3701) (Note 5)
h_{FE}	90	–	–	(2N3700) I_C = 10 mA, V_{CE} = 10 Volts
	40	120	–	(2N3701) (Note 5)
h_{FE}	50	–	–	(2N3700) I_C = 0.1 mA, V_{CE} = 10 Volts
	30	100	–	(2N3701) (Note 5)
h_{FE}	50	–	–	(2N3700) I_C = 500 mA, V_{CE} = 10 Volts
	30	100	–	(2N3701) (Note 5)
h_{FE}	15	–	–	(2N3700) I_C = 1.0 A, V_{CE} = 10 Volts
	15	–	–	(2N3701) (Note 5)
h_{FE}(−55°C)	40	–	–	(2N3700) I_C = 150 mA, V_{CE} = 10 Volts
	–	–	–	(2N3701) (Note 5)
$V_{BE(sat)}$	–	1.1	Volts	(2N3700) I_C = 150 mA, I_B = 15 mA
	–	1.1	Volts	(2N3701)

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Min	Max	Unit		Conditions
$V_{CE(sat)}$	–	0.2	Volt	(2N3700)	I_C = 150 mA, I_B = 15 mA
	–	0.2	Volt	(2N3701)	(Note 5)
$V_{CE(sat)}$	–	0.5	Volt	(2N3700)	I_C = 500 mA, I_B = 50 mA
	–	0.5	Volt	(2N3701)	(Note 5)
h_{fe}	5.0	10	–	(2N3700)	I_C = 50 mA, V_{CE} = 10 Volts
	4.0	10	–	(2N3701)	
h_{fe}	80	400	–	(2N3700)	I_C = 1.0 mA, V_{CE} = 5.0 Volts
	30	200	–	(2N3701)	
C_{obo}	–	12	pf	(2N3700)	I_E = 0, V_{CB} = 10 Volts
	–	12	pf	(2N3701)	
C_{ibo}	–	60	pf	(2N3700)	I_C = 0, V_{EB} = 0.5 Volt
	–	60	pf	(2N3701)	
$r_b'C_c$	25	400	psec	(2N3700)	I_C = 10 mA, V_{CB} = 10 Volts
	25	400	psec	(2N3701)	
I_{CBO}	–	10	nA	(2N3700)	I_E = 0, V_{CB} = 90 Volts
	–	10	nA	(2N3701)	
$I_{CBO(150°C)}$	–	10	μA	(2N3700)	I_E = 0, V_{CB} = 90 Volts
	–	10	μA	(2N3701)	
I_{EBO}	–	10	nA	(2N3700)	I_C = 0, V_{EB} = 5.0 Volts
	–	10	nA	(2N3701)	
BV_{CBO}	140	–	Volts	(2N3700)	I_C = 100μA, I_E = 0
	140	–	Volts	(2N3701)	
$V_{CEO(sust)}$	80	–	Volts	(2N3700)	I_C = 30 mA, I_B = 0 (Notes 4 and 5)
	80	–	Volts	(2N3701)	
BV_{EBO}	7.0	–	Volts	(2N3700)	I_C = 0, I_E = 100μA
	7.0	–	Volts	(2N3701)	
NF	–	4.0	dB	(2N3700)	I_C = 100μA, V_{CE} = 10 Volts, f = 1 KHz, R_G = 1 KΩ

2N5209, 2N5210

LOW-LEVEL, LOW-NOISE NPN SILICON AMPLIFIER TRANSISTORS

ABSOLUTE MAXIMUM RATINGS

Characteristic	Unit
Collector-Emitter Voltage	50 Vdc
Collector-Base Voltage	50 Vdc
Emitter-Base Voltage	4.5 Vdc
Collector Current - Continuous	50 mAdc
Peak	100 mAdc

Total Device Dissipation @ T_A = 25°C	310 mW
Derate above 25°C	2.81 mW/°C
Thermal Resistance, Junction to Ambient	0.357 °C/mW

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Min	Typ	Max	Unit	Conditions
BV_{CEO}	50	–	–	Vdc	I_C = 1.0 mAdc, I_B = 0
BV_{CBO}	50	–	–	Vdc	I_C = 0.1 mAdc, I_E = 0
I_{CBO}	–	–	10	nAdc	V_{CB} = 10 Vdc, I_E = 0
	–	–	50		V_{CB} = 35 Vdc, I_E = 0
I_{EBO}	–	–	50	nAdc	V_{BE} = 3.0 Vdc, I_C = 0
	–	–	100		V_{BE} = 4.5 Vdc, I_C = 0
h_{FE}	100	–	300	–	I_C = 100 *u*Adc, V_{CE} = 5.0 Vdc 2N5209
	200	–	600		2N5210
	150	–	–		I_C = 1.0 mAdc, V_{CE} = 5.0 Vdc 2N5209
	250	–	–		2N5210
	150	–	–		I_C = 10 mAdc, V_{CE} = 5.0 Vdc 2N5209
	250	–	–		2N5210
$V_{CE(sat)}$	–	–	0.7	Vdc	I_C = 10 mAdc, I_B = 1.0 mAdc
$V_{BE(on)}$	–	–	0.85	Vdc	I_C = 1.0 mAdc, V_{CE} = 5.0 Vdc
f_T	30	80	–	MHz	I_C = 500 *u*Adc, V_{CE} = 5.0 Vdc, f = 20 MHz
C_{cb}	–	–	4.0	pF	V_{CB} = 5.0 Vdc, I_E = 0, f = 100 kHz emitter guarded
h_{fe}	150	–	600	–	I_C = 1.0 mAdc, V_{CE} = 5.0 Vdc, f = 1.0 kHz 2N5209
	250	–	900		2N5210
NF	–	–	3.0	dB	I_C = 20 *u*Adc, V_{CE} = 5.0 Vdc, R_S = 22 k ohms, f = 10 Hz to 15.7 kHz 2N5209
	–	–	2.0		2N5210
	–	1.6	4.0		I_C = 20 *u*Adc, V_{CE} = 5.0 Vdc, R_S = 10 k ohms, f = 1.0 kHz 2N5209
	–	1.4	3.0		2N5210

2N5219

Package: To-92

GENERAL PURPOSE NPN SILICON TRANSISTOR

ABSOLUTE MAXIMUM RATINGS

Characteristic	Unit
Collector-Emitter Voltage	15 Vdc
Collector-Base Voltage	20 Vdc
Emitter-Base Voltage	3.0 Vdc
Collector Current - Continuous	100 mAdc
Total Device Dissipation @ T_A = 25°C	310 mW
Derate above 25°C	2.81 mW/°C
Operating and Storage Junction Temperature Range	-55 to +135 °C
Thermal Resistance, Junction to Ambient	0.357 °C/mW

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Min	Max	Unit	Conditions
BV_{CEO}	15	–	Vdc	I_C = 1.0 mAdc, I_B = 0
BV_{CBO}	20	–	Vdc	I_C = 100 uAdc, I_E = 0
BV_{EBO}	3.0	–	Vdc	I_E = 100 uAdc, I_C = 0
I_{CBO}	–	100	nAdc	V_{CB} = 10 Vdc, I_E = 0
I_{EBO}	–	500	nAdc	V_{BE} = 2.0 Vdc, I_C = 0
h_{FE}	35	500	–	I_C = 2.0 mAdc, V_{CE} = 10 Vdc
$V_{CE(sat)}$	–	0.4	Vdc	I_C = 10 mAdc, I_B = 1.0 mAdc
$V_{BE(sat)}$	–	1.0	Vdc	I_C = 10 mAdc, I_B = 1.0 mAdc
f_T	150	–	MHz	I_C = 10 mAdc, V_{CE} = 10 Vdc
C_{cb}	–	4.0	pF	V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz
h_{fe}	35	1500	–	I_C = 2.0 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz

LOW-POWER GENERAL PURPOSE NPN SILICON AMPLIFIER TRANSISTOR

ABSOLUTE MAXIMUM RATINGS

Characteristics	Unit
Collector-Emitter Voltage	15 Vdc
Collector-Base Voltage	15 Vdc
Emitter-Base Voltage	3.0 Vdc
Collector Current - Continuous	500 mAdc
Total Device Dissipation @ T_A = 25°C	310 mW
Derate above 25°C	2.81 mW/°C
Operating and Storage Junction Temperature Range	-55 to +135 °C
Thermal Resistance, Junction to Ambient	0.357 °C/mW

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Min	Max	Unit	Conditions
BV_{CEO}	15	–	Vdc	I_C = 10 mAdc, I_B = 0
BV_{CBO}	15	–	Vdc	I_C = 100 uAdc, I_E = 0
BV_{EBO}	3.0	–	Vdc	I_E = 100 uAdc, I_C = 0
I_{CBO}	–	100	nAdc	V_{CB} = 10 Vdc, I_E = 0
I_{EBO}	–	100	nAdc	V_{BE} = 3.0 Vdc, I_C = 0
h_{FE}	25	–	–	I_C = 10 mAdc, V_{CE} = 10 Vdc
	30	600		I_C = 50 mAdc, V_{CE} = 10 Vdc
$V_{CE(sat)}$	–	0.5	Vdc	I_C = 150 mAdc, I_B = 15 mAdc
$V_{BE(sat)}$	–	1.1	Vdc	I_C = 150 mAdc, I_B = 15 mAdc
f_T	100	–	MHz	I_C = 20 mAdc, V_{CE} = 10 Vdc
C_{cb}	–	10	pF	V_{CB} = 5.0 Vdc, I_E = 0, f = 1.0 MHz
h_{fe}	30	1800	–	I_C = 50 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz

2N5223

Package: To-92

LOW-LEVEL GENERAL PURPOSE NPN SILICON AMPLIFIER TRANSISTOR

ABSOLUTE MAXIMUM RATINGS

Characteristic	Unit
Collector-Emitter Voltage	20 Vdc
Collector-Base Voltage	25 Vdc
Emitter-Base Voltage	3.0 Vdc
Collector Current	100 mAdc
Total Device Dissipation @ T_A = 25°C	310 mW
Derate above 25°C	2.81 mW/°C
Operating and Storage Junction Temperature Range	-55 to +135 °C
Thermal Resistance, Junction to Ambient	0.357 °C/mW

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Min	Max	Unit	Conditions
BV_{CEO}	20	–	Vdc	I_C = 1.0 mAdc, I_B = 0
BV_{CBO}	25	–	Vdc	I_C = 100 uAdc, I_E = 0
BV_{EBO}	3.0	–	Vdc	I_E = 100 uAdc, I_C = 0
I_{CBO}	–	100	nAdc	V_{CB} = 10 Vdc, I_E = 0
I_{EBO}	–	500	nAdc	V_{BE} = 3.0 Vdc, I_C = 0
h_{FE}	50	800	–	I_C = 2.0 mAdc, V_{CE} = 10 Vdc
$V_{CE(sat)}$	–	0.7	Vdc	I_C = 10 mAdc, I_B = 1.0 mAdc
$V_{BE(sat)}$	–	1.2	Vdc	I_C = 10 mAdc, I_B = 1.0 mAdc
f_T	150	–	MHz	I_C = 10 mAdc, V_{CE} = 10 Vdc
C_{cb}	–	4.0	pF	V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz
h_{fe}	50	1600	–	I_C = 2.0 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz

Package: To-92

MEDIUM POWER NPN SILICON AMPLIFIER TRANSISTOR

ABSOLUTE MAXIMUM RATINGS

Characteristic	Unit
Collector-Emitter Voltage	25 Vdc
Collector-Base Voltage	25 Vdc
Emitter-Base Voltage	4.0 Vdc
Collector Current	500 mAdc
Total Device Dissipation @ T_A = 25°C	310 mW
Derate above 25°C	2.81 mW/°C
Operating and Storage Junction Temperature Range	-55 to +135 °C
Thermal Resistance, Junction to Ambient	0.357 °C/mW

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Min	Max	Unit	Conditions
BV_{CEO}	25	–	Vdc	I_C = 10 mAdc, I_B = 0
BV_{CBO}	25	–	Vdc	I_C = 100 uAdc, I_E = 0
BV_{EBO}	4.0	–	Vdc	I_E = 100 uAdc, I_C = 0
I_{CBO}	–	300	nAdc	V_{CB} = 15 Vdc, I_E = 0
I_{EBO}	–	500	nAdc	V_{BE} = 4.0 Vdc, I_C = 0
h_{FE}	25	–	–	I_C = 10 mAdc, V_{CE} = 10 Vdc
	30	600		I_C = 50 mAdc, V_{CE} = 10 Vdc
$V_{CE(sat)}$	–	0.8	Vdc	I_C = 100 mAdc, I_B = 10 mAdc
$V_{BE(sat)}$	–	1.0	Vdc	I_C = 100 mAdc, I_B = 10 mAdc
f_T	50	–	MHz	I_C = 20 mAdc, V_{CE} = 10 Vdc
C_{cb}	–	20	pF	V_{CB} = 5.0 Vdc, I_E = 0, f = 1.0 MHz
h_{fe}	30	1800	–	I_C = 50 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz

2N5368 thru 2N5371
GENERAL PURPOSE NPN SILICON TRANSISTORS

Package : TO-92

ABSOLUTE MAXIMUM RATINGS @ 25°C (free air)

Characteristics	Unit
Storage temperature range	-55 to +150 °C
Operating Collector Junction Temperature	+150 °C
Lead temperature 1/16" from case 10 seconds max.	+260 °C
Collector current	500 mA
Continuous device dissipation at or below 25°C free-air temperature	360 mW
Linear derating factor above 25°C	2.87 mW/°C
Emitter-base voltage	5 V
Collector-base voltage	60 V
Collector-base voltage (2N5371)	40 V
Collector-emitter voltage (Applicable from I_C = 0 mA to I_C = 10 mA)	30 V

ELECTRICAL CHARACTERISTICS @ 25°C free-air temperature

Symbol	Min	Max	Unit	Conditions
I_{CBO}	–	50	nA	2N5368, 2N5369, 2N5370 V_{CB} = 40 V, I_E = 0
	–	50	nA	2N5371 V_{CB} = 30 V, I_E = 0
I_{EBO}	–	50	nA	V_{EB} = 3 V, I_C = 0
BV_{CBO}	60	–	V	2N5368, 2N5369, 2N5370 I_C = 10 uA, I_E = 0
	40	–	V	2N5371 I_C = 10 uA, I_E = 0
BV_{EBO}	5	–	V	I_E = 10 uA, I_C = 0
BV_{CEO}	30	–	V	I_C = 10 mA, I_B = 0 (Note 1)
h_{FE}	20	–	–	2N5368
	50	–	–	2N5369
	75	–	–	2N5370 V_{CE} = 10 V, I_C = 1 mA
	20	–	–	2N5371
h_{FE}	40	–	–	2N5368
	75	–	–	2N5369
	150	–	–	2N5370 V_{CE} = 10 V, I_C = 10 mA, (Note 1)
	40	–	–	2N5371
h_{FE}	60	200	–	2N5368
	100	300	–	2N5369
	200	600	–	2N5370 V_{CE} = 10 V, I_C = 150 mA (Note 1)
	60	600	–	2N5371
V_{BE}	–	1.2	V	V_{CE} = 10 V, I_C = 150 mA (Note 1)
$V_{BE(sat)}$	–	1.3	V	I_C = 150 mA, I_B = 15 mA (Note 1)
$V_{CE(sat)}$	–	0.3	V	I_C = 150 mA, I_B = 15 mA (Note 1)
C_{cb}	–	8	pF	V_{CB} = 10 V, I_E = 0, f = 1 MHz (Note 2)
$[h_{fe}]$	2.5	–	–	V_{CE} = 10 V, I_C = 20 mA, f = 100 MHz
t_{on}	–	40	nsec	I_C = 150 mA, V_{CC} = 30 V, I_{B1} = 15 mA, (see fig. 1)
t_{off}	–	350	nsec	2N5368, 2N5369 I_C = 150 mA, V_{CC} = 30 V,
	–	400	nsec	2N5370, 2N5371 I_{B1} = I_{B2} = 15 mA (see fig. 2)

NOTES: 1. Pulse test: PW = 300 usec, duty cycle $\leq$ 2%.
2. C_{cb} measurement employs a three-terminal capacitance bridge incorporating a guard circuit. The emitter terminal shall be connected to the guard terminal of the bridge.

Package: TO-92

GENERAL PURPOSE NPN SILICON TRANSISTORS

ABSOLUTE MAXIMUM RATINGS @ 25°C (free air)

Characteristics	Unit
Storage temperature range	-55 to +150 °C
Operating Collector Junction Temperature	+150 °C
Lead temperature 1/16" from case 10 seconds max.	+260 °C
Emitter-base voltage	5 V
Collector-base voltage	60 V
Collector-emitter voltage (Applicable from I_C = 0 mA, to I_C = 10 mA)	30 V
Collector current	500 mA
Continuous device dissipation at or below 25°C free-air temperature	360 mW
Linear derating factor above 25°C	2.87 mW/°C

ELECTRICAL CHARACTERISTICS @ 25°C free-air temperature

Symbol	Min	Max	Unit	Conditions
I_{CBO}	–	10	nA	V_{CB} = 30 V, I_E = 0
BV_{CBO}	60	–	V	I_C = 10 uA, I_E = 0
BV_{EBO}	5	–	V	I_E = 100 nA, I_C = 0
BV_{CEO}	30	–	V	I_C = 10 mA, I_B = 0 (Note 1)
h_{FE}	100	500	–	2N5376 V_{CE} = 5 V, I_C = 10 uA
	40	200	–	2N5377 V_{CE} = 5 V, I_C = 10 uA
h_{FE}	120	600	–	2N5376 V_{CE} = 5 V, I_C = 1 mA
	100	500	–	2N5377 V_{CE} = 5 V, I_C = 1 mA
h_{FE}	150	–	–	2N5376 V_{CE} = 5 V, I_C = 10 mA (Note 1)
	120	–	–	2N5377
$V_{BE(sat)}$	0.65	0.80	V	I_C = 10 mA, I_B = 1 mA
$V_{CE(sat)}$	–	0.2	V	I_C = 10 mA, I_B = 1 mA
h_{ib}	20	32	Ohms	I_C = 1 mA, V_{CE} = 5 V, f = 1 kHz
h_{ob}	0.05	0.2	umhos	I_C = 1 mA, V_{CE} = 5 V, f = 1 kHz
h_{fe}	120	1000	–	2N5376 I_C = 1 mA, V_{CE} = 5 V, f - 1 kHz
	100	900	–	2N5377
C_{cb}	–	8	pF	V_{CB} = 10 V, I_E = 0, f = 1 MHz (Note 2)
$[h_{fe}]$	30	150	–	V_{CE} = 5 V, I_C = 500 uA, f = 10 MHz
NF	–	2.0	dB	2N5376 I_C = 10 uA, V_{CE} = 5 V, Rg = 10 Ohms,
	–	3.0	dB	2N5377 Bandwith = 10 Hz to 15.7 kHz

NOTES: 1. Pulse test: Pulse width = 300 usec, duty cycle $\leq$ 2 %.

2. C_{cb} measurement employs a three-terminal capacitance bridge incorporating a guard circuit. The emitter shall be connected to the guard terminal of the bridge.

2N5449, 2N5450, 2N5451
NPN SILICON AMPLIFIER TRANSISTORS

Package: To-92

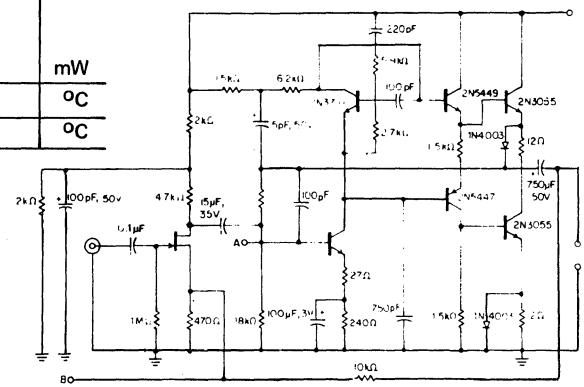
ABSOLUTE MAXIMUM RATINGS at 25°C free-air temperature (unless otherwise noted)

Characteristic	2N5449 / 2N5450	2N5451	Unit
Collector-Base Voltage	50	40	V
Collector-Emitter Voltage (See Note 1)	30	20	V
Emitter-Base Voltage	5	5	V
Continuous Collector Current	800		mA
Continuous Device Dissipation at (or below) 25°C Free-Air Temperature (See Note 2)	360		mW
Continuous Device Dissipation at (or below) 25°C Lead Temperature (See Note 3)	500		mW
Storage Temperature Range	-65 to 150		°C
Junction Temperature-Operating	260		°C

NOTES:

1. These values apply when the base-emitter diode is open-circuited.
2. Derate linearly to 150°C free-air temperature at the rate of 2.88 mW/deg.
3. Derate linearly to 150°C lead temperature at the rate of 4 mW/deg. Lead temperature is measured on the collector lead 1/16 inch from the case.

SILICON 15-WATT QUASI-COMPLEMENTARY POWER AMPLIFIER



***ELECTRICAL CHARACTERISTICS** AT 25°C FREE-AIR TEMPERATURE

Symbol	2N5449 Min	2N5449 Max	2N5450 Min	2N5450 Max	2N5451 Min	2N5451 Max	Unit	Test Conditions
$V_{(BR)CBO}$	50		50		40		V	I_C = 100 uA, I_E = 0
$V_{(BR)CEO}$	30		30		20		V	I_C = 10 mA, I_B = 0, See Note 4
$V_{(BR)EBO}$	5		5		5		V	I_E = 100 uA, I_C = 0
I_{CBO}		100		100		100	nA	V_{CB} = 20 V, I_B = 0
I_{EBO}		100		100		100	nA	V_{EB} = 3 V, I_C = 0
h_{fe}	100	300	50	150	30	600		V_{CE} = 2 V, I_C = 50 mA, See Note 4
V_{BE}	0.5	1	0.5	1	0.5	1	V	V_{CE} = 2 V, I_C = 100 mA, See Note 4
$V_{CE(sat)}$		0.6		0.8		1	V	I_B = 5 mA, I_C = 100 mA, See Note 4
$\lvert h_{fe} \rvert$	5		5		5			V_{CE} = 2 V, I_C = 50 mA, f = 20 MHz
C_{cb}		12		12		12	pF	V_{CB} = 10 V, I_E = 0, f = 1 MHz, See Note 5

NOTES: 4. These parameters must be measured using pulse techniques. Ip = 300 us, duty cycle — 3%.
5. C_{cb} is measured using three-terminal measurement techniques with the emitter guarded.

ABSOLUTE MAXIMUM RATINGS

Characteristic		Unit
Collector-Emitter Voltage	60	Vdc
Collector-Base Voltage	60	Vdc
Emitter-Base Voltage	4.0	Vdc
Collector Current - Continuous	500	MAdc
Total Device Dissipation @ T_A = 25°C	500	mW
Derate above 25°C	4.54	mW/°C
Total Device Dissipation @ T_C = 25°C	800	mW
Derate above 25°C	7.27	mW/°C
Operating and Storage Junction Temperature Range	-55 to +135	°C
Thermal Resistance, Junction to Case	0.137	°C/mW
Thermal Resistance, Junction to Ambient	0.220	°C/mW

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Min	Typ	Max	Unit	Conditions
BV_{CEO}	60	–	–	Vdc	I_C = 1.0 mAdc, I_B = 0
BV_{EBO}	4.0	–	–	Vdc	I_E = 100 *u*Adc, I_C = 0
I_{CBO}	–	–	100	nAdc	V_{CB} = 60 Vdc, I_E = 0
h_{FE}	50	125	–	–	I_C = 10 mAdc, V_{CE} = 1.0 Vdc
	50	150	–		I_C = 100 mAdc, V_{CE} = 1.0 Vdc
	–	90	–		I_C = 350 mAdc, V_{CE} = 1.0 Vdc
$V_{CE(sat)}$	–	0.08	0.25	Vdc	I_C = 100 mAdc, I_B = 10 mAdc
$V_{BE(sat)}$	–	0.75	–		I_C = 100 mAdc, I_B = 10 mAdc
$V_{BE(on)}$	–	0.7	1.2	Vdc	I_C = 100 mAdc, V_{CE} = 1.0 Vdc
f_T	50	200	–	MHz	I_C = 100 mAdc, V_{CE} = 1.0 Vdc, f = 100 MHz
C_{ob}	–	6.0	–	pF	V_{CB} = 10 Vdc, I_E = 0, f = 100 kHz
C_{ib}	–	15	–	pF	V_{BE} = 0.5 Vdc, I_C = 0, f = 100 kHz

MPS-A10

GENERAL PURPOSE NPN SILICON AMPLIFIER TRANSISTORS

Package: To-92

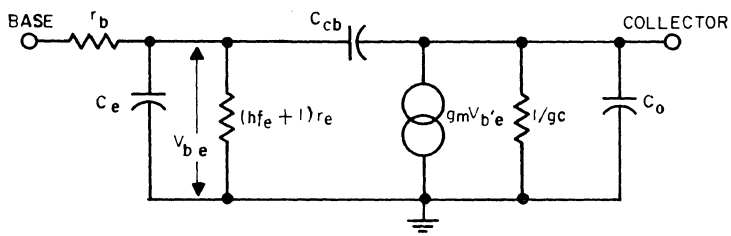
ABSOLUTE MAXIMUM RATINGS

Characteristic	Unit
Collector-Emitter Voltage	40 Vdc
Emitter-Base Voltage	4.0 Vdc
Collector Current - Continuous	100 mAdc
Total Device Dissipation @ T_A = 25°C	300 mW
Derate above 25°C	2.73 mW/°C
Operating and Storage Junction Temperature Range	-55 to +135 °C
Thermal Resistance, Junction to Ambient	0.367 °C/mW

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Min	Max	Unit	Conditions
BV_{CEO}	40	—	Vdc	I_C = 1.0 mAdc, I_B = 0
BV_{EBO}	4.0	—	Vdc	I_E = 100 *u*Adc, I_C = 0
I_{CBO}	—	100	nAdc	V_{CB} = 30 Vdc, I_E = 0
h_{FE}	40	400	—	I_C = 5.0 mAdc, V_{CE} = 10 Vdc
f_T	50	—	MHz	I_C = 5.0 mAdc, V_{CE} = 10 Vdc, f = 20 MHz
C_{ob}	—	4.0	pF	V_{CB} = 10 Vdc, I_E = 0, f = 100 kHz

Figure 1—Simplified AC Equivalent Circuit (Common Emitter)



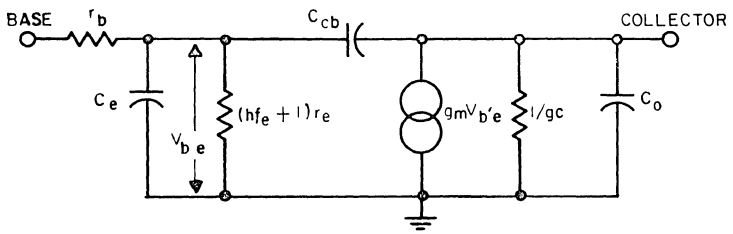
ABSOLUTE MAXIMUM RATINGS

Characteristic	Unit
Collector-Emitter Voltage	40 Vdc
Emitter-Base Voltage	4.0 Vdc
Collector Current - Continuous	100 mAdc
Total Device Dissipation @ T_A = 25°C	300 mW
Derate above 25°C	2.73 mW/°C
Operating and Storage Junction Temperature Range	-55 to +135 °C
Thermal Resistance, Junction to Ambient	0.367 °C/mW

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Min	Max	Unit	Conditions
BV_{CEO}	40	–	Vdc	I_C = 1.0 mAdc, I_B = 0
BV_{EBO}	4.0	–	Vdc	I_E = 100 uAdc, I_C = 0
I_{CBO}	–	100	nAdc	V_{CB} = 30 Vdc, I_E = 0
h_{FE}	40	400	–	I_C = 5.0 mAdc, V_{CE} = 10 Vdc
$V_{CE(sat)}$	–	0.25	Vdc	I_C = 10 mAdc, I_B = 1.0 mAdc
f_T	125	–	MHz	I_C = 5.0 mAdc, V_{CE} = 10 Vdc, f = 100 MHz
C_{ob}	–	4.0	pF	V_{CB} = 10 Vdc, I_E = 0, f = 100 kHz

Figure 1—Simplified AC Equivalent Circuit (Common Emitter)



MPS2711, MPS2712
LOW-POWER NPN SILICON SMALL-SIGNAL TRANSISTOR

Package: To-92

ABSOLUTE MAXIMUM RATINGS

Characteristic	Unit
Collector-Emitter Voltage	18 Vdc
Collector-Base Voltage	18 Vdc
Emitter-Base Voltage	5.0 Vdc
Collector Current	100 mAdc
Total Device Dissipation @ T_A = 25°C	310 mW
Total Device Dissipation @ T_C = 60°C	210 mW
Operating Junction Temperature	135 °C
Storage Temperature Range	-55 to +135 °C
Thermal Resistance, Junction to Ambient	0.357 °C/W

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Min	Max	Unit	Conditions
I_{CBO}	—	0.5	*u*Adc	V_{CB} = 18 Vdc, I_E = 0
	—	1.5		V_{CB} = 18 Vdc, I_E = 0, T_A = 100°C
I_{EBO}	—	0.5	*u*Adc	V_{EB} = 5 Vdc, I_C = 0
h_{FE}	30	90	—	V_{CE} = 4.5 Vdc, I_C = 2 mAdc MPS2711
	75	225		MPS2712
C_{ob}	—	4.0	pF	V_{CB} = 10 V, I_E = 0 f = 1 MHz
h_{fe}	30	120	—	V_{CE} = 10 Vdc, I_C = 2 mAdc, f = 1 kHz MPS2711
	80	200		MPS2712

Package: To-92 GENERAL PURPOSE NPN SILICON AMPLIFIER TRANSISTORS

ABSOLUTE MAXIMUM RATINGS

Characteristic	Unit
Collector-Base Voltage	25 Vdc
Collector-Emitter Voltage	25 Vdc
Emitter-Base Voltage	5.0 Vdc
Collector dc Current	100 mAdc
Total Device Dissipation	200 mW
@ 25°C Ambient Temperature	
Derating Factor above 25°C	2.67 mW/°C
Total Device Dissipation	120 mW
@ 55°C Ambient Temperature	
Derating Factor above 25°C	2.67 mW/°C
Junction Temperature-Operating	100 °C
Storage Temperature Range	-30 to +125 °C

ELECTRICAL CHARACTERISTICS (Tc = 25°C unless otherwise noted)

Symbol	Min	Max	Unit	Conditions
I_{CBO}	–	0.5	uA	V_{CB} = 25 V, I_E = 0
	–	15	uA	V_{CB} = 25 V, I_E = 0, T_A = 100°C
I_{EBO}	–	0.5	uA	V_{EB} = 5 V
h_{fe}			–	V_{CE} = 10 V, I_C = 2 mA
	90	180		MPS2923
	150	300		MPS2924
	235	470		MPS2925
C_{ob}	–	12	pF	V_{CB} = 10 V, I_E = 0, f = MHz

MPS2926, MPS3721

Package: To-92

GENERAL PURPOSE NPN SILICON TRANSISTOR

ABSOLUTE MAXIMUM RATINGS

Characteristic	Unit
Collector-Emitter Voltage	18 Vdc
Collector-Base Voltage	18 Vdc
Emitter-Base Voltage	5.0 Vdc
Collector Current	100 mAdc
Total Device Dissipation @ 25°C Ambient Temperature	310 mW
Total Device Dissipation @ 60°C Ambient Temperature	210 mW
Thermal Resistance, Junction to Ambient	0.357 °C/mW
Junction Temperature, Operating	135 °C
Storage Temperature Range	-55 to +135 °C

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Min	Typ	Max	Unit	Conditions
I_{CBO}	–	–	0.5	uA	V_{CB} = 18 Vdc, I_E = 0
	–	–	15		V_{CB} = 18 Vdc, I_E = 0, T_A = 100°C
I_{EBO}	–	–	0.5	uA	V_{EB} = 5 Vdc, I_C = 0
f_T	–	300	–	MHz	I_C = 4 mA, V_{CE} = 5 V MPS 2926
C_{ob}	–	–	3.5	pF	V_{CB} = 10 V, I_E = 0, f = 1 MHz
h_{fe}	35	–	470	–	V_{CE} = 10 V, I_C = 2 mA, f = 1 kHz MPS2926
	60	–	660		MPS3721

Package: To-92

NPN SILICON SMALL-SIGNAL AUDIO TRANSISTOR

ABSOLUTE MAXIMUM RATINGS

Characteristic	Unit
Collector-Emitter Voltage	25 Vdc
Collector-Base Voltage	25 Vdc
Emitter-Base Voltage	5.0 Vdc
Collector Current	100 mAdc
Total Device Dissipation @ T_A = 25°C	310 mW
Total Device Dissipation @ T_C = 60°C	210 mW
Operating Junction Temperature	135 °C
Storage Temperature Range	-55 to +135 °C
Thermal Resistance, Junction to Ambient	0.357 °C/mW

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Min	Max	Unit	Conditions
BV_{CEO}	25	—	Vdc	I_C = 1 mAdc, I_B = 0
I_{CBO}	—	0.1	uAdc	V_{CB} = 18 Vdc, I_E = 0
I_{EBO}	—	0.1	uAdc	V_{EB} = 5 Vdc, I_C = 0
h_{FE}	150	300	—	V_{CE} = 4.5 Vdc, I_C = 2 mAdc MPS3392
	90	180		MPS3393
	55	110		MPS3394
	150	500		MPS3395
C_{ob}	—	3.5	pF	V_{CB} = 10 V, I_E = 0, f = 1 MHz
h_{fe}	150	500	—	V_{CE} = 4.5 V, I_C = 2 mA, f = 1 kHz MPS3392
	90	400		MPS3393
	55	300		MPS3394
	150	800		MPS3395

GENERAL PURPOSE NPN SILICON RFAMPLIFIER TRANSISTORS

ABSOLUTE MAXIMUM RATINGS

Characteristic	Unit
Collector-Emitter Voltage	45 Vdc
Collector-Base Voltage	45 Vdc
Emitter-Base Voltage	4.0 Vdc
Total Device Dissipation @ T_A = 25°C	310 mW
Derate above 25°C	2.81 mW/°C
Operating and Storage Junction Temperature Range	-55 to +135 °C
Thermal Resistance, Junction to Ambient	0.357 °C/mW

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Min	Typ	Max	Unit	Conditions
$BV_{CEO(sus)}$*	45	–	–	Vdc	I_C = 10 mAdc, I_B = 0
BV_{CBO}	45	–	–	Vdc	I_C = 100 *u*Adc, I_E = 0
BV_{EBO}	4.0	–	–	Vdc	I_E = 10 *u*Adc, I_C = 0
I_{CBO}	–	–	50	nAdc	V_{CB} = 35 Vdc, I_E = 0
	–	–	5.0	*u*Adc	V_{CB} = 35 Vdc, I_E = 0, T_A = 65°C
h_{FE}	40	–	160	–	I_C = 10 mAdc, V_{CE} = 10 Vdc
f_T	200	–	–	MHz	I_C = 10 mAdc, V_{CE} = 15 Vdc, f = 100 MHz
C_{ob}	–	–	3.5	pF	V_{CB} = 10 Vdc, I_E = 0, f = 100 kHz
r'_bC_c	–	–	55	ps	I_E = 10 mAdc, V_{CB} = 15 Vdc, f = 31.8 MHz
NF	–	4.0	–	dB	I_C = 3.0 mAdc, V_{CE} = 10 Vdc, R_S = 300 ohms, f = 1.0 MHz

*Pulse Test: Pulse Width $\leq$ 300 us; Duty Cycle $\leq$ 1.0%.

ABSOLUTE MAXIMUM RATINGS

Characteristics	MPS3704 MPS3705	MPS3706	Unit
Collector-Emitter Voltage ...	30	20	Vdc
Collector-Base Voltage	50	40	Vdc
Emitter-Base Voltage	5.0		Vdc
Collector Current - Continuous	600		mAdc
Total Device Dissipation @ T_A = 25°C	310		mW
Derate above 25°C	2.81		mW/°C
Operating and Storage Junction Temperature Range	-55 to +135		°C
Thermal Resistanct, Junction to Ambient	0.357		°C/mW

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Min	Max	Unit	Conditions	
BV_{CEO}*	30	–	Vdc	I_C = 10 mAdc, I_E = 0	MPS3704
	30	–			MPS3705
	20	–			MPS3706
BV_{CBO}	50	–	Vdc	I_C = 100 uAdc, I_E = 0	MPS3704
	50	–			MPS3705
	40	–			MPS3706
BV_{EBO}	5.0	–	Vdc	I_E = 100 uAdc, I_C = 0	
I_{CBO}	–	100	nAdc	V_{CB} = 20 Vdc, I_E = 0	
I_{EBO}	–	100	nAdc	V_{BE} = 3 Vdc, I_C = 0	
h_{FE}*	100	300	–	I_C = 50 mAdc, V_{CE} = 2 Vdc	MPS3704
	50	150			MPS3705
	30	600			MPS3706
$V_{CE(sat)}$*	–	0.6	Vdc	I_C = 100 mAdc, I_B = 5 mAdc	MPS3704
	–	0.8			MPS3705
	–	1.0			MPS3706
$V_{BE(on)}$*	0.5	1.0	Vdc	I_C = 100 mAdc, V_{CE} = 2 Vdc	
f_T	100	–	MHz	I_C = 50 mAdc, V_{CE} = 2 Vdc, f = 20 MHz	
C_{ob}	–	12	pF	V_{CB} = 10 Vdc, I_E = 0, f = 1 MHz	

*Pulse Test: Pulse Width = 300 us; Duty Cycle = 2%.

MPS3707 thru MPS3711

Package: To-92

GENERAL PURPOSE NPN SILICON AMPLIFIER TRANSISTOR

ABSOLUTE MAXIMUM RATINGS

Characteristics	Unit
Collector-Emitter Voltage	30 Vdc
Collector-Base Voltage	30 Vdc
Emitter-Base Voltage	6.0 Vdc
Collector Current	30 mAdc
Total Device Dissipation @ T_A = 25°C	310 mW
Total Device Dissipation @ T_C = 60°C	210 mW
Operating Junction Temperature	135 °C
Storage Temperature Range	-55 to +135 °C
Thermal Resistance, Junction to Ambient	0.357 °C/W

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Min	Max	Unit	Conditions	
BV_{CEO}	30	–	Vdc	I_C = 1 mAdc, I_B = 0	
I_{CBO}	–	100	nAdc	V_{CB} = 20 Vdc, I_E = 0	
I_{EBO}	–	100	nAdc	V_{EB} = 6 Vdc, I_C = 0	
h_{FE}	100	400	–	I_C = 100 uAdc, V_{CE} = 5 Vdc	MPS3707
	45	660		I_C = 1 mAdc, V_{CE} = 5 Vdc	MPS3708
	45	165			MPS3709
	90	330			MPS3710
	180	660			MPS3711
$V_{CE(sat)}$	–	1.0	Vdc	I_C = 10 mAdc, I_B = 0.5 mAdc	
V_{BE}	0.5	1.0	Vdc	I_C = 1 mAdc, V_{CE} = 5 Vdc	
h_{FE}	100	550	–	I_C = 100 uAdc, V_{CE} = 5 Vdc, f = 1 kHz MPS3707	
	45	800		I_C = 1 mAdc, V_{CE} = 5 Vdc, f = 1 kHz MPS3708	
	45	250			MPS3709
	90	450			MPS3710
	180	800			MPS3711
NF	–	5.0	dB	V_{CE} = 5 V, I_C = 100 uA, R_G = 5 kΩ, Noise Bandwidth = 15.7 kHz Note 1	MPS3707

Note 1 Average Noise Figure is measured in an amplifier with low frequency response down 3 dB at 10 Hz.

Package: To-92

GENERAL PURPOSE NPN SILICON AMPLIFIER TRANSISTOR

ABSOLUTE MAXIMUM RATINGS

Characteristics	Unit
Collector-Emitter Voltage	25 Vdc
Collector-Base Voltage	25 Vdc
Emitter-Base Voltage	5.0 Vdc
Collector Current - Continuous	100 mAdc
Total Device Dissipation @ T_A = 25°C	210 mW
Derate above 25°C	1.91 mW/°C
Operating and Storage Junction Temperature Range	-55 to +135 °C
Thermal Resistance, Junction to Ambient	0.524 °C/mW

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Min	Typ	Max	Unit	Conditions
BV_{CEO}	25	–	–	Vdc	I_C = 10 mAdc, I_B = 0
I_{CES}	–	–	100	nAdc	V_{CE} = 25 Vdc, V_{BE} = 0
I_{CBO}	–	–	100	nAdc	V_{CB} = 25 Vdc, I_E = 0
	–	–	10	*u*Adc	V_{CB} = 25 Vdc, I_E = 0, T_A = 100°C
I_{EBO}	–	–	100	nAdc	V_{BE} = 5.0 Vdc, I_C = 0
h_{FE}	100	–	500	–	I_C = 10 mAdc, V_{CE} = 10 Vdc
$V_{CE(sat)}$	–	–	0.25	Vdc	I_C = 10 mAdc, I_B = 1.0 mAdc
$V_{BE(sat)}$	–	0.75	–	Vdc	I_C = 10 mAdc, I_B = 1.0 mAdc
$V_{BE(on)}$	0.5	–	1.2	Vdc	I_C = 10 mAdc, V_{CE} = 10 Vdc
f_T	–	120	–	MHz	I_C = 2.0 mAdc, V_{CE} = 5.0 Vdc
C_{cb}	1.6	–	10	pF	V_{CB} = 0, I_E = 0, f = 1.0 MHz
h_{fe}	100	–	750	–	I_C = 10 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz

MPS6530 thru MPS6532

NPN SILICON AMPLIFIER TRANSISTORS

Package: To-92

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Characteristic			Unit
Collector-Base Voltage			
MPS6530, MPS5631	60		Vdc
MPS6532	50		
MPS6530, MPS6531	40		
MPS6532	30		
Emitter-Base Voltage	5.0	4.0	

Collector Current	600	600	mAdc
Total Device Dissipation			
@ T_A = 60°C	210	210	mW
@ T_A = 25°C	310	310	
Thermal Resistance, Junction to Ambient	0.357	0.357	°C/mW
Junction Temperature	135	135	°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Min	Typ	Max	Unit	Conditions	
BV_{CBO}	60	–	–	Vdc	I_C = 10 *u*Adc, I_E = 0	MPS6530, MPS6531
	50	–	–			MPS6532
BV_{CEO}	40	–	–	Vdc	I_C = 10 mAdc, I_B = 0	MPS6530, MPS6531
	30	–	–			MPS6532
BV_{EBO}	5.0	–	–	Vdc	I_B = 10 *u*Adc, I_C = 0	
I_{CBO}	–	–	0.05	*u*Adc	V_{CB} = 40 Vdc, I_E = 0	MPS6530, MPS6531
	–	–	0.1			MPS6532
	–	–	2.0		V_{CB} = 30 Vdc, I_E = 0, T_A = 60°C	MPS6530, MPS6531
	–	–	5.0		V_{CB} = 30 Vdc, I_E = 0, T_A = 60°C	MPS6532
h_{FE}	30	75	–	–	I_C = 10 mAdc, V_{CE} = V_{CE} = 1 Vdc	MPS6530
	60	120	–			MPS6531
	40	85	120		I_C = 100 mAdc, V_{CE} = 1 Vdc	MPS6530
	90	150	270			MPS6531
	30	–	–			MPS6532
	25	60	–		I_C = 500 mAdc, V_{CE} = 10 Vdc	MPS6530
	50	80	–			MPS6531
$V_{CE(sat)}$	–	0.2	0.5	Vdc	I_C = 100 mAdc, I_B = 10 mAdc	MPS6530, MPS6532
	0.13	0.13	0.3			MPS6531
$V_{BE(sat)}$	–	0.82	1.0	Vdc	I_C = 100 mAdc, I_B = 10 mAdc	MPS6530, MPS6531
	–	0.85	1.2			MPS6532
C_{ob}	–	3.5	5.0	pF	V_{CB} = 10 Vdc, I_E = 0, f = 100 kHz	
f_T	–	390	–	MHz	I_C = 50 mAdc, V_{CE} = 10 Vdc	

Package: To-92

GENERAL PURPOSE NPN SILICON AMPLIFIER TRANSISTORS

ABSOLUTE MAXIMUM RATINGS

Characteristics	Unit
Collector-Emitter Voltage	45 Vdc
Collector-Base Voltage	60 Vdc
Emitter-Base Voltage	4.0 Vdc
Collector Current - Continuous	200 mAdc
Total Device Dissipation @ T_A = 25°C	310 mW
Derate above 25°C	2.81 mW/°C
Operating and Storage Junction Temperature Range	-55 to +135 °C
Thermal Resistance, Junction to Ambient	0.357 °C/mW

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Min	Typ	Max	Unit	Conditions
BV_{CEO}	45	–	–	Vdc	I_C = 1 mAdc, I_B = 0
BV_{CBO}	60	–	–	Vdc	I_C = 100 uAdc, I_E = 0
BV_{EBO}	4.0	–	–	Vdc	I_E = 100 uAdc, I_C = 0
I_{CBO}	–	–	100	nAdc	V_{CB} = 30 Vdc, I_E = 0
h_{FE}	40	–	160	–	I_C = 10 mAdc, V_{CE} = 10 Vdc MPS6565
	100	–	400		MPS6566
$V_{CE(sat)}$	–	0.1	0.4	Vdc	I_C = 10 mAdc, I_B = 1 mAdc
C_{ob}	–	–	3.5	pF	V_{CB} = 10 Vdc, I_E = 0, f = 100 kHz
C_{ib}	–	3.7	–	pF	V_{BE} = 0.5 Vdc, I_C = 0, f = 100 kHz
h_{fe}	2.0	–	–	–	I_C = 10 mAdc, V_{CE} = 10 Vdc, f = 100 MHz
h_{oe}	–	60	–	umhos	I_C = 10 mAdc, V_{CE} = 10 Vdc, f = 1 kHz
h_{ie}	–	500	–	ohms	I_C = 10 mAdc, V_{CE} = 10 Vdc, f = 1 kHz
h_{re}	–	2.5	–	$X10^{-4}$	I_C = 10 mAdc, V_{CE} = 10 Vdc, f = 1 kHz
NF	–	4.0	–	dB	I_C = 100 uAdc, V_{CE} = 5 Vdc, R_S = 1000 ohms, f = 10 Hz to 15.7 kHz

MPS6591Ⓕ

NPN SILICON AMPLIFIER TRANSISTOR

Package: To-92

High Voltage ..... BV_{CEO} = 80 V (Min) MPS6590
Low Noise ..... NF = 3.0 dB (Typ) Wideband

ABSOLUTE MAXIMUM RATINGS (Note 1)

Characteristics	Unit
Storage Temperature	-55 to +150 °C
Operating Junction Temperature	-55 to +150 °C
Total Dissipation (Notes 2 and 3)	
at 25°C Case Temperature	1.0 W
at 25°C Ambient Temperature	.625 W
at 70°C Ambient Temperature	.400 W
Collector to Base Voltage	60 V
Collector to Emitter Voltage (Note 4)	50 V
Emitter to Base Voltage	4.0 V
DC Collector Current	250 mA

ELECTRICAL CHARACTERISTICS (25°C Free Air Temperature unless otherwise noted)

Symbol	Min	Typ	Max	Unit	Test Conditions
BV_{CEO}	50			Volts	I_C = 1.0 mA, I_B = 0
BV_{CBO}	60			Volts	I_C = 100 uA, I_E = 0
BV_{EBO}	4.0			Volts	I_E = 100 uA, I_C = 0
I_{CBO}				nA	V_{CB} = 50 V, I_E = 0
I_{CBO}			100	nA	V_{CB} = 30 V, I_E = 0
h_{FE}	40				I_C = 10 mA, V_{CE} = 10 V
$V_{CE(sat)}$			0.6	Volt	I_C = 10 mA, I_B = 1.0 mA
C_{cb}			12	pF	V_{CB} = 10 V, I_E = 0, f = 100 kHz
C_{eb}			50	pF	V_{BE} = 0.5 V, I_C = 0, f = 100 kHz
h_{ie}		1.4		kΩ	I_C = 10 mA, V_{CE} = 5.0 V, f = 1.0 kHz
h_{re}		0.8		$X10^{-4}$	I_C = 10 mA, V_{CE} = 5.0 V, f = 1.0 kHz
h_{fe}	2.0				I_C = 10 mA, V_{CE} = 10W, f = 30 MHz
h_{oe}		75		umhos	I_C = 10 mA, V_{CE} = 5.0 V, f = 1.0 kHz
NF		3.0		dB	I_C = 100 uA, V_{CE} = 5.0 V, f = 10 Hz to 15.7 kHz, R_s = 4kΩ

NOTES:
(1) These ratings are limiting values above which the serviceability of any individual semiconductor device may be impaired.
(2) These are steady state limits. The factory should be consulted on applications involving pulsed or low duty cycle operations.
(3) These ratings give a maximum junction temperature of 150°C and junction to case thermal resistance of 125° C/Watt (derating factor of 8.0 mW/°C); junction to ambient thermal resistance of 200°C/Watt (derating factor of 5.0 mW/°C).
(4) Rating refers to a high current point where collector to emitter voltage is lowest.
(5) Pulse conditions: length = 300 us; duty cycle = 1%.

ABSOLUTE MAXIMUM RATINGS

Characteristics	Unit
Collector-Emitter Voltage	90 Volts
Collector-Emitter Voltage	140 Volts
Collector-Base Voltage	120 Volts
Emitter-Base Voltage	7.0 Volts
Collector Current	1.0 A
Total Device Dissipation @ $T_A = 25°C$	1.0 Watt
Derate above 25°C	5.71 mW/°C
Total Device Dissipation @ $T_C = 25°C$	5.0 Watts
Derate above 25°C	28.6 mW/°C
Operating and Storage Junction Temperature Range	−65 to +200 °C

ELECTRICAL CHARACTERISTICS ($T_A = 25°C$ unless otherwise noted)

Symbol	Min	Max	Unit	Conditions
$BV_{CEO(sus)}$*	90	–	Volts	$I_C = 100$ mA, $I_B = 0$
$BV_{CER(sus)}$	140	–	Volts	$I_C = 100$ mA, $R_{BE} = 10$ ohms
BV_{CBO}	120	–	Volts	$I_C = 100\ \mu A$, $I_E = 0$
BV_{EBO}	7.0	–	Volts	$I_E = 100\ \mu A$, $I_C = 0$
I_{CBO}	–	10	μA	$V_{CB} = 90$ Volts, $I_E = 0$, $T_A = 150°C$
I_{EBO}	–	0.01	μA	$V_{BE} = 5.0$ Volts, $I_C = 0$
h_{FE}*	60	200	–	$I_C = 150$ mA, $V_{CE} = 10$ Volts
$V_{CE(sat)}$	–	0.5	Volt	$I_C = 150$ mA, $I_B = 15$ mA
$V_{BE(sat)}$	–	1.1	Volts	$I_C = 150$ mA, $I_B = 15$ mA
C_{ob}	–	15	pF	$V_{CB} = 10$ Volts, $I_E = o$, 100 kHz $\leq f \leq$ 1.0 MHz
C_{ib}	–	85	pF	$V_{BE} = 0.5$ Volts, $I_C = 0$, 100 kHz $\leq f \leq$ 1.0 MHz
h_{ib}	4.0	8.0	ohms	$I_C = 5.0$ mA, $V_{CB} = 10$ Volts, f = 1.0 kHz
h_{rb}	–	3.0	$X10^{-4}$	$I_C = 5.0$ mA, $V_{CB} = 10$ Volts, f = 1.0 kHz
h_{fe}	50	275	–	$I_C = 5.0$ mA, $V_{CE} = 5.0$ Volts, f = 1.0 kHz
h_{ob}	–	0.5	μmho	$I_C = 5.0$ mA, $V_{CB} = 10$ Volts, f = 1.0 kHz

* Pulse Test: Pulse Width $\leq 300\ \mu s$; Duty Cycle $\leq 2.0\%$

2N2868®

HIGH-SPEED NPN SILICON, HIGH CURRENT SWITCHING TRANSISTOR

Package: TO-5

ABSOLUTE MAXIMUM RATINGS (Note 1)

Characteristics	Unit
Storage Temperature	−65°C to +300°C
Operating Junction Temperature	200°C Maximum
Lead Temperature (Soldering, no time limit)	250°C Maximum
Total Device Dissipation	
@ T_C = 25°C (Notes 2 and 3)	2.8 Watts
@ T_C = 100°C (Notes 2 and 3)	1.6 Watts
@ T_A = 25°C (Notes 2 and 3)	0.8 Watt
Collector-Base Voltage	60 Volts
Collector-Emitter Voltage (Note 4)	40 Volts
Emitter-Base Voltage	7.0 Volts
Collector Current	1.0 Amp

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Min	Max	Unit	Conditions
h_{FE}	40	120	–	I_C = 150 mA, V_{CE} = 10 Volts (Note 5)
h_{FE}	30	–	–	I_C = 150 mA, V_{CE} = 1.0 Volt (Note 5)
h_{FE}	30	–	–	I_C = 10 mA, V_{CE} = 10 Volts
h_{FE}	20	–	–	I_C = 500 mA, V_{CE} = 10 Volts (Note 5)
h_{FE}(−55°C)	20	–	–	I_C = 10 mA, V_{CE} = 10 Volts
$V_{CE(sat)}$	–	0.25	Volt	I_C = 150 mA, I_B = 15 mA
$V_{BE(sat)}$	–	1.3	Volts	I_C = 150 mA, I_B = 15 mA
h_{fe}	2.5	–	–	I_C = 50 mA, V_{CE} = 10 Volts
I_{CBO}	–	10	nA	V_{CB} = 30 Volts, I_E = 0
I_{CBO}(150°C)	–	15	μA	V_{CB} = 30 Volts, I_E = 0
I_{EBO}	–	50	nA	V_{EB} = 5.0 Volts, I_C = 0
I_{CEX}	–	100	nA	V_{CE} = 30 Volts, V_{EB} = 3.0 Volts
I_{EBX}	–	100	nA	V_{CE} = 30 Volts, V_{EB} = 3.0 Volts
BV_{CBO}	60	–	Volts	I_C = 100μA, I_E = 0

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Min	Max	Unit	Conditions
$V_{CEO(sust)}$	40	–	Volts	I_C = 25 mA (pulsed), I_B = 0 (Notes 4 and 5)
BV_{EBO}	7 0	–	Volts	I_E = 100 μA, I_C = 0
C_{ob}	–	20	pf	V_{CB} = 10 Volts, I_E = 0
τ_b	–	2.0	μsec	See Figure I

NOTES:

(1) These ratings are limiting values above which the serviceability of any individual semiconductor device may be impaired.

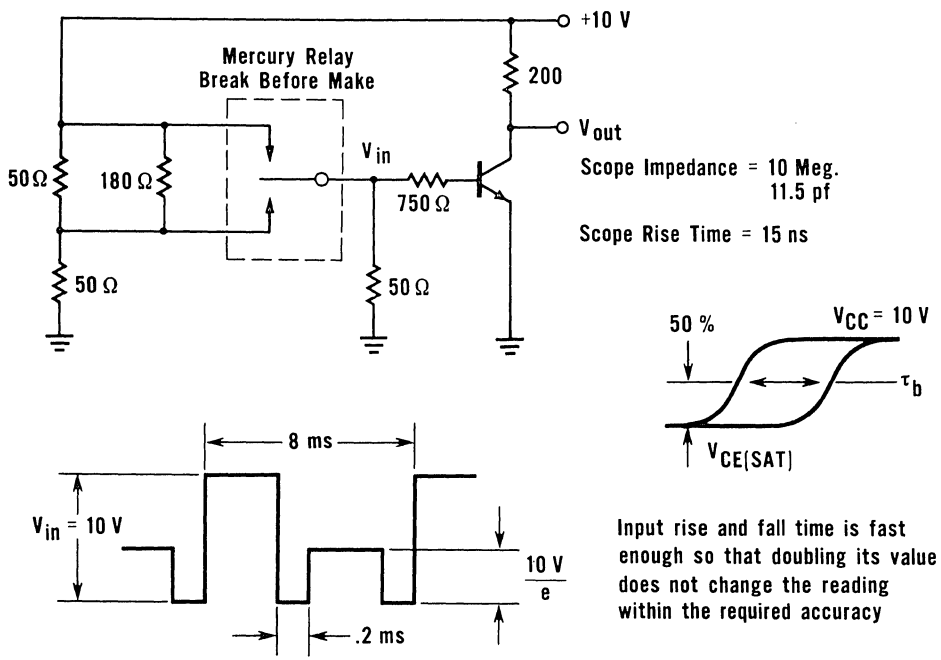
(2) These are steady state limits. The factory should be consulted on applications involving pulsed or low duty cycle operations.

(3) These ratings give a maximum junction temperature of 200°C and junction-to-case thermal resistance of 62.5°C/Watt (derating factor of 1 6 mW/°C; junction-to-ambient thermal resistance of 2 18°C/Watt (derating factor of 4.6 mW/°C).

(4) This rating refers to a high-current point where collector-to-emitter voltage is lowest. For more information send for Fairchild Publication APP-4.

(5) Pulse Conditions: length ≤300 μsec; duty cycle ≤2%.

FIGURE 1



Input rise and fall time is fast enough so that doubling its value does not change the reading within the required accuracy

2N3252, 2N3253

NPN SILICON HIGH-CURRENT SATURATED SWITCHING AND CORE DRIVER TRANSISTORS

Package: TO-5

ABSOLUTE MAXIMUM RATINGS

Characteristics		Unit
Collector-Base Voltage	2N3252	60 Volts
	2N3253	75 Volts
Collector-Emitter Voltage	2N3252	30 Volts
	2N3253	40 Volts
Emitter-Base Voltage		5 Volts
Total Device Dissipation @ T_C = 25°C		5 Watts
Derate above 25°C		28.6 mW/°C
Total Device Dissipation @ T_A = 25°C		1.0 Watt
Derate above 25°C		5.71 mW/°C
Junction Operating Temperature Range		−65 to +200 °C
Storage Temperature Range		−65 to +200 °C
Thermal Resistance: 2N3252		35°C/W
Thermal Resistance: 2N3253		0.175°C/mW

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Min	Max	Unit	Conditions
C_{ob}	–	12	pF	V_{CB} = 10 Volts, I_E = 0, f= 100 kHz
C_{ib}	–	80	pF	V_{EB} = 0.5 Volt, I_C = 0, f = 100 kHz
f_T	200	–	MHz	2N3252 I_C = 50 mA, V_{CE} = 10 Volts,
	175	–	MHz	2N3253 f = 100 MHz
Q_T	–	5	nC	I_C = 500 mA, I_{B1} = 50 mA, V_{CC} = 30 Volts
t_d	–	15	ns	I_C = 500 mA, I_{B1} = 50 mA
t_r	–	30	ns	2N3252 V_{CC} = 30 Volts, V_{BE} = 2 Volts
	–	35	ns	2N3253 V_{CC} = 30 Volts, V_{BE} = 2 Volts
t_s	–	40	ns	I_C = 500 mA, I_{B1} = I_{B2} = 50 mA
t_f	–	30	ns	V_{CC} = 30 Volts
I_{CBO}	–	0.50	μA	(2N3252) V_{CB} = 40 Volts, I_E = 0
I_{CBO}	–	75	μA	(2N3252) V_{CB} = 40 Volts, I_E = 0, T_A = 100°C
I_{CBO}	–	0.50	μA	(2N3253) V_{CB} = 60 Volts, I_E = 0

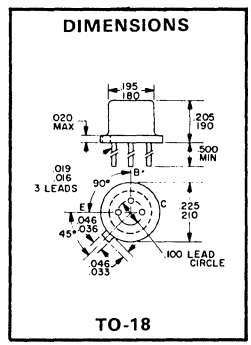
ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Min	Max	Unit	Conditions
I_{CBO}	–	75	μA	(2N3253) V_{CB} = 60 Volts, I_E = 0, T_A = 100°C
I_{EBO}	–	0.05	μA	V_{BF} = 4 Volts, I_C = 0
I_{CEX}	–	0.5	μA	(2N3252) V_{CE} = 40 Volts, $V_{EB(off)}$ = 4 Volts
I_{CEX}	–	0.5	μA	(2N3253) V_{CE} = 60 Volts, $V_{EB(off)}$ = 4 Volts
I_{BL}	–	0.50	μA	(2N3252) V_{CE} = 40 Volts, $V_{EB(off)}$ = 4 Volts
I_{BL}	–	0.50	μA	(2N3253) V_{CE} = 60 Volts, $V_{EB(off)}$ = 4 Volts
BV_{CBO}	60	–	Volts	(2N3252) I_C = 10 μA, I_E = 0
	75	–	Volts	(2N3253)
BV_{CEO}*	30	–	Volts	(2N3252) I_C = 10 mA, pulsed, I_B = 0*
	40	–	Volts	(2N3253)
BV_{EBO}	5	–	Volts	I_E = 10 μA, I_C = 0
$V_{CE(sat)}$*	–	0.3	Volt	(2N3252) I_C = 150 mA, I_B = 15 mA*
	–	0.35	Volt	(2N3253)
$V_{CE(sat)}$*	–	0.5	Volt	(2N3252) I_C = 500 mA, I_B = 50 mA
	–	0.60	Volt	(2N3253)
$V_{CE(sat)}$*	–	1.0	Volt	(2N3252) I_C = 1.0 A, I_B = 100 mA
	–	1.2	Volts	(2N3253)
$V_{BE(sat)}$*	–	1.0	Volt	I_C = 150 mA, I_B = 15mA*
$V_{BE(sat)}$*	0.7	1.3	Volts	I_C = 500 mA, I_B = 50 mA
$V_{BE(sat)}$*	–	1.8	Volts	I_C = 1.0 A, I_B = 100 mA
h_{FE}*	30	–	–	(2N3252) I_C = 150 mA, V_{CE} = 1 Volt*
	25	–	–	(2N3253)
h_{FE}*	30	90	–	(2N3252) I_C = 500 mA, V_{CE} = 1 Volt
	25	75	–	(2N3253)
h_{FE}*	25	–	–	(2N3252) I_C = 1 A, V_{CE} = 5 Volts
	20	–	–	(2N3253)

* Pulse Test: Pulse Width = 300 μs, Duty Cycle = 2%.

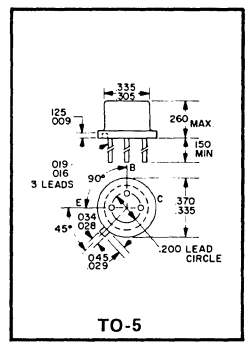
HIGH SPEED NPN SILICON PLANAR EPITAXIAL HIGH-VOLTAGE HIGH-CURRENT TRANSISTORS

2N4013-14



TO-18

2N3724-25



TO-5

- **High Voltage: 80V min. 2N3725, 2N4014**
- **High Gain: 65 typ. @ 1000 mA**
- **Low V_{CE} (sat): 0.5V typ. @ 1000 mA**
- **Low C_{ob}: 4.8 pF typ. @ 10V. 2N3725, 2N4014**
- **Fast t_{on}: 18 nsec typ. @ 500mA**
- **Fast t_{off}: 45 nsec typ. @ 500mA**

The ITT 2N3724 • 2N3725 and 2N4013 • 2N4014 are high-voltage, high-current NPN silicon planar epitaxial transistors useful for applications requiring breakdown voltages up to 50V and operating current to one ampere. Low saturation voltage and fast switching times make the transistor ideal for high-frequency amplifiers, core drivers, relay drivers and pulse generators.

ABSOLUTE MAXIMUM RATINGS

CHARACTERISTICS	2N3724 2N4013	2N3725 2N4014	UNITS
Collector-to-Base Voltage	50	80	Volts
Collector-to-Emitter Voltage (shorted base)	50	80	Volts
Collector-to-Emitter Voltage (open base)	30	50	Volts
Emitter-to-Base Voltage	6.0	6.0	Volts
Collector Current (300 μsec; 1% duty cycle)	1.0	1.0	Amps
Junction Temperature (op. and stg.)	−65 to +200		°C
Maximum Power Dissipation	**2N4013 2N4014**	**2N3724 2N3725**	
Total Dissipation @ T_C=25°C	1.2	3.5	Watts
(derate above 25°C)	(6.8 mW/°C)	(20mW/°C)	
Total Dissipation @ T_A=25°C	0.36	0.8	Watts
(derate above 25°C)	(2.06 mW/°C)	(4.56 mW/°C)	

ELECTRICAL CHARACTERISTICS @ 25°C unless otherwise noted.

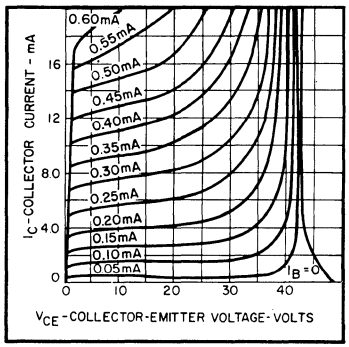
SYMBOL	2N3724 2N4013 MIN.	2N3724 2N4013 TYP.	2N3724 2N4013 MAX.	2N3725 2N4014 MIN.	2N3725 2N4014 TYP.	2N3725 2N4014 MAX.	UNIT	CONDITIONS
BV_{CBO}	**50**			**80**			**Vdc**	**I_C=10μA**
BV_{CES}	50			80			Vdc	I_C=10μA
LV_{CEO}[1,2]	**30**			**50**			**Vdc**	**I_C=10mA**
BV_{EBO}	6.0			6.0			Vdc	I_E=10μA
h_{FE}[1]	30	60		30	60			I_C=10mA V_{CE}=1.0V
	60	90	150	60	90	150		I_C=100mA V_{CE}=1.0V
	40	65		40	65			I_C=300mA V_{CE}=1.0V
	35	50		35	50			I_C=500mA V_{CE}=1.0V
	25	45		20	40			I_C=800mA V_{CE}=2.0V
	30	**65**		**25**	**65**			**I_C=1000mA V_{CE}=5.0V**
	30	45		30	40			I_C=100mA V_{CE}=1.0V T_A=−55°C
	20	40		20	35			I_C=500mA V_{CE}=1.0V T_A=−55°C
V_{CE}(sat)[1]		0.11	0.25		0.19	0.25	Vdc	I_C=10mA I_B=1.0mA
		0.13	0.2		0.21	0.26	Vdc	I_C=100mA I_B=10mA
		0.22	0.32		0.31	0.4	Vdc	I_C=300mA I_B=30mA
		0.3	0.42		0.4	0.52	Vdc	I_C=500mA I_B=50mA
		0.4	0.65		0.5	0.8	Vdc	I_C=800mA I_B=80mA
		0.5	**0.75**		**0.6**	**0.95**	**Vdc**	**I_C=1000mA I_B=100mA**
V_{BE} (sat)[1]		0.64	0.76		0.64	0.76	Vdc	I_C=10mA I_B=1.0mA
		0.75	0.86		0.75	0.86	Vdc	I_C=100mA I_B=10mA
		0.89	1.1		0.89	1.1	Vdc	I_C=300mA I_B=30mA
	0.9	0.95	1.2	0.9	0.95	1.2	Vdc	I_C=500mA I_B=50mA
		1.0	1.5		1.0	1.5	Vdc	I_C=800mA I_B=80mA
		1.1	1.7		1.1	1.7	Vdc	I_C=1000mA I_B=100mA
I_{CBO}		0.25	1.7				μA	V_{CB}=40V
					0.33	1.7	μA	V_{CB}=60V
		27	120				μA	V_{CB}=40V T_A=100°C
					25	120	μA	V_{CB}=60V T_A=100°C
C_{ob}		**6.0**	**12**		**4.8**	**10**	**pF**	**V_{CB}=10V**
C_{ib}		40	55		40	55	pF	V_{EB}=0.5V
h_{fe}	3.0	4.5		3.0	4.5			I_C=50mA V_{CE}=10V f=100MHz
t_{on}		**18**	**35**		**18**	**35**	**nsec**	**I_C≈500mA I_{B1}≈50mA I_{B2}≈50mA**
t_{off}		**45**	**60**		**45**	**60**	**nsec**	

NOTES: 1. Pulsed width ≤300 μsec; 1% duty cycle.
2. Lowest emitter-to-collector voltage.

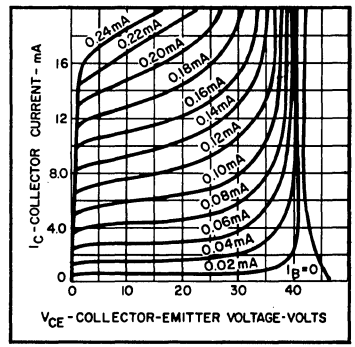
COLLECTOR CHARACTERISTICS 2N3724 2N4013

Collector Current vs. Collector Voltage, Low Base Current

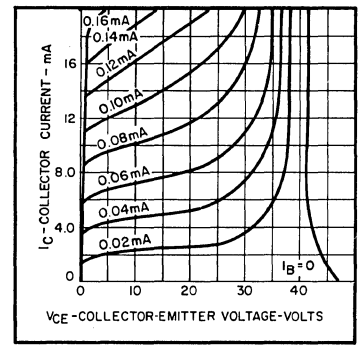
$T_A = -55°C$



$T_A = 25°C$

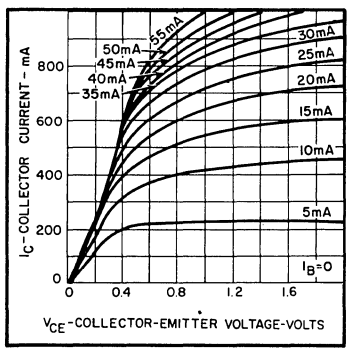


$T_A = 100°C$

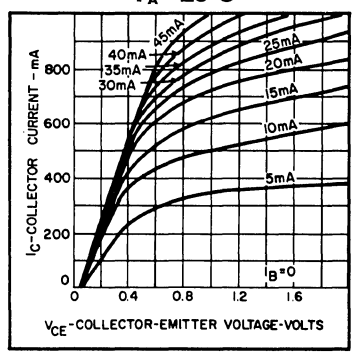


Collector Current vs. Collector Voltage, High Base Current

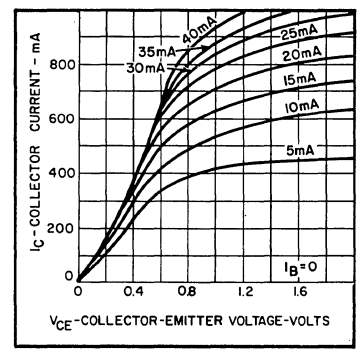
$T_A = -55°C$



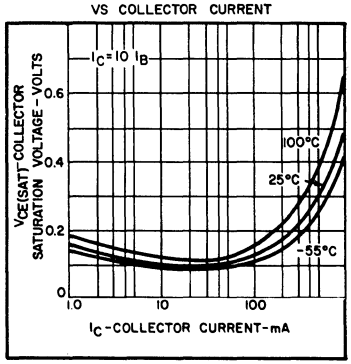
$T_A = 25°C$



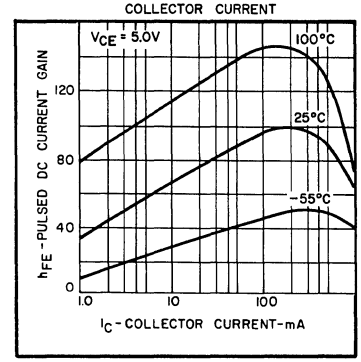
$T_A = 100°C$



COLLECTOR SATURATION VOLTAGE VS COLLECTOR CURRENT



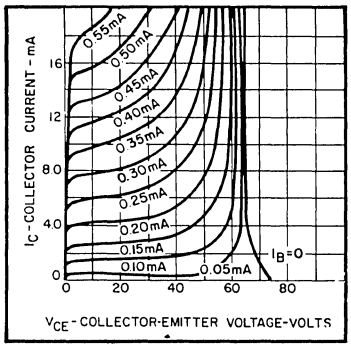
PULSED DC CURRENT GAIN VS COLLECTOR CURRENT



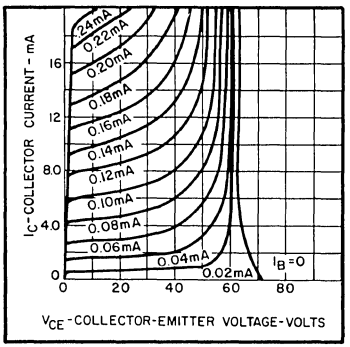
COLLECTOR CHARACTERISTICS 2N3725 2N4014

Collector Current vs. Collector Voltage, Low Base Current

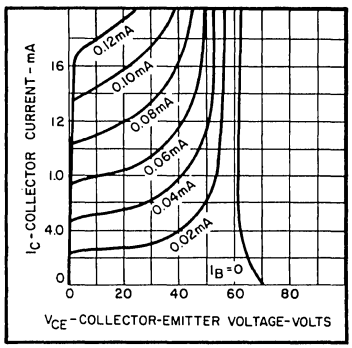
$T_A = -55°C$



$T_A = 25°C$

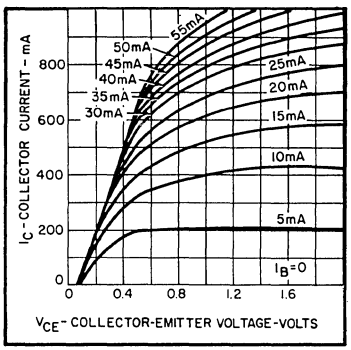


$T_A = 100°C$

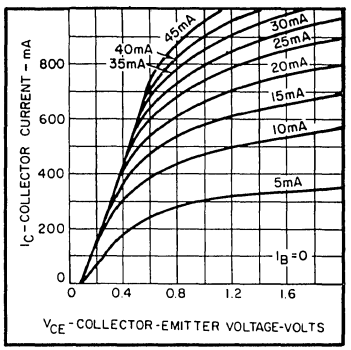


Collector Current vs. Collector Voltage, High Base Current

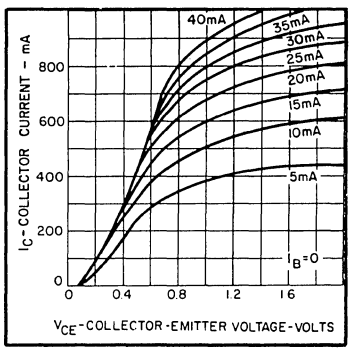
$T_A = -55°C$



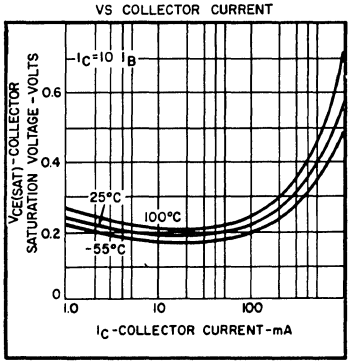
$T_A = 25°C$



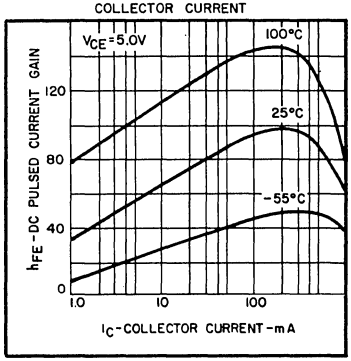
$T_A = 100°C$



COLLECTOR SATURATION VOLTAGE VS COLLECTOR CURRENT



PULSED DC CURRENT GAIN VS COLLECTOR CURRENT



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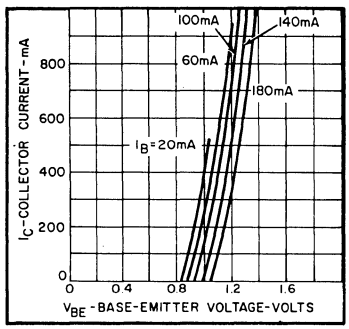
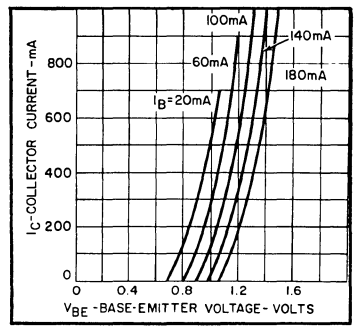
COLLECTOR CHARACTERISTICS 2N3724 2N3725 2N4013 2N4014

Collector Current vs. Base-Emitter Voltage

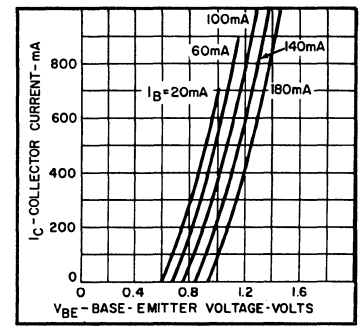
$T_A = -55°C$



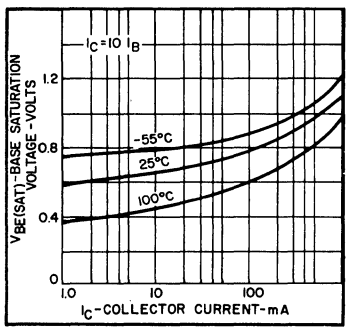
$T_A = 25°C$



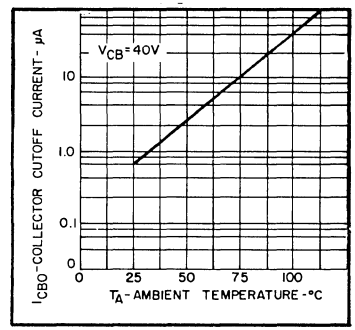
$T_A = 100°C$



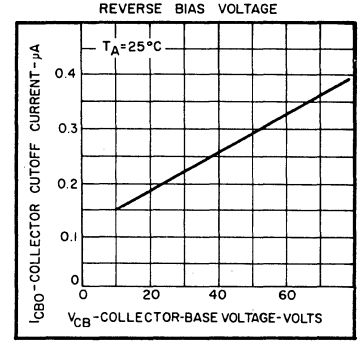
BASE SATURATION VOLTAGE VS COLLECTOR CURRENT



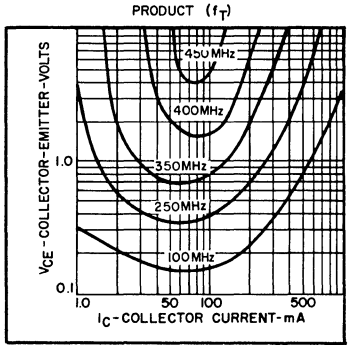
COLLECTOR CUTOFF CURRENT VS AMBIENT TEMPERATURE



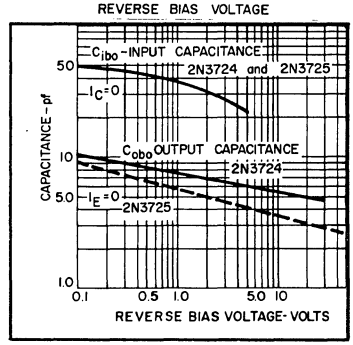
COLLECTOR CUTOFF CURRENT VS REVERSE BIAS VOLTAGE



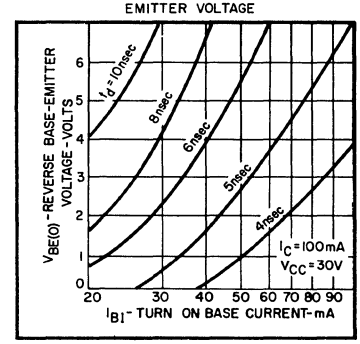
CONTOURS OF CONSTANT BANDWIDTH PRODUCT (f_T)



INPUT AND OUTPUT CAPACITANCE VS REVERSE BIAS VOLTAGE



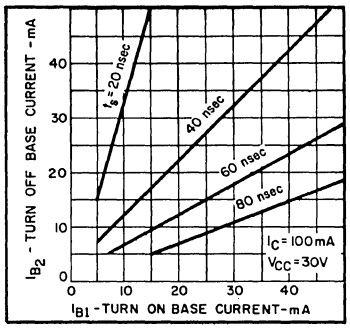
DELAY TIME VS TURN ON BASE CURRENT AND REVERSE BASE-EMITTER VOLTAGE



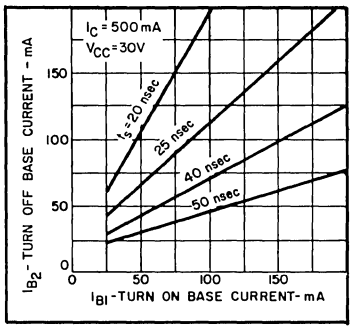
5

SWITCHING CHARACTERISTICS 2N3724 2N3725 2N4013 2N4014

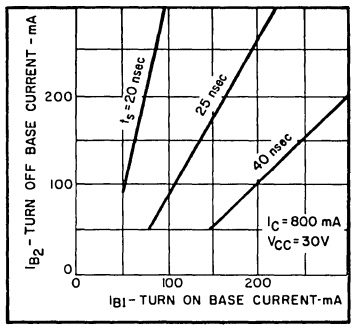
STORAGE TIME VS TURN ON AND TURN OFF BASE CURRENTS



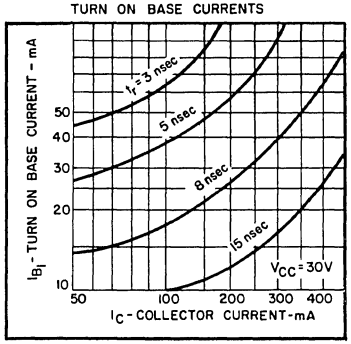
STORAGE TIME VS TURN ON AND TURN OFF BASE CURRENTS



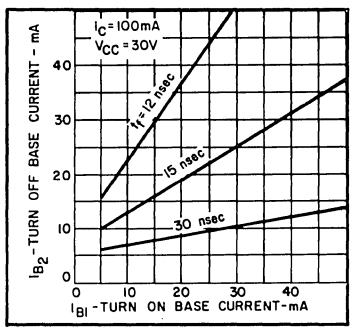
STORAGE TIME VS TURN ON AND TURN OFF BASE CURRENTS



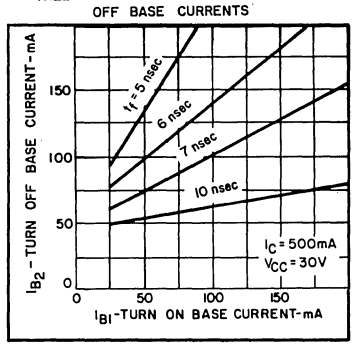
RISE TIME VS COLLECTOR AND TURN ON BASE CURRENTS



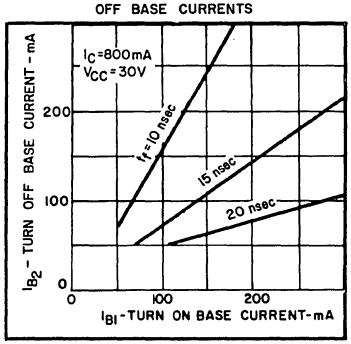
FALL TIME VS TURN ON AND TURN OFF BASE CURRENTS



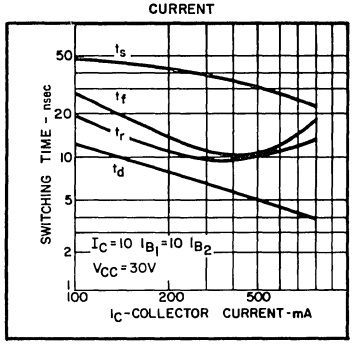
FALL TIME VS TURN ON AND TURN OFF BASE CURRENTS



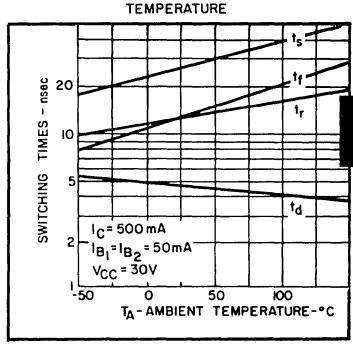
FALL TIME VS TURN ON AND TURN OFF BASE CURRENTS



SWITCHING TIMES VS COLLECTOR CURRENT



SWITCHING TIMES VS AMBIENT TEMPERATURE



2N3734, 2N3736Ⓕ

NPN SILICON HIGH VOLTAGE, HIGH CURRENT SWITCHING TRANSISTORS

Packages:
2N3734, TO-5
2N3736, TO-46

The ITT 2N3734 and 2N3736 are high voltage, high current NPN diffused silicon planar epitaxial transistors useful for memory applications requiring breakdown voltages up to 50 volts and high current capacity with Beta specified to 1.5 amperes.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Characteristics	Unit
Storage Temperature	−65°C to +200°C
Operating Junction Temperature	+200°C Maximum
Lead Temperature (Soldering, 10 sec Time Limit)	+230°C Maximum
Total Device Dissipation @:	
T_C = 25°C (2N3734)	4.0 Watts
(2N3736)	2.0 Watts
T_A = 25°C (2N3734)	1.0 Watt
(2N3736)	0.5 Watt
Collector-Base Voltage	50 Volts
Collector-Emitter Voltage (Note 4)	30 Volts
Emitter-Base Voltage	5.0 Volts
Collector Current	1.5 Amps

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Min	Max	Unit	Conditions
$V_{CEO(sust)}$	30	–	Volts	I_C = 10 mA (pulsed), I_B = 0 (Notes 4 and 5)
$V_{CE(sat)}$	–	0.9	Volt	I_C = 1.0 A, I_B = 100 mA (Note 5)
$V_{CE(sat)}$	–	0.5	Volt	I_C = 500 mA, I_B = 50 mA (Note 5)
t_d	–	8.0	nsec	I_C = 1.0 A, I_{B1} = 100 mA (see Fig. 1)
t_r	–	40	nsec	I_C = 1.0 A, I_{B1} = 100 mA (see Fig. 1)
t_s	–	30	nsec	I_C = 1.0 A, I_{B1} = 100 mA, I_{B2} = −100 mA (see Fig. 2)
t_f	–	30	nsec	I_C = 1.0 A, I_{B1} = 100 mA, I_{B2} = −100 mA (see Fig. 2)
h_{fe}	3.0	–	–	I_C = 50 mA, V_{CE} = 10 Volts
C_{obo}	–	9.0	pf	I_E = 0, V_{CB} = 10 Volts

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Min	Max	Unit	Conditions
C_{ibo}	–	80	pf	I_C = 0, V_{BE} = 0.5 Volt
h_{FE}	40	–	Volts	I_C = 150 mA, V_{CE} = 1.0 Volt (Note 5)
h_{FE}	35	–	Volts	I_C = 10 mA, V_{CE} = 1.0 Volt (Note 5)
h_{FE}	35	–	Volts	I_C = 500 mA, V_{CE} = 1.0 Volt (Note 5)
h_{FE}	30	120	Volts	I_C = 1.0 A, V_{CE} = 1.5 Volts (Note 5)
h_{FE}	30	–	Volts	I_C = 1.5 A, V_{CE} = 5.0 Volts (Note 5)
$V_{CE(sat)}$	–	0.2	Volt	I_C = 10 mA, I_B = 1.0 mA (Note 5)
$V_{CE(sat)}$	–	0.3	Volt	I_C = 150 mA, I_B = 15 mA (Note 5)
$V_{BE(sat)}$	–	0.8	Volt	I_C = 10 mA, I_B = 1.0 mA (Note 5)
$V_{BE(sat)}$	–	1.0	Volt	I_C = 150 mA, I_B = 15 mA (Note 5)
$V_{BE(sat)}$	–	1.2	Volts	I_C = 500 mA, I_B = 50 mA (Note 5)
$V_{BE(sat)}$	0.9	1.4	Volts	I_C = 1.0 A, I_B = 100 mA (Note 5)
I_{CEX}	–	0.2	μA	V_{CE} = 25 Volts, V_{EB} = 2.0 Volts
I_{CEX}(100°C)	–	20	μA	V_{CE} = 25 Volts, V_{EB} = 2.0 Volts
I_{BL}	–	0.3	μA	V_{CE} = 25 Volts, V_{EB} = 2.0 Volts
BV_{CBO}	50	–	Volts	I_C = 10μA, I_E = 0
BV_{EBO}	5.0	–	Volts	I_C = 0, I_E = 10 uA
Q_T	–	10	ncoul	I_C = 1.0 A, I_B = 100 mA V_{CC} = 30 Volts

NOTES:

(1) These ratings are limiting values above which the serviceability of any individual semiconductor device may be impaired.

(2) These are steady state limits. The factory should be consulted on applications involving pulsed or low duty cycle operations.

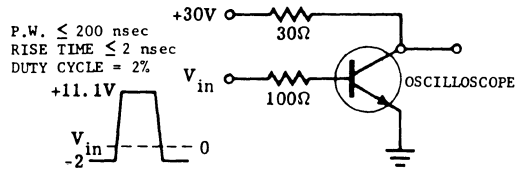
(3) These ratings give a maximum junction temperature of 200°C and junction-to-case thermal resistance of 43.8°C/watt (derating factor of 22.8 mW/°C) for the 2N3734; and 87.5°C/watt (derating factor of 11.4 mW/°C) for the 2N3736, junction-to-ambient thermal resistance of 175°C/watt (derating factor of 5.71 mW/°C) for the 2N3734; and 350°C/watt (derating factor of 2.86 mW/°C) for the 2N3736.

(4) Ratings refer to a high-current point where collector-to-emitter voltage is lowest.

(5) Pulse Conditions: length = 300μsec; duty cycle = 1%.

CIRCUIT DIAGRAM

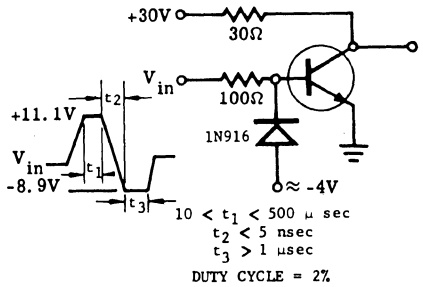
FIGURE 1



Z_{in} > 100 Kohm
C_{in} ≤ 12 pf
Rise time ≤ 5 nsec

T_{on} Circuit

FIGURE 2



Z_{in} > 100 Kohm
C_{in} ≤ 12 pf
Rise time ≤ 5 nsec

T_{off} Circuit

Package: TO-5

NPN SILICON HIGH-VOLTAGE, HIGH-CURRENT SWITCHING TRANSISTORS

The ITT 2N4046 and 2N4047 are high-voltage, high-current transistors useful for memory applications requiring breakdown voltages up to 50 volts and operating currents up to one ampere. Fast turn-on and turn-off times are assured because of the high minimum f_T (250 Mc) and tight control on storage time.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Characteristics	Unit
Collector-Base Voltage	
(2N4046)	50 Volts
(2N4047)	80 Volts
Collector-Emitter Voltage	
(2N4046)	50 Volts
(2N4047)	80 Volts
Collector-Emitter Voltage (Note 4)	
(2N4046)	30 Volts
(2N4047)	50 Volts
Emitter-Base Voltage	6.0 Volts
Maximum Collector Current	500 mA
Total Device Dissipation @:	
T_C = 25°C (Notes 2 and 3)	3.5 Watts
T_A = 25°C (Notes 2 and 3)	0.8 Watt
Storage Temperature	−65°C to +200 °C
Operating Junction Temperature	+200°C Maximum
Lead Temperature	
(Soldering, 60 sec Time Limit)	+300°C Maximum

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol		Min	Typ	Max	Unit	Conditions
$V_{CEO(sust)}$	2N4046	30	-	-	Volts	I_C = 10 mA (pulsed), I_B = 0
	2N4047	50	-	-	Volts	(Notes 4 and 5)
$V_{CE(sat)}$	2N4046	-	0.5	0.75	Volt	I_C = 1000 mA (pulsed), I_B = 100 mA
	2N4047	-	0.6	0.95	Volt	(Note 5)
$V_{CE(sat)}$	2N4046	-	0.3	0.42	Volt	I_C = 500 mA (pulsed), I_B = 50 mA
	2N4047	-	0.4	0.52	Volt	(Note 5)
t_{on}	2N4046, 2N4047	-	18	35	nsec	$I_C \approx$ 500 mA, $I_{B1} \approx$ 50 mA (Note 6)
t_{off}	2N4046, 2N4047	-	45	60	nsec	$I_C \approx$ 500 mA, $I_{B1} \approx$ 50 mA (Note 6) $I_{B2} \sim -50$ mA
h_{fe}	2N4046, 2N4047	2.5	4.5	-	-	I_C = 50 mA, V_{CE} = 10 Volts

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol		Min	Typ	Max	Unit	Conditions
C_{obo}	2N4046	-	6.0	12	pf	I_E = 0, V_{CB} = 10 Volts
	2N4047	-	4.8	10	pf	
C_{ibo}	2N4046, 2N4047	-	40	55	pf	I_C = 0, V_{EB} = 0.5 volt
h_{FE}	2N4046, 2N4047	40	90	150	-	I_C = 100 mA, V_{CE} = 1.0 Volt (Note 5)
h_{FE}	2N4046	30	50	-	-	I_C = 500 mA, V_{CE} = 1.0 Volt
	2N4047	20	45	-	-	(Note 5)
h_{FE}	2N4046	30	65	-	-	I_C = 300 mA, V_{CE} = 1.0 Volt
	2N4047	30	60	-	-	(Note 5)
h_{FE}	2N4046	25	65	-	-	I_C = 1000 mA, V_{CE} = 5.0 Volts
	2N4047	15	65	-	-	(Note 5)
h_{FE}	2N4046, 2N4047	20	60	-	-	I_C = 10 mA, V_{CE} = 1.0 Volt (Note 5)
h_{FE}	2N4046	20	45	-	-	I_C = 800 mA, V_{CE} = 2.0 Volts
	2N4047	15	40	-	-	(Note 5)
$V_{CE(sat)}$	2N4046	-	0.11	0.25	Volt	I_C = 10 mA, I_B = 1.0 mA
	2N4047	-	0.19	0.25	Volt	(Note 5)
$V_{CE(sat)}$	2N4046	-	0.13	0.2	Volt	I_C = 100 mA, I_B = 10 mA
	2N4047	-	0.21	0.26	Volt	(Note 5)
$V_{CE(sat)}$	2N4046	-	0.22	0.32	Volt	I_C = 300 mA, I_B = 30 mA
	2N4047	-	0.31	0.4	Volt	(Note 5)
$V_{CE(sat)}$	2N4046	-	0.4	0.65	Volt	I_C = 800 mA, I_B = 80 mA
	2N4047	-	0.5	0.8	Volt	(Note 5)
$V_{BE(sat)}$	2N4046, 2N4047	-	0.64	0.76	Volt	I_C = 10 mA, I_B = 1.0 mA (Note 5)
$V_{BE(sat)}$	2N4046, 2N4047	-	0.75	0.86	Volt	I_C = 100 mA, I_B = 10 mA (Note 5)
$V_{BE(sat)}$	2N4046, 2N4047	-	0.89	1.1	Volts	I_C = 300 mA, I_B = 30 mA (Note 5)
$V_{BE(sat)}$	2N4046, 2N4047	0.9	0.95	1.2	Volts	I_C = 500 mA, I_B = 50 mA (Note 5)
$V_{BE(sat)}$	2N4046, 2N4047	-	1.0	1.5	Volts	I_C = 800 mA, I_B = 80 mA (Note 5)
$V_{BE(sat)}$	2N4046, 2N4047	-	1.1	1.7	Volts	I_C = 1000 mA, I_B = 100 mA (Note 5)
I_{CBO}	2N4046	-	0.25	1.7	μA	I_E = 0, V_{CB} = 40 Volts
I_{CBO}	2N4047	-	0.33	1.7	μA	I_E = 0, V_{CB} = 60 Volts
I_{CBO}(+85°C)	2N4046	-	25	120	μA	I_E = 0, V_{CB} = 40 Volts

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol		Min	Typ	Max	Unit	Conditions
I_{CBO}(+85°C)	2N4047	-	25	120	μA	I_E = 0, V_{CB} = 60 Volts
BV_{CBO}	2N4046	50	-	-	Volts	I_C = 10 μA, I_E = 0
	2N4047	80	-	-	Volts	
BV_{CES}	2N4046	50	-	-	Volts	I_C = 10 μA, V_{BE} = 0
	2N4047	80	-	-	Volts	
BV_{EBO}	2N4046, 2N4047	6 0	-	-	Volts	I_C = 0, I_E = 10 μA

NOTES:

(1) These ratings are limiting values above which the serviceability of any individual semiconductor device may be impaired

(2) These are steady state limits The factory should be consulted on applications involving pulsed or low duty cycle operations

(3) These ratings give a maximum junction temperature of 200°C and junction-to-case thermal resistance of 50°C/watt (derating factor of 20 mW/°C) Junction-to-ambient thermal resistance of 219°C/watt (derating factor of 4 56 mW/°C)

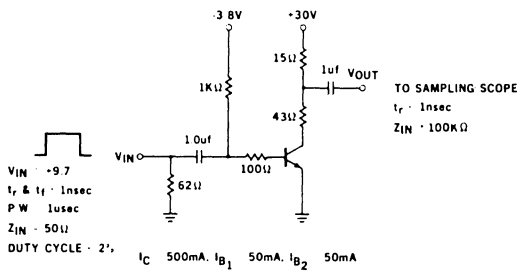
(4) Ratings refer to a high-current point where collector-to-emitter voltage is lowest

(5) Pulse Conditions length = 300μsec. duty cycle = 1%

(6) See switching circuit for exact value of I_C, I_{B1}, and I_{B2}

SCHEMATIC

FIGURE 1 – SWITCHING TIME TEST CIRCUIT



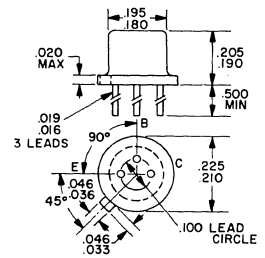
HIGH-SPEED NPN SILICON PLANAR EPITAXIAL SATURATED SWITCHING TRANSISTOR

For Improved Performance See ITT 2N2368.

ABSOLUTE MAXIMUM RATINGS

CHARACTERISTICS		UNITS
Collector-to-Base Voltage	25	Volts
Collector-to-Emitter Voltage	15	Volts
Emitter-to-Base Voltage	3	Volts
Operating Junction Temperature	200	°C
Storage Temperature	−65 to +200	°C
P_D @ T_C = 25°C	1.0	Watt
P_D @ T_A = 25°C	0.3	Watt

DIMENSIONS



TO-18

ELECTRICAL CHARACTERISTICS (25C° free air unless otherwise noted)

SYMBOL	MIN.	MAX.	UNIT	CONDITIONS
BV_{CBO}	25		Vdc	I_C=1.0μA
V_{CER}	20		Vdc	I_C=30mA, R_{BE}=10Ω pulsed
BV_{EBO}	3		Vdc	I_E=10μA
h_{FE}	20			I_C=10mA, V_{CE}=1.0V
V_{CE}(sat)		0.6	Vdc	I_C=10mA, I_B=1.0mA
V_{BE}(sat)		0.9	Vdc	I_C=10mA, I_B=1.0mA
I_{CBO}		50	nA	V_{CB}=15V
I_{CBO}		30	μA	V_{CB}=15V, T_A=+150°C
C_{ob}		6.0	pF	V_{CB}=10V
h_{fe}	2			I_C=10mA, V_{CE}=15V, f=100MHz
t_{pd}	5	11	ns	I_C=4.5mA
t_s		60	ns	I_C=I_{B1}=I_{B2}=10mA, V_{CC}=10V, R_L=1KΩ

NOTE: Pulse width ≤ 300 μsec, duty cycle ≤ 2%.

ELECTRICAL CHARACTERISTICS (25°C free air unless otherwise noted)

SYMBOL	MIN.	MAX.	UNIT	CONDITIONS
BV_{CBO}	25		Vdc	$I_C=10\mu A$
LV_{CER}	20		Vdc	$I_C=10mA$, $R_{BE}=10\Omega$ pulsed
BV_{EBO}	5		Vdc	$I_E=10\mu A$
h_{FE}	20			$I_C=10mA$, $V_{CE}=1V$
$V_{CE}(sat)$		0.6	Vdc	$I_C=10mA$, $I_B=1mA$
$V_{BE}(sat)$	0.7	0.9	Vdc	$I_C=10mA$, $I_B=1mA$
I_{CBO}		0.5	μA	$V_{CB}=15V$
I_{CBO}		30	μA	$V_{CB}=15V$, $T_A=150°C$
C_{ob}		5	pF	$V_{CB}=5V$
h_{fe}	2			$I_C=10mA$, $V_{CE}=10V$, $f=100MHz$
t_s		25	ns	$I_C=I_{B1}=I_{B2}=10mA$, $V_{CC}=10V$, $R_L=1K\Omega$
t_{on}		40	ns	$I_{B1}=3mA$, $I_{B2}=1mA$, $V_{CC}=3V$, $R_L=270\Omega$
t_{off}		75	ns	$I_{B1}=3mA$, $I_{B2}=1mA$, $V_{CC}=3V$, $R_L=270\Omega$

ELECTRICAL CHARACTERISTICS (25°C free air unless otherwise noted)

SYMBOL	MIN.	MAX.	UNIT	CONDITIONS
BV_{CBO}	25		Vdc	$I_C=10\mu A$
LV_{CER}	20		Vdc	$I_C=10mA$, $R_{BE}=10\Omega$ pulsed
LV_{CEO}	15		Vdc	$I_C=10mA$ pulsed
BV_{EBO}	5		Vdc	$I_E=10\mu A$
h_{FE}	20	60		$I_C=10mA$, $V_{CE}=IV$
$V_{CE}(sat)$		0.4	Vdc	$I_C=10mA$, $I_B=1mA$
$V_{BE}(sat)$	0.7	0.9	Vdc	$I_C=10mA$, $I_B=1mA$
I_{CBO}		0.5	μA	$V_{CB}=15V$
I_{CBO}		30	μA	$V_{CB}=15V$, $T_A=150°C$
I_{CER}		10	μA	$V_{CE}=20V$, $R_{BE}=100K$
C_{ob}		5	pF	$V_{CB}=5V$
h_{fe}	2.0			$I_C=10mA$, $V_{CE}=10V$, $f=100MHz$
r_b'		50	ohms	$I_C=10mA$, $V_{CE}=15V$, $f=300MHz$
τ_s		25	ns	$I_C=I_{B1}=I_{B2}=10mA$, $V_{CC}=10V$, $R_L=1K\Omega$
t_{on}		40	ns	$I_{B1}=3mA$, $I_{B2}=1mA$, $V_{CC}=3V$, $R_L=270\Omega$
t_{off}		75	ns	$I_{B1}=3mA$, $I_{B2}=1mA$, $V_{CC}=3V$, $R_L=270\Omega$

NOTE: Pulse width $\leq$ 300 μsec, duty cycle $\leq$ 2%.

2N708®

SILICON SWITCHING TRANSISTOR

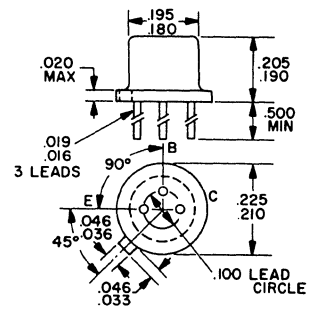
HIGH-SPEED NPN SILICON PLANAR EPITAXIAL SATURATED SWITCHING TRANSISTOR

For Improved Performance See ITT 2N2369A.

ABSOLUTE MAXIMUM RATINGS

CHARACTERISTICS		UNITS
Collector-to-Base Voltage	40	Volts
Collector-to-Emitter Voltage	15	Volts
Emitter-to-Base Voltage	5	Volts
Operating Junction Temperature	200	°C
Storage Temperature	−65 to +200	°C
P_D @ T_C = 25°C	1.2	Watts
P_D @ T_A = 25°C	.36	Watt

DIMENSIONS
(IN INCHES)



TO-18

ELECTRICAL CHARACTERISTICS (25°C free air unless otherwise noted)

SYMBOL	MIN.	MAX.	UNIT	CONDITIONS
BV_{CBO}	40		Vdc	I_C=1μA
LV_{CER}	20		Vdc	I_C=3mA pulsed, R_{BE}=10Ω
LV_{CEO}	15		Vdc	I_C=30mA pulsed
BV_{EBO}	5		Vdc	I_E=10μA
h_{FE}	30	120		I_C=10mA, V_{CE}=1V
h_{FE}	15			I_C=0.5mA, V_{CE}=1V, T_A=−55°C
h_{FE}	15			I_C=10mA, V_{CE}=1V
V_{CE}(sat)		.40	Vdc	I_C=10mA, I_B=1.0mA
V_{CE}(sat)		.40	Vdc	I_C=7mA, I_B=.7mA, T_A=+125°C
V_{BE}(sat)	.72	.80	Vdc	I_C=10mA, I_B=1.0mA
V_{BE}(sat)		.90	Vdc	I_C=10mA, I_B=1.0mA, T_A=−55°C
I_{CBO}		25	nA	V_{CB}=20V
I_{CBO}		15	μA	V_{CB}=20V, T_A=+150°C
I_{EBO}		0.1	μA	V_{EB}=4V
I_{CEX}		10	μA	V_{CE}=20V, V_{EB}=.25V, T_A=125°C
C_{ob}		6	pF	V_{CB}=10V
h_{fe}	3			I_C=10mA, V_{CE}=10V, f=100MHz
r_b'		50	ohms	I_C=10mA, V_{CE}=10V, f=300MHz
τ_s		25	ns	I_C=I_{B1}=I_{B2}=10mA
t_{on}		40	ns	I_C=10mA, I_{B1}=3mA, V_{EB}=2V
t_{off}		75	ns	I_C=10mA, I_{B1}=3mA, I_{B2}=1mA

NOTE: Pulse width ≤ 300 μsec, duty cycle ≤ 2%.

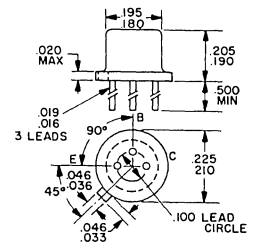
HIGH SPEED NPN SILICON PLANAR EPITAXIAL SATURATED SWITCHING TRANSISTOR

For Improved Performance See ITT 2N2369

ABSOLUTE MAXIMUM RATINGS

CHARACTERISTICS		UNITS
Collector-to-Base Voltage	20	Volts
Collector-to-Emitter Voltage	12	Volts
Emitter-to-Base Voltage	5	Volts
Operating Junction Temperature	200	°C
Storage Temperature	−65 to +200	°C
P_D @ T_C = 25°C	1.0	Watt
P_D @ T_A = 25°C	0.3	Watt

DIMENSIONS



TO-18

ELECTRICAL CHARACTERISTICS (25°C free air unless otherwise noted)

SYMBOL	MIN.	MAX.	UNIT	CONDITIONS
BV_{CBO}	20		Vdc	I_C=1μA
LV_{CEO}	12		Vdc	I_C=10mA pulsed
BV_{EBO}	5		Vdc	I_C=10μA
h_{FE}	20			I_C=1.0mA, V_{CE}=0.25V
h_{FE}	40	120		I_C=10mA, V_{CE}=0.35V
h_{FE}	20			I_C=100mA, V_{CE}=1.0V pulsed
h_{FE}	20			I_C=10mA, V_{CE}=0.35V, T_A= −55°C
V_{CE}(sat)	0.35		Vdc	I_C=10mA, I_B=1mA, T_A=170°C
V_{CE}(sat)	1		Vdc	I_C=100mA, I_B=10mA, T_A=170°C pulsed
V_{BE}(sat)	0.65	0.85	Vdc	I_C=10mA, I_B=1mA
V_{BE}(sat)		1.5	Vdc	I_C=100mA, I_B=10mA pulsed
V_{BE}(sat)		1.1	Vdc	I_C=10mA, I_B=1mA, T_A= −55°C
V_{BE}(sat)		1.6	Vdc	I_C=100mA, I_B=10mA, T_A= −55°C pulsed
I_{CBO}		1	μA	V_{CB}=20V
I_{CEO}		30	μA	V_{CE}=10V, V_{BE}=0.35V, T_A=100°C
I_{CES}		1	μA	V_{CE}=20V
I_{CES}		100	μA	V_{CE}=20V, T_A=170°C
C_{ob}		5	pF	V_{CB}=5V
h_{fe}	2.8			I_C=10mA, V_{CE}=10V, f=100MHz
T_s		18	ns	I_C=I_{B1}=I_{B2}=10mA
t_{on}		12	ns	I_C=100mA, I_{B1}=40mA, I_{B2}=20mA
t_{on}		16	ns	I_C=10mA, I_{B1}=3mA, I_{B2}=1.5mA
t_{off}		45	ns	I_C=100mA, I_{B1}=40mA, I_{B2}=20mA
t_{off}		24	ns	I_C=10mA, I_{B1}=3mA, I_{B2}=1.5mA

NOTE: Pulse width ≤ 300μsec, duty cycle ≤ 2%.

2N753®

SILICON SWITCHING TRANSISTOR

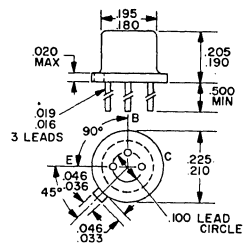
HIGH-SPEED NPN SILICON PLANAR EPITAXIAL SATURATED SWITCHING TRANSISTOR

For Improved Performance See ITT 2N2369.

ABSOLUTE MAXIMUM RATINGS

CHARACTERISTICS		UNITS
Collector-to-Base Voltage	25	Volts
Collector-to-Emitter Voltage	15	Volts
Emitter-to-Base Voltage	5	Volts
Operating Junction Temperature	175	°C
Storage Temperature	−65 to +200	°C
P_D @ T_C = 25°C	1.0	Watt
P_D @ T_A = 25°C	0.3	Watt

DIMENSIONS



TO-18

ELECTRICAL CHARACTERISTICS (25°C free air unless otherwise noted)

SYMBOL	MIN.	MAX.	UNIT	CONDITIONS
BV_{CBO}	25		Vdc	I_C=10μA
LV_{CER}	20		Vdc	I_C=10mA, R_{BE}=10Ω pulsed
LV_{CEO}	15		Vdc	I_C=10mA pulsed
BV_{EBO}	5		Vdc	I_C=10μA
h_{FE}	40	120		I_C=10mA, V_{CE}=1.0V
V_{CE}(sat)		0.6	Vdc	I_C=10mA, I_B=1.0mA
V_{BE}(sat)	0.7	0.9	Vdc	I_C=10mA, I_B=1.0mA
I_{CBO}		0.5	μA	V_{CB}=15V
I_{CBO}		30	μA	V_{CB}=15V, T_A=150°C
I_{CER}		10	μA	V_{CE}=20V, R_{BE}=100KΩ
C_{ob}	5		pF	V_{CB}=5V
h_{fe}	2			I_C=10mA, V_{CE}=10V, f=100MHz
τ_s		35	ns	I_C=10mA, I_{B1}=I_{B2}=10mA, V_{CC}=10V
t_{on}		40	ns	V_{CC}=3V, R_L=270Ω, I_{B1}=3mA
t_{off}		75	ns	V_{CC}=3V, R_L=270Ω, I_{B1}=3mA, I_{B2}=1mA

NOTES: Pulse width ≤ 300μsec, duty cycle ≤ 2%.

2N783Ⓔ
HIGH-SPEED NPN SILICON SWITCHING TRANSISTOR

ABSOLUTE MAXIMUM RATINGS (Note 1)

Characteristics	Unit
Storage Temperature	−65°C to +300°C
Operating Junction Temperature	175°C Maximum
Total Device Dissipation	
@ T_C = 25°C (Notes 2 and 3)	1.0 Watt
@ T_A = 25°C (Notes 2 and 3)	0.3 Watt
Collector-Base Voltage	40 Volts
Collector-Emitter Voltage (R_{BE} = 10Ω)	20 Volts
Emitter-Base Voltage	5.0 Volts
Collector Current	200 mA

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Min	Max	Unit	Conditions
h_{FE}	20	60	-	I_C = 10 mA, V_{CE} = 1.0 Volt
$V_{CE(sat)}$	-	0.25	Volt	I_C = 10 mA, I_B = 1.0 mA
$V_{BE(sat)}$	0.7	0.9	Volt	I_C = 10 mA, I_B = 1.0 mA
I_{CBO}	-	250	nA	I_E = 0, V_{CB} = 25 Volts
I_{CBO}(150°C)	-	30	μA	I_E = 0, V_{CB} = 25 Volts
h_{fe}	2.0	-	-	I_C = 10 mA, V_{CE} = 10 Volts
C_{ob}	-	3.5	pf	I_E = 0, V_{CB} = 10 Volts
t_s	-	10	nsec	I_C = 10 mA, V_{CC} = 10 Volts (Note 4)
t_{on}	-	16	nsec	I_{B1} = 3.0 mA, I_{B2} = 1.0 mA (Note 5)
t_{off}	-	30	nsec	I_{B1} = 3.0 mA, I_{B2} = 1.0 mA (Note 5)
BV_{CBO}	40	-	Volts	I_E = 0, I_C = 100 μA
BV_{CER}	20	-	Volts	I_C = 1.0 mA, V_{BE} = 0
BV_{EBO}	5.0	-	Volts	I_C = 0, I_E = 100 μA

NOTES:

(1) These ratings are limiting values above which the serviceability of any individual semiconductor device may be impaired

(2) These are steady state limits. The factory should be consulted on applications involving pulsed or low duty cycle operations

(3) These ratings give a maximum junction temperature of 175°C and junction-to-case thermal resistance of 150°C/Watt (derating factor of 6.67 mW/°C), junction-to-ambient thermal resistance of 500°C/Watt (derating factor of 2.0 mW/°C)

(4) I_{B1} = 10 mA, I_{B2} = 10 mA, R_L = 1KΩ, (see Figure 2).

(5) V_{CC} = 3.0 Volts, R_L = 270 Ω, (see Figure 1).

CIRCUIT DIAGRAM

FIGURE 1 TURN-ON AND TURN-OFF CIRCUIT

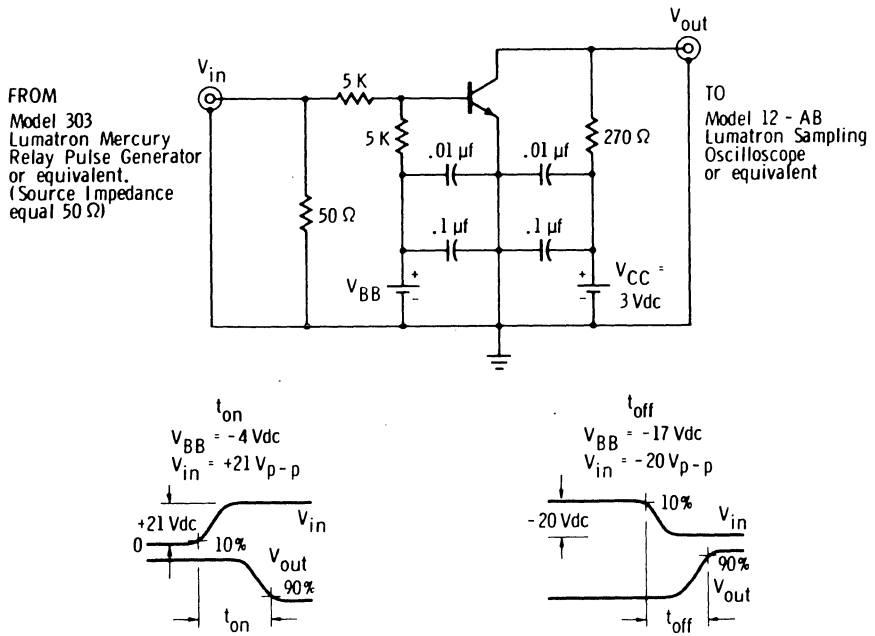
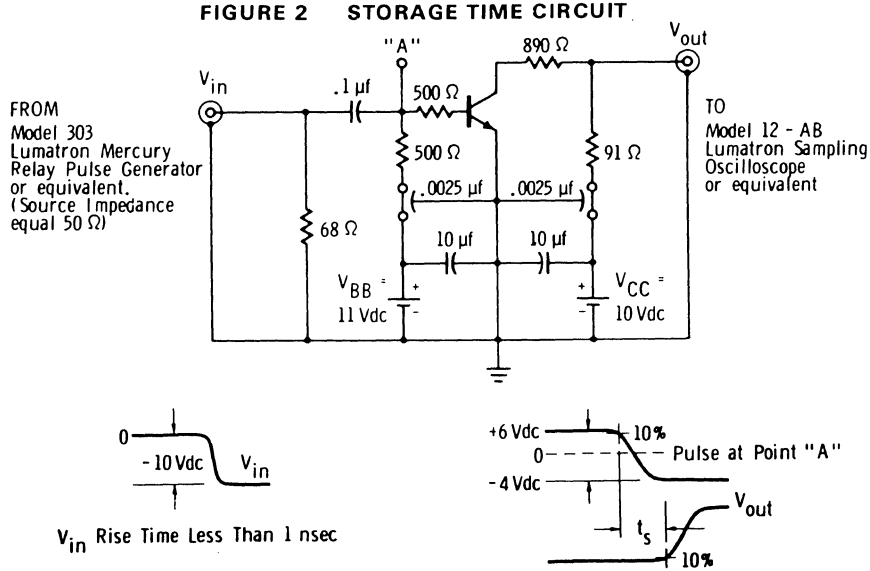


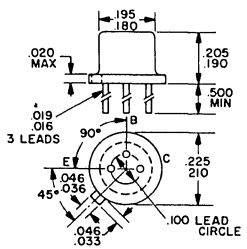
FIGURE 2 STORAGE TIME CIRCUIT



HIGH-SPEED NPN SILICON PLANAR EPITAXIAL SATURATED SWITCHING TRANSISTOR

For Improved Performance See ITT 2N2368.

DIMENSIONS



TO-18

ABSOLUTE MAXIMUM RATINGS

CHARACTERISTICS		UNITS
Collector-to-Base Voltage	30	Volts
Collector-to-Emitter Voltage	12	Volts
Emitter-to-Base Voltage	5	Volts
Operating Junction Temperature	175	°C
Storage Temperature	−65 to +200	°C
P_D @ T_C = 25°C	1.0	Watt
P_D @ T_A = 25°C	0.3	Watt

ELECTRICAL CHARACTERISTICS (25°C free air unless otherwise noted)

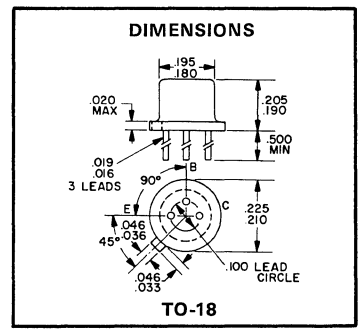
SYMBOL	MIN.	MAX.	UNIT	CONDITIONS
BV_{CBO}	30		Vdc	I_C = 100μA
BV_{CER}	15		Vdc	I_C = 10μA, R_{BE} = 10Ω
BV_{EBO}	5		Vdc	I_C = 100μA
h_{FE}	25			I_C = 10mA, V_{CE} = 10V
V_{CE}(sat)		0.19	Vdc	I_C = 10mA, I_B = 1mA
V_{BE}(sat)	0.7	0.9	Vdc	I_C = 10mA, I_B = 1mA
I_{CBO}		250	nA	V_{CB} = 25V
I_{CBO}		30	μA	V_{CB} = 25V, T_A = 150°C
C_{ob}		3.5	pF	V_{CB} = 10V
h_{fe}	2			I_C = 10mA, V_{CE} = 10V, f = 100MHz
t_s		15	ns	I_C = I_{B1} = I_{B2} = 10mA, V_{CC} = 10V, R_L = 1KΩ
t_{on}		20	ns	I_{B1} = 3mA, I_{B2} = 1mA, V_{CC} = 3V, R_L = 270Ω
t_{off}		40	ns	I_{B1} = 3mA, I_{B2} = 1mA, V_{CC} = 3V, R_L = 270Ω

2N834©

SILICON SWITCHING TRANSISTOR

HIGH-SPEED NPN SILICON PLANAR EPITAXIAL SATURATED SWITCHING TRANSISTOR

For Improved Performance See ITT 2N2369.



ABSOLUTE MAXIMUM RATINGS

CHARACTERISTICS		UNITS
Collector-to-Base Voltage	40	Volts
Collector-to-Emitter Voltage	25	Volts
Emitter-to-Base Voltage	5	Volts
Operating Junction Temperature	175	°C
Storage Temperature	−65 to +200	°C
P_D @ T_C = 25°C	1.0	Watt
P_D @ T_A = 25°C	0.3	Watt

ELECTRICAL CHARACTERISTICS (25°C free air unless otherwise noted)

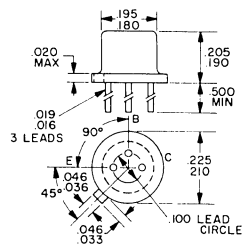
SYMBOL	MIN.	MAX.	UNIT	CONDITIONS
BV_{CBO}	40		Vdc	I_C = 100μA
BV_{CES}	30		Vdc	I_C = 10μA
BV_{EBO}	5		Vdc	I_E = 100μA
h_{FE}	25			I_C = 10mA, V_{CE} = 1.0V
V_{CE}(sat)		0.25	Vdc	I_C = 10mA, I_B = 1.0mA
V_{CE}(sat)		0.4	Vdc	I_C = 50mA, I_B = 5.0mA pulsed
V_{BE}(sat)		0.9	Vdc	I_C = 10mA, I_B = 1.0mA
I_{CBO}		0.5	μA	V_{CB} = 20V
I_{CBO}		30	μA	V_{CB} = 20V, T_A = 150°C
C_{ob}		4	pF	V_{CB} = 10V
h_{fe}	3.5			I_C = 10mA, V_{CE} = 15V, f = 100MHz
τ_s		25	ns	I_C = 10mA, I_{B1} = I_{B2} = 10mA
t_{on}		35	ns	I_C = 10mA, I_{B1} = 3mA, I_{B2} = 1mA
t_{off}		75	ns	I_C = 10mA, I_{B1} = 3mA, I_{B2} = 1mA

NOTE: Pulse width ≤ 300 μsec, duty cycle ≤ 2%.

HIGH-SPEED NPN SILICON PLANAR EPITAXIAL SATURATED SWITCHING TRANSISTOR

For Improved Performance See ITT 2N2369.

DIMENSIONS



TO-18

ABSOLUTE MAXIMUM RATINGS

CHARACTERISTICS		UNITS
Collector-to-Base Voltage	25	Volts
Collector-to-Emitter Voltage	15	Volts
Emitter-to-Base Voltage	3	Volts
Operating Junction Temperature	175	°C
Storage Temperature	−65 to +200	°C
P_D @ T_C = 25°C	1.0	Watts
P_D @ T_A = 25°C	0.3	Watts

ELECTRICAL CHARACTERISTICS (25°C free air unless otherwise noted)

SYMBOL	MIN.	MAX.	UNIT	CONDITIONS
BV_{CBO}	25		Vdc	I_C = 10μA
BV_{CES}	20		Vdc	I_C = 10μA
BV_{EBO}	3		Vdc	I_C = 10μA
h_{FE}	20			I_C = 10mA, V_{CE} = 1V
V_{CE}(sat)		0.3	Vdc	I_C = 10mA, I_B = 1mA
V_{BE}(sat)		0.9	Vdc	I_C = 10mA, I_B = 1mA
I_{CBO}		0.5	μA	V_{CB} = 20V
I_{CBO}		30	μA	V_{CB} = 20V, T_A = 150°C
C_{ob}		4	pF	V_{CB} = 10V
h_{fe}	3			I_C = 10mA, V_{CE} = 15V, f = 100MHz
τ_s		35	ns	I_C = 10mA, I_{B1} = I_{B2} = 10mA
t_{on}		20	ns	I_C = 10mA, I_{B1} = 3mA, I_{B2} = 1mA
t_{off}		35	ns	I_C = 10mA, I_{B1} = 3mA, I_{B2} = 1mA

Package: TO-18

2N914Ⓔ

NPN SILICON SATURATED SWITCH AND VHF AMPLIFIER

ABSOLUTE MAXIMUM RATINGS

Characteristics	Unit
Collector-Base Voltage	40 Volts
Collector-Emitter Voltage	
$R_{BE} \leq 10$ ohms (Note 4)	20 Volts
Collector-Emitter Voltage (Note 4)	15 Volts
Emitter-Base Voltage	5.0 Volts
Total Dissipation @ :	
$T_C = 25°C$ (Notes 2 and 3)	1.2 Watts
$T_C = 100°C$ (Notes 2 and 3)	0.68 Watt
$T_A = 25°C$ (Notes 2 and 3)	0.36 Watt
Storage Temperature	−65°C to +300°C
Operating Junction Temperature	200°C Maximum
Lead Temperature	
(Soldering, No Time Limit)	300°C Maximum

ELECTRICAL CHARACTERISTICS ($T_A = 25°C$ unless otherwise noted)

Symbol	Min	Typ	Max	Unit	Conditions
h_{FE}	30	55	120	–	$I_C = 10$ mA, $V_{CE} = 1.0$ Volt (Note 5)
$h_{FE(-55°C)}$	12	28	–	–	$I_C = 10$ mA, $V_{CE} = 1.0$ Volt (Note 5)
h_{FE}	10	17	–	–	$I_C = 500$ mA, $V_{CE} = 5.0$ Volts (Note 5)
$V_{BE(sat)}$	0.70	0.74	0.80	Volt	$I_C = 10$ mA, $I_B = 1.0$ mA
$V_{CE(sat)}$	–	0.40	0.70	Volt	$I_C = 200$ mA, $I_B = 20$ mA
$V_{CE(sat)}$	–	0.20	0.25	Volt	$I_C = 10\ I_B$ (Note 6)
h_{fe}	3.0	3.7	–	–	$I_C = 20$ mA, $V_{CE} = 10$ Volts
C_{obo}	–	4.5	6.0	pf	$I_E = 0$, $V_{CB} = 10$ Volts
C_{ibo}	–	–	9.0	pf	$I_C = 0$, $V_{EB} = 0.5$ Volt
I_{CBO}	–	4.0	25	mμA	$I_E = 0$, $V_{CB} = 20$ Volts
$I_{CBO(150°C)}$	–	3.0	15	μA	$I_E = 0$, $V_{CB} = 20$ Volts
BV_{CBO}	40	–	–	Volts	$I_C = 1.0\mu A$, $I_E = 0$
$V_{CER(sust)}$	20	–	–	Volts	$I_C = 30$ mA (pulsed), $R_{BE} \leq 10$ ohms (Notes 4 and 5)

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Min	Typ	Max	Unit	Conditions
$V_{CEO(sust)}$	15	–	–	Volts	I_C = 30 mA (pulsed), I_B = 0 (Notes 4 and 5)
BV_{EBO}	5.0	–	–	Volts	I_C = 0, I_E = 10 μA
I_{EBO}	–	0.007	0.1	μA	I_C = 0, V_{EB} = 4.0 Volts
I_{CEX}(125°C)	–	3.0	10	μA	V_{CE} = 20 Volts, V_{BE} = +0.25 Volt
τ_s	–	13	20	nsec	$I_C = I_{B1} \approx$ 20 mA, $I_{B2} \approx -20$ mA (Notes 7 and 8)
t_{d+r}	–	25	40	nsec	$I_C \approx$ 200 mA, $I_{B1} \approx$ 40 mA (Note 8)
t_{s+f}	–	25	40	nsec	$I_C \approx$ 200 mA, $I_{B1} \approx$ 40 mA, $I_{B2} \approx -20$ mA (Note 8)

NOTES:

(1) These ratings are limiting values above which the serviceability of any individual semiconductor device may be impaired

(2) These are steady state limits. The factory should be consulted on applications involving pulsed or low duty cycle operations.

(3) These ratings give a maximum junction temperature of 200°C and junction-to-case thermal resistance of 145°C/watt (derating factor of 6.9 mW/°C), junction-to-ambient thermal resistance of 486°C/watt (derating factor of 2.1 mW/°C)

(4) Rating refers to a high current point where collector-to-emitter voltage is lowest

(5) Pulse Conditions: length = 300μsec; duty cycle = 1%

(6) I_C = 1.0 mA through 20 mA

(7) Measured on Sampling Scope. PW ≥ 200 nsec.

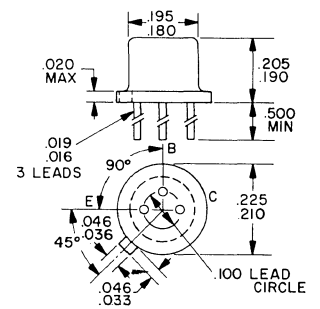
(8) See switching circuits for exact values of I_C, I_{B1}, and I_{B2}.

HIGH SPEED NPN SILICON PLANAR EPITAXIAL SATURATED SWITCHING TRANSISTORS

- High f_T: 650 mHz, typ.
- High Gain: 40 min. @ $I_C = 10mA$
- Low C_{ob} : 4pf max. @ $V_{CB} = 5V$
- Low T_{on} = 9 nsec typ.
- Low t_{off} = 13 nsec typ.

The ITT 2N2368 and 2N2369 are NPN silicon planar epitaxial saturated switching transistors for applications at current ranges from 0.1 to 100 mA. High gain and narrow base region provide excellent radiation resistance. They can operate at clock rates above 10 MHz for commercial computer applications.

DIMENSIONS

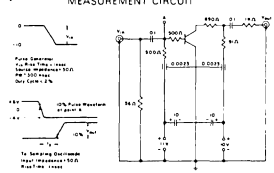
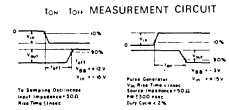
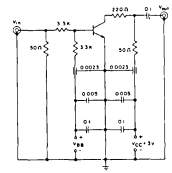


TO-18

ABSOLUTE MAXIMUM RATINGS

CHARACTERISTICS		UNITS
Collector-to-Base Voltage	40	Volts
Collector-to-Emitter Voltage (shorted base)	40	Volts
Collector-to-Emitter Voltage (open base)	15	Volts
Emitter-to-Base Voltage	4.5	Volts
Collector Current (10 μsec. pulse)	500	mA
Junction Temperature (op. and stg.)	−65 to +200	°C
Total Power Dissipation @ $T_C = 25°C$	1.2	Watts
(derate 6.8 mW/°C above 25°C)		
@ $T_C = 100°C$	0.68	Watts
Total Power Dissipation @ $T_A = 25°C$	0.36	Watts
(derate 2.06 mW/°C above 25°C)		

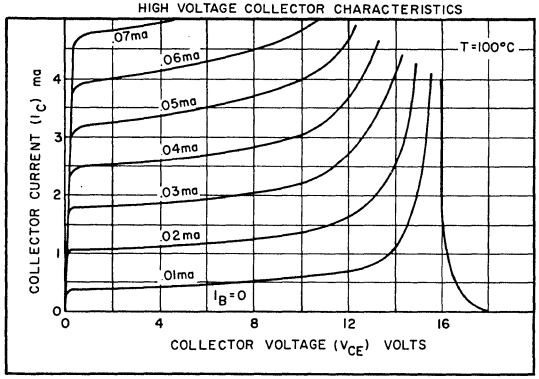
ELECTRICAL CHARACTERISTICS @ 25°C unless otherwise noted.

SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS
h_{FE} [1])	20 40		60 120		I_C=10mA, V_{CE}=1V 2N2368 2N2369
	10 20				I_C=10mA, V_{CE}=1V, T=−55°C 2N2368 2N2369
	10 20				I_C=100mA, V_{CE}=2V 2N2368 2N2369
V_{CE} (sat)		0.2	0.25	Vdc	I_C=10mA, I_B=1mA
V_{BE} (sat)	0.7	0.75	0.85	Vdc	I_C=10mA, I_B=1mA
I_{CBO}		0.1 10	0.4 30	μA μA	V_{CB}=20V, I_E=0 V_{CB}=20V, I_E=0, T=150°C
f_T		**650**		**MHz**	**V_{CE}=10V, I_C=10mA**
C_{ob}		**2.5**	**4.0**	**pf**	**V_{CB}=5V, I_E=0**
τ_S [2] (charge storage time)		**5**	**10**	**nsec**	$I_C = I_{B1} \approx 10$mA, $I_{B2} \approx -10$mA CHARGE STORAGE TIME MEASUREMENT CIRCUIT 
t_{on} (2)		**9.0**	**12**	**nsec**	**$I_C \approx 10$mA,** **$I_{B1} \approx 3$mA** t_{ON} t_{OFF} MEASUREMENT CIRCUIT 
t_{off} [2]		**10** **13**	**15** **18**	**nsec** **nsec**	**I_C 10mA,** **I_{B1} 3mA,** **$I_{B2} \approx -1.5$mA** 2N2368 2N2369 
BV_{CBO}	40			Vdc	I_C=10μA, I_E=0
BV_{CES}	40			Vdc	I_C=10μA, I_B=0
V_{CEO}(sust)	15			Vdc	I_C=10mA, I_B=0
BV_{EBO}	4.5			Vdc	I_E=10μA, I_C=0

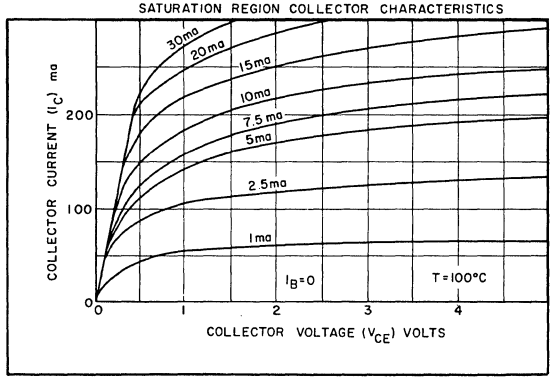
NOTES: 1. Pulse measurement: width ≤ 300 μsec, duty cycle ≤ 2%.
2. See switching circuits for exact I_C, I_{B1}, and I_{B2}.

TYPICAL CHARACTERISTICS[1]

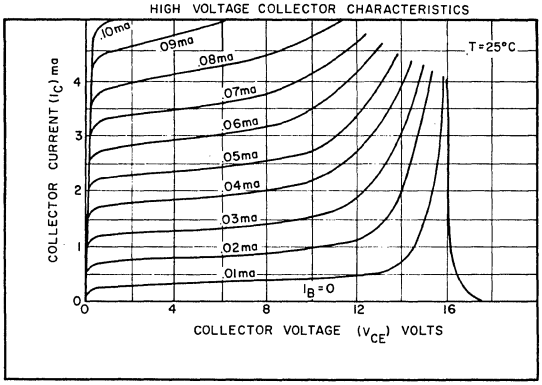
HIGH VOLTAGE COLLECTOR CHARACTERISTICS



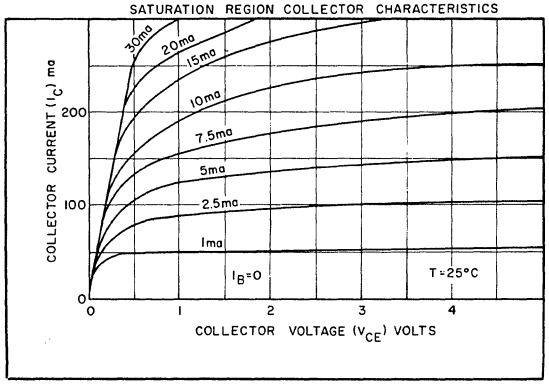
SATURATION REGION COLLECTOR CHARACTERISTICS



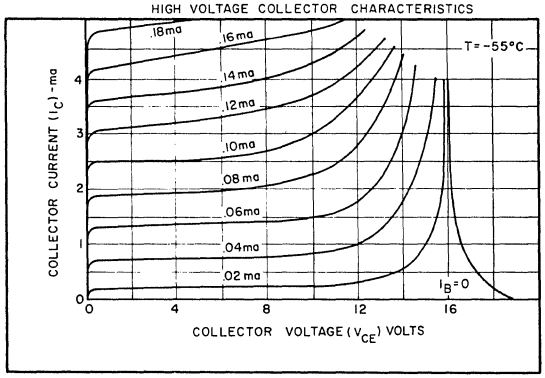
HIGH VOLTAGE COLLECTOR CHARACTERISTICS



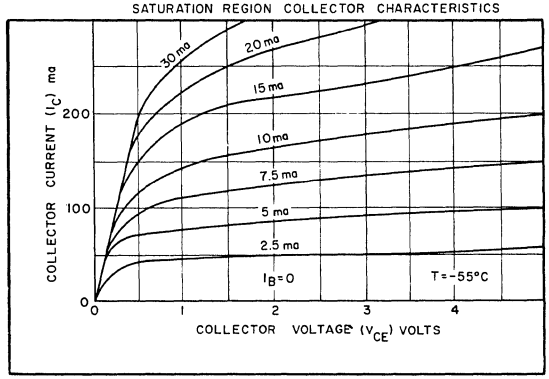
SATURATION REGION COLLECTOR CHARACTERISTICS



HIGH VOLTAGE COLLECTOR CHARACTERISTICS



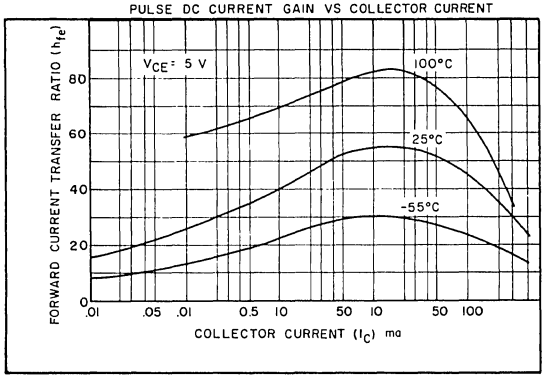
SATURATION REGION COLLECTOR CHARACTERISTICS



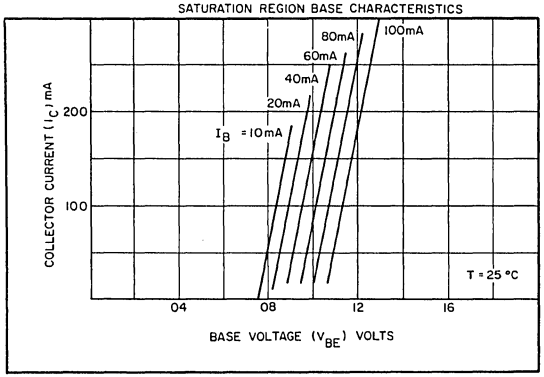
NOTE: Single family characteristics on Transistor Curve Tracer

TYPICAL CHARACTERISTICS, continued

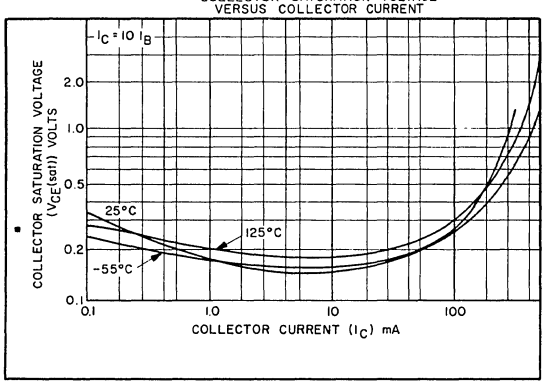
PULSE DC CURRENT GAIN VS COLLECTOR CURRENT



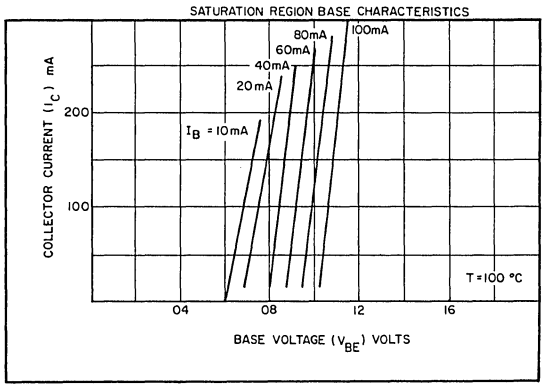
SATURATION REGION BASE CHARACTERISTICS



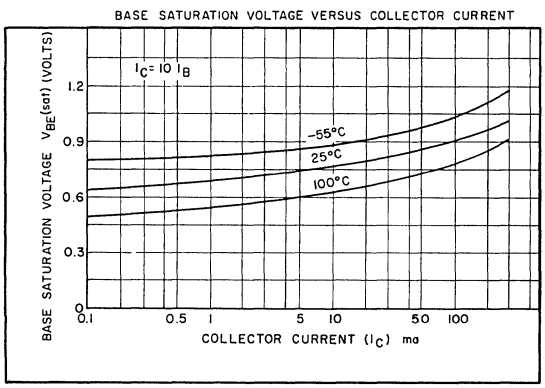
COLLECTOR SATURATION VOLTAGE VERSUS COLLECTOR CURRENT



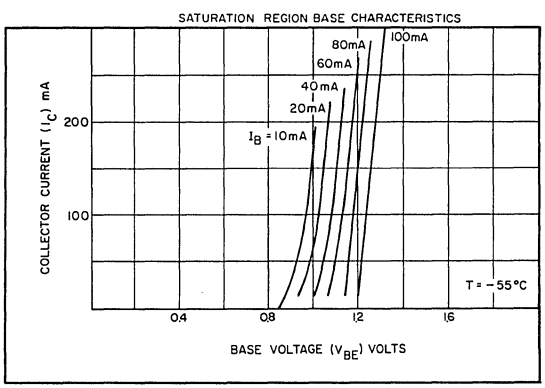
SATURATION REGION BASE CHARACTERISTICS



BASE SATURATION VOLTAGE VERSUS COLLECTOR CURRENT

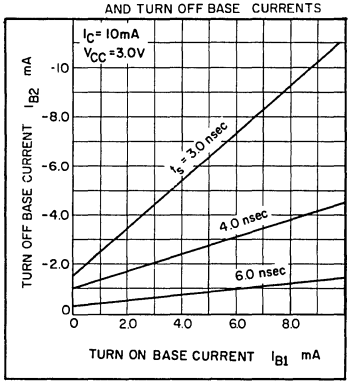


SATURATION REGION BASE CHARACTERISTICS

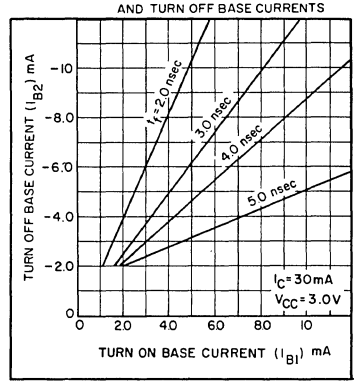


TYPICAL CHARACTERISTICS, continued

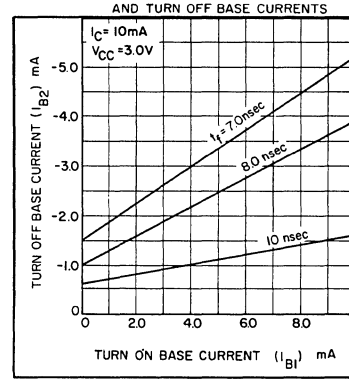
STORAGE TIME VERSUS TURN ON AND TURN OFF BASE CURRENTS



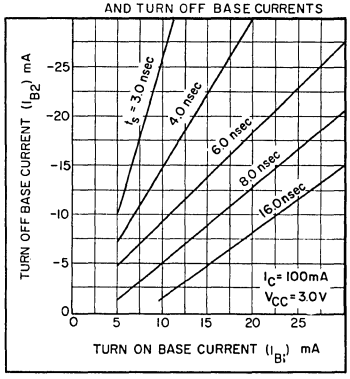
FALL TIME VERSUS TURN ON AND TURN OFF BASE CURRENTS



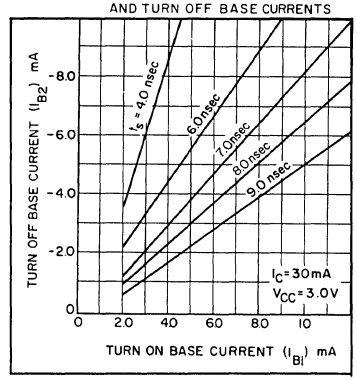
FALL TIME VERSUS TURN ON AND TURN OFF BASE CURRENTS



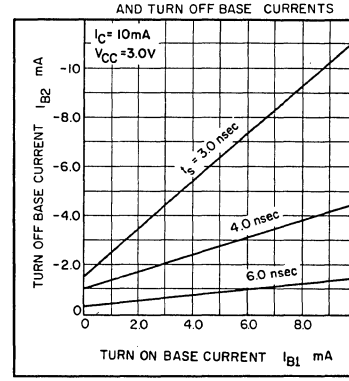
STORAGE TIME VERSUS TURN ON AND TURN OFF BASE CURRENTS



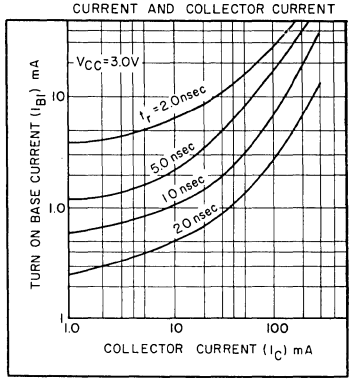
STORAGE TIME VERSUS TURN ON AND TURN OFF BASE CURRENTS



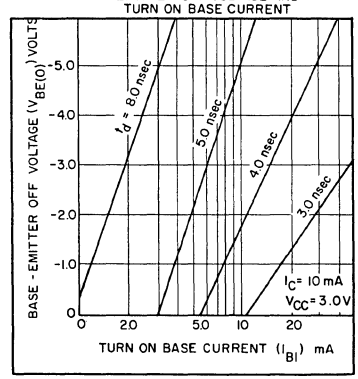
STORAGE TIME VERSUS TURN ON AND TURN OFF BASE CURRENTS



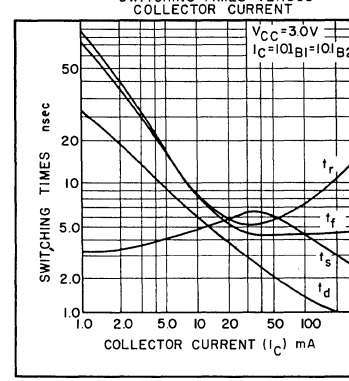
RISE TIME VERSUS TURN ON BASE CURRENT AND COLLECTOR CURRENT



DELAY TIME VERSUS BASE-EMITTER OFF VOLTAGE AND TURN ON BASE CURRENT



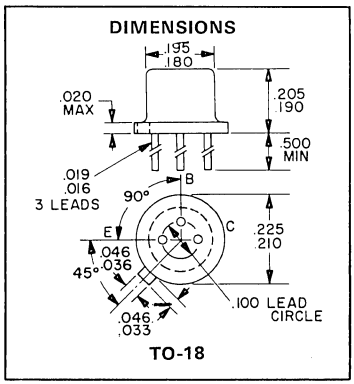
SWITCHING TIMES VERSUS COLLECTOR CURRENT



HIGH SPEED NPN SILICON SATURATED SWITCHING TRANSISTOR

- High f_T: 675 MHz, typ.
- High Gain: 40 min. @ $I_C = 10$ mA
- Low C_{ob}: 4 pf max. @ $V_{CB} = 5V$
- Low t_{on}: 9 nsec typ.;
- Low t_{off}: 13 nsec typ.

The ITT 2N2369A is a NPN silicon planar epitaxial saturated switching transistor for applications at current ranges from 0.1 to 100 mA. High gain and narrow base region provide excellent radiation resistance. The 2N2369A can operate at clock rates above 10 MHz for commercial computer applications.

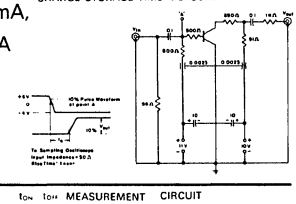
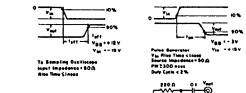
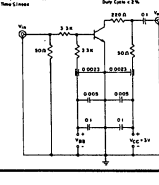


TO-18

ABSOLUTE MAXIMUM RATINGS

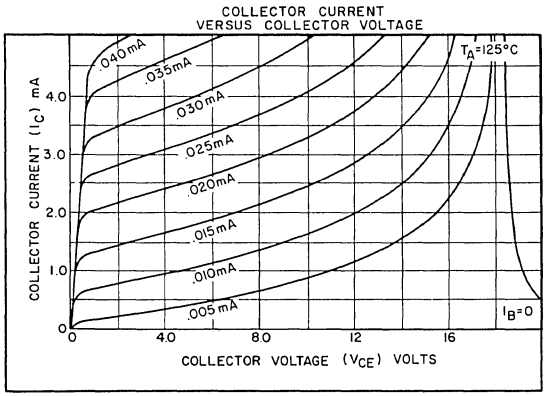
CHARACTERISTICS		UNITS
Collector-to-Base Voltage	40	Volts
Collector-to-Emitter Voltage (shorted base)	40	Volts
Collector-to-Emitter Voltage (open base)	15	Volts
Emitter-to-Base Voltage	4.5	Volts
Collector Current (continuous)	200	mA
Collector Current (10 μsec pulse)	500	mA
Junction Temperature (op. and stg.)	−65 to +200	°C
Total Power Dissipation @ $T_C = 25°C$	1.2	Watts
(derate 6.8 mW/°C above 25°C) @ $T_C = 100°C$	0.68	Watts
Total Power Dissipation @ $T_A = 25°C$ (derate 2.06 mW/°C above 25°C)	0.36	Watts

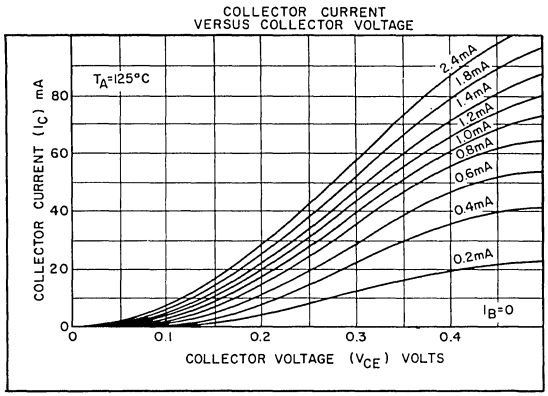
ELECTRICAL CHARACTERISTICS @ $T_A = 25°C$ unless otherwise noted

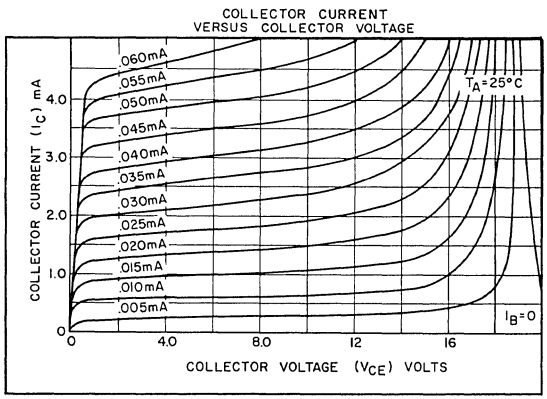
SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS
h_{FE}[1]	**40**	**66**	**120**		**I_C=10mA, V_{CE}=1V**
	40	**63**	**120**		**I_C=10mA, V_{CE}=0.35V**
	20	50			I_C=10mA, V_{CE}=0.35V, T=−55°C
	30	71			I_C=30mA, V_{CE}=0.4V
	20				I_C=100mA. V_{CE}=1V
V_{CE}(sat)		0.14	0.2	Vdc	I_C=10mA, I_B=1mA
		0.19	0.3	Vdc	I_C=10mA, I_B=1mA, T=125°C
		0.17	0.25	Vdc	I_C=30mA, I_B=3mA
		0.28	0.5	Vdc	I_C=100mA, I_B=10mA
V_{BE}(sat)	0.7	0.8	0.85	Vdc	I_C=10mA, I_B=1mA
	0.59		1.02	Vdc	I_C=10mA, I_C=1mA, T=−65 to +125°C
		0.9	1.15	Vdc	I_C=30mA, I_B=3mA
		1.1	1.6	Vdc	I_C=100mA, I_B=10mA
I_{CES}		0.05	0.4	μA	V_{CE}=20V, V_{BE}=0
I_{CBO}		10	30	μA	V_{CB}=20V, I_E=0, T=150°C
f_T	**500**	**675**		**MHz**	**V_{CE}=10V, I_C=10mA**
C_{ob}		**2.3**	**4.0**	**pf**	**V_{CB}=5V, I_E=0**
τ_S (charge storage time)		6.0	13	nsec	$I_C = I_{B1} \approx 10mA$, $I_{B2} \approx -10mA$ CHARGE STORAGE TIME MEASUREMENT CIRCUIT 
t_{on}		**9.0**	**12**	**nsec**	**$I_C \approx 10mA$, $I_{B1} \approx 3mA$** t_{on} t_{off} MEASUREMENT CIRCUIT 
t_{off}		**13**	**18**	**nsec**	**$I_C \approx 10mA$, $I_{B1} \approx 3mA$, $I_{B2} \approx -1.5mA$** 
BV_{CBO}	40			Vdc	I_C=10μA, I_E=0
BV_{CES}	40			Vdc	I_C=10μA, V_{BE}=0
V_{CEO}(sust)[1,2]	15			Vdc	I_C=10mA, I_B=0
BV_{EBO}	4.5			Vdc	I_E=10μA, I_C=0

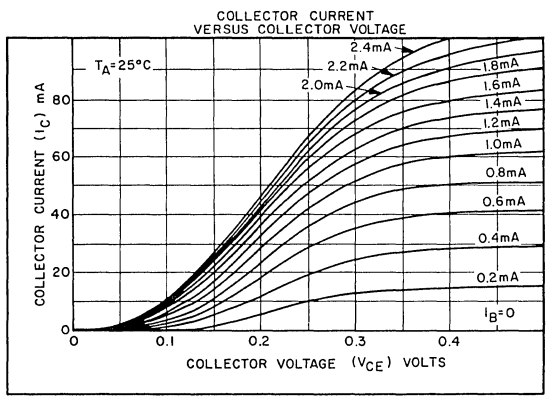
NOTES: 1. Pulse measurement: width ≤ 300 μsec, duty cycle ≤ 2%. 2. Rating refers to a high-current point where collector-to-emitter voltage is lowest.

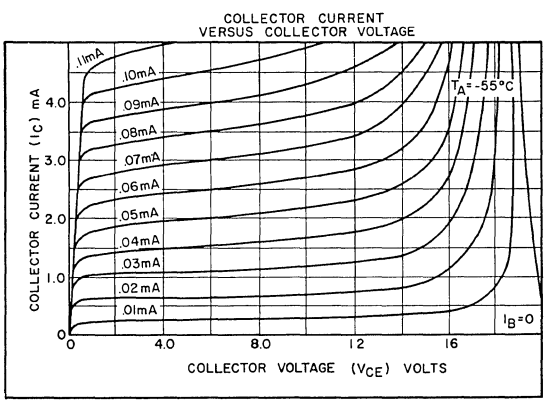
TYPICAL COLLECTOR CHARACTERISTICS[1]

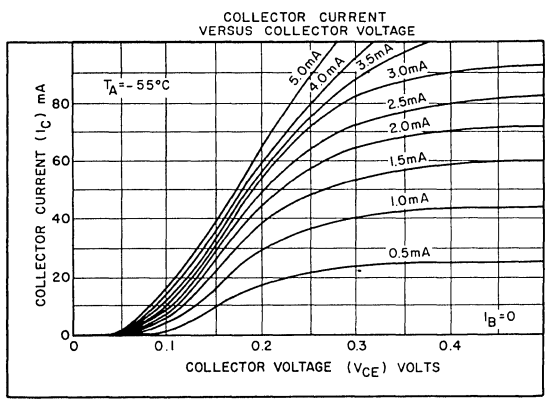








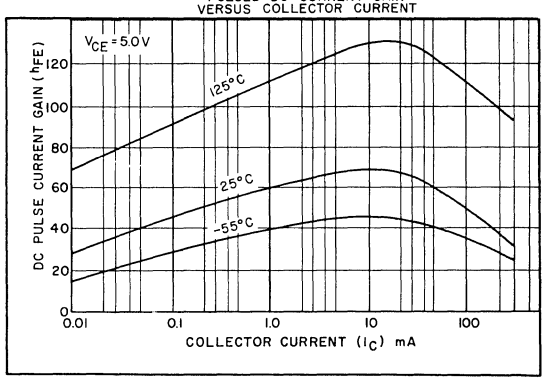




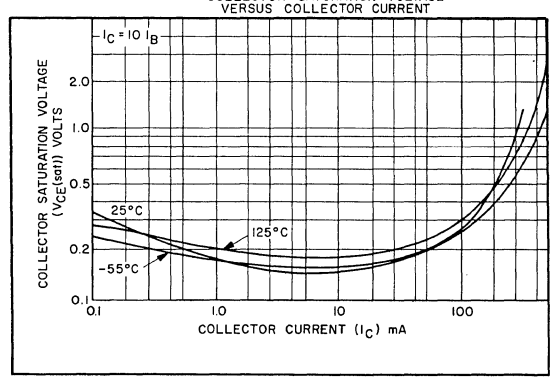
NOTE: Single family characteristics on Transistor Curve Tracer

TYPICAL COLLECTOR CHARACTERISTICS, continued

PULSED DC CURRENT GAIN
VERSUS COLLECTOR CURRENT

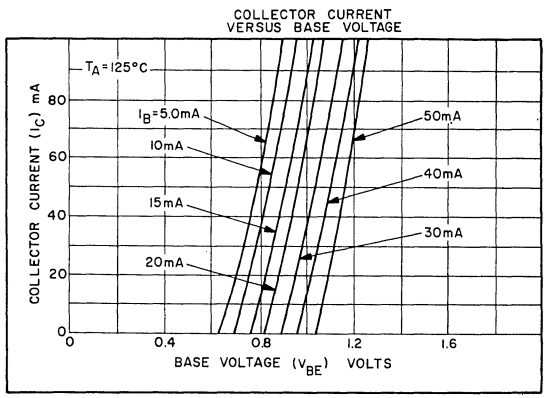


COLLECTOR SATURATION VOLTAGE
VERSUS COLLECTOR CURRENT

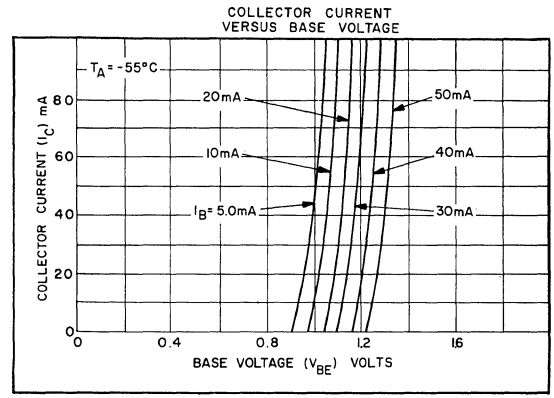


TYPICAL BASE CHARACTERISTICS[1]

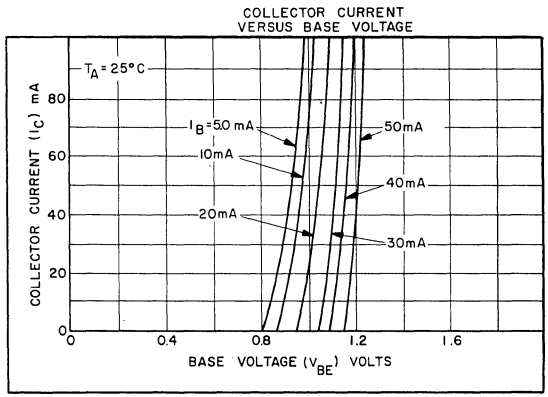
COLLECTOR CURRENT
VERSUS BASE VOLTAGE



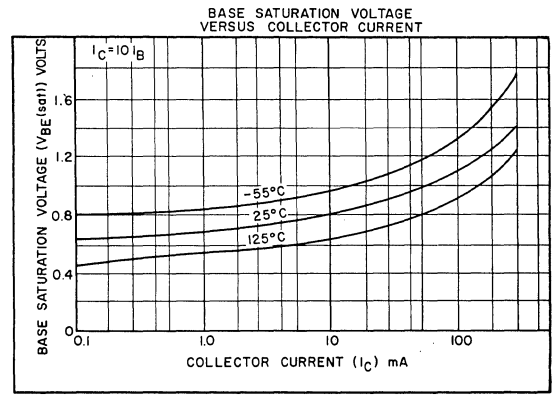
COLLECTOR CURRENT
VERSUS BASE VOLTAGE



COLLECTOR CURRENT
VERSUS BASE VOLTAGE

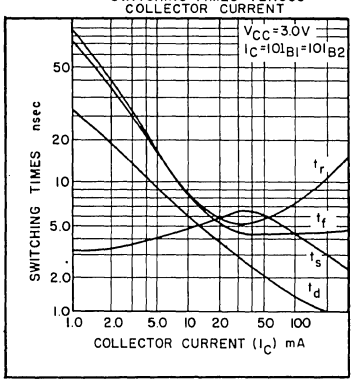


BASE SATURATION VOLTAGE
VERSUS COLLECTOR CURRENT

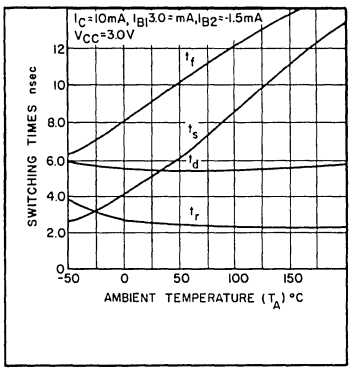


TYPICAL ELECTRICAL CHARACTERISTICS

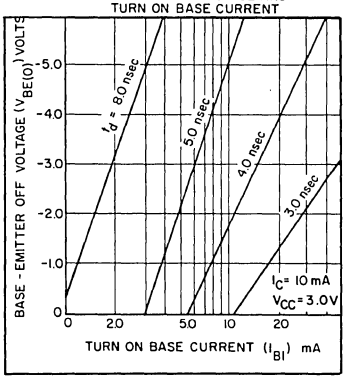
SWITCHING TIMES VERSUS COLLECTOR CURRENT



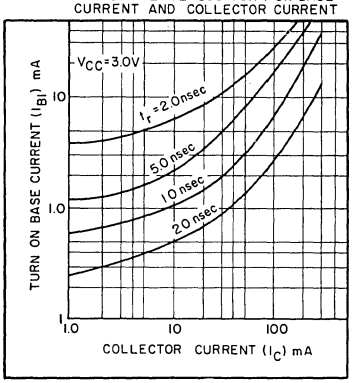
SWITCHING TIMES VERSUS AMBIENT TEMPERATURE



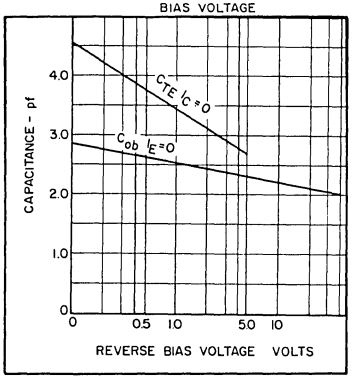
DELAY TIME VERSUS BASE-EMITTER OFF VOLTAGE AND TURN ON BASE CURRENT



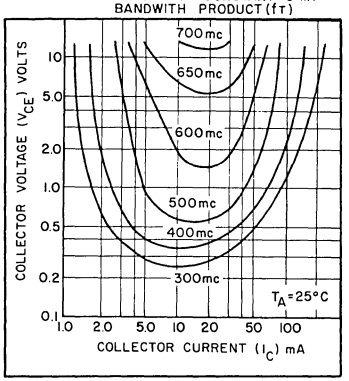
RISE TIME VERSUS TURN ON BASE CURRENT AND COLLECTOR CURRENT



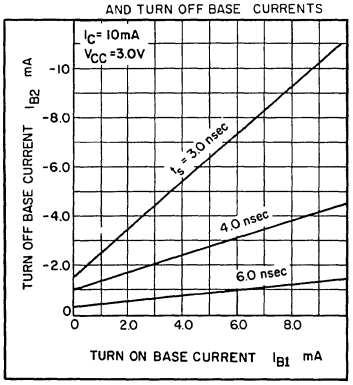
EMITTER TRANSITION AND OUTPUT CAPACITANCES VERSUS REVERSE BIAS VOLTAGE



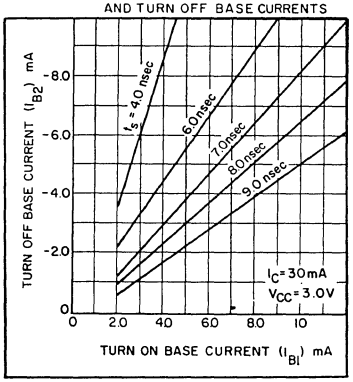
CONTOURS OF CONSTANT GAIN BANDWITH PRODUCT (fT)



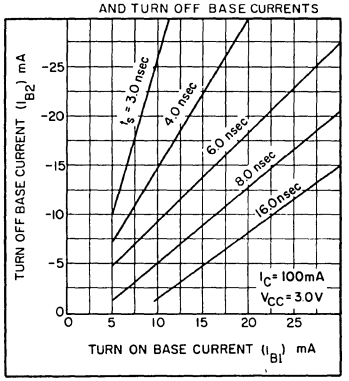
STORAGE TIME VERSUS TURN ON AND TURN OFF BASE CURRENTS



STORAGE TIME VERSUS TURN ON AND TURN OFF BASE CURRENTS

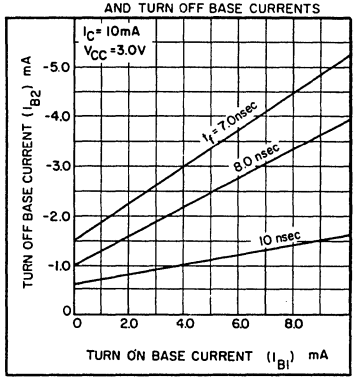


STORAGE TIME VERSUS TURN ON AND TURN OFF BASE CURRENTS

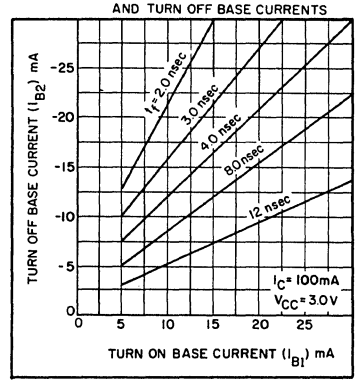


TYPICAL CHARACTERISTICS, continued

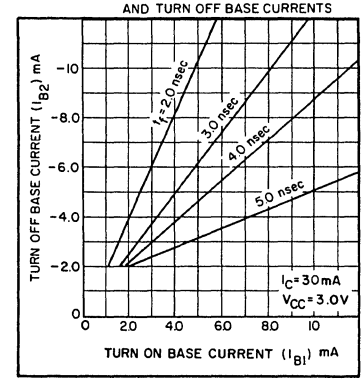
FALL TIME VERSUS TURN ON AND TURN OFF BASE CURRENTS



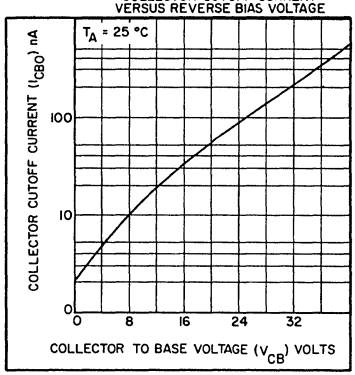
FALL TIME VERSUS TURN ON AND TURN OFF BASE CURRENTS



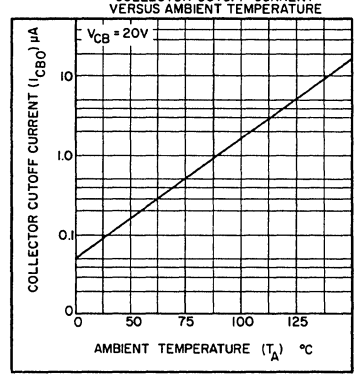
FALL TIME VERSUS TURN ON AND TURN OFF BASE CURRENTS



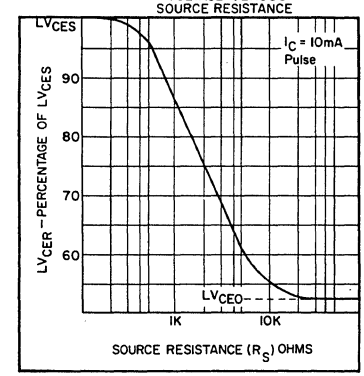
COLLECTOR CUTOFF CURRENT VERSUS REVERSE BIAS VOLTAGE



COLLECTOR CUTOFF CURRENT VERSUS AMBIENT TEMPERATURE



LOWER LIMITING VOLTAGE VERSUS SOURCE RESISTANCE



2N2710
HIGH-SPEED NPN SILICON SATURATED SWITCHING TRANSISTOR

ABSOLUTE MAXIMUM RATINGS

Characteristics	Unit
Collector-Emitter Voltage	20 Volts
Collector-Emitter Voltage	30 Volts
Collector-Base Voltage	40 Volts
Emitter-Base Voltage	5.0 Volts
Collector Current — Continuous	500 mA
Total Device Dissipation @ T_A = 25°C	0.36 Watt
Derate above 25°C	2.1 mW/°C
Total Device Dissipation @ T_C = 25°C	1.2 Watts
Operating Junction Temperature Range	+200 °C
Storage Temperature Range	−65 to +200 °C

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Min	Max	Unit	Conditions
BV_{CEO}	20	–	Volts	I_C = 10 mA, I_B = 0
BV_{CES}	30	–	Volts	I_C = 10 μA, V_{BE} = 0
BV_{CBO}	40	–	Volts	I_C = 10 μA, I_E = 0
BV_{EBO}	5.0	–	Volts	I_E = 10 μA, I_C = 0
I_{CBO}	–	30	μA	V_{CB} = 20 Volts, I_E = 0
I_{CBO}	–	30	μA	V_{CB} = 20 Volts, I_E = 0, T_A = +150°C
I_{EBO}	–	1.0	μA	V_{BE} = 3.0 Volts, I_C = 0
h_{FE}	40	–	–	I_C = 10 mA, V_{CE} = 1.0 Volt
h_{FE}	40	–	–	I_C = 50 mA, V_{CE} = 1.0 Volt
$V_{CE(sat)}$	–	0.25	Volt	I_C = 10 mA, I_B = 1.0 mA
$V_{CE(sat)}$	–	0.4	Volt	I_C = 50 mA, I_B = 5.0 mA
$V_{BE(sat)}$	–	0.9	Volt	I_C = 10 mA, I_B = 1.0 mA
$V_{BE(sat)}$	–	1.3	Volts	I_C = 50 mA, I_B = 5.0 mA
f_T	500	–	MHz	I_C = 10 mA, V_{CE} = 20 Volts, f = 100 MHz
C_{ob}	–	4.0	pF	V_{CB} = 10 Volts, I_E = 0, f = 4.0 MHz

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Min	Max	Unit	Conditions
t_{on}	–	20	ns	V_{CC} = 3.0 Volts, $V_{BE(off)}$ = 2.0 Volts, I_C = 10 mA, I_{B1} = 3.0 mA
t_{off}	–	35	ns	V_{CC} = 3.0 Volts, I_C = mA, I_{B1} = 3.0 mA, I_{B2} = 1.0 mA
t_s	–	15	ns	V_{CC} = 10 Volts, I_C = I_{B1} = I_{B2} = 10 mA

CIRCUIT DIAGRAM

FIGURE 1 – STORAGE TEST CIRCUIT

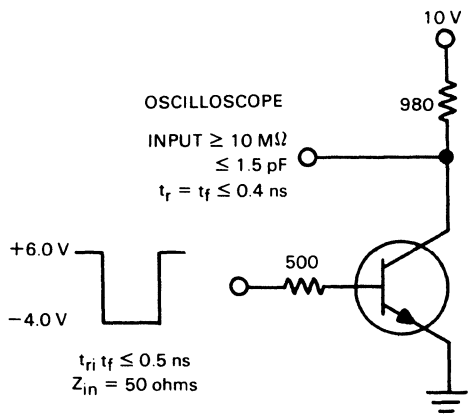
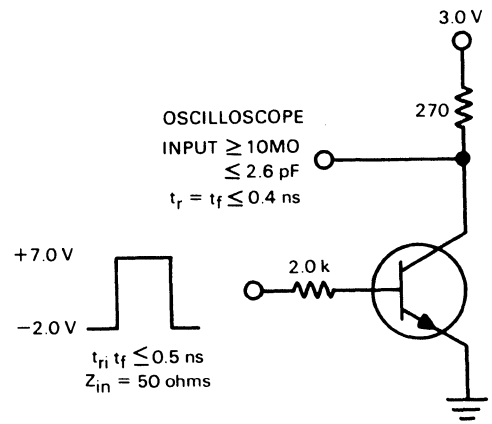


FIGURE 2 – TURN ON AND TURN OFF TIME TEST CIRCUIT



Package: TO-18

HIGH-SPEED NPN SILICON SATURATED SWITCHING TRANSISTOR

The ITT 2N3011 is an NPN silicon planar eptiaxial transistor designed specifically for high-speed saturated switching applications in the 50-100 mc range at current levels from 100 microamperes to 100 milliamperes. It is suitable for most small-signal, RF, and digital type circuits.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Characteristics	Unit
Collector-Base Voltage	30 Volts
Collector-Emitter Voltage	30 Volts
Collector-Emitter Voltage (Note 4)	12 Volts
Emitter-Base Voltage	5.0 Volts
Total Device Dissipation @:	
T_C = 25°C (Notes 2 and 3)	1.2 Watts
T_C = 100°C (Notes 2 and 3)	0.68 Watt
T_A = 25°C (Notes 2 and 3)	0.36 Watt
Storage Temperature	−65°C to +200 °C
Operating Junction Temperature	200°C Maximum
Lead Temperature (Soldering, 60 sec Time Limit)	300°C Maximum

NOTES:

(1) These ratings are limiting values above which the serviceability of any individual semiconductor device may be impaired.

(2) These are steady state limits. The factory should be consulted on applications involving pulsed or low duty cycle operations.

(3) These ratings give a maximum junction temperature of 200°C and junction-to-case thermal resistance of 146°C/watt (derating factor of 6.85 mW/°C); junction-to-ambient thermal resistance of 486°C/watt (derating factor of 2.06 mW/°C).

(4) Rating refers to a high-current point where collector-to-emitter voltage is lowest.

(5) Pulse Conditions: length = 300 μsec; duty cycle = 1%.

(6) See switching circuits for exact values of I_C, I_{B1}, and I_{B2}.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

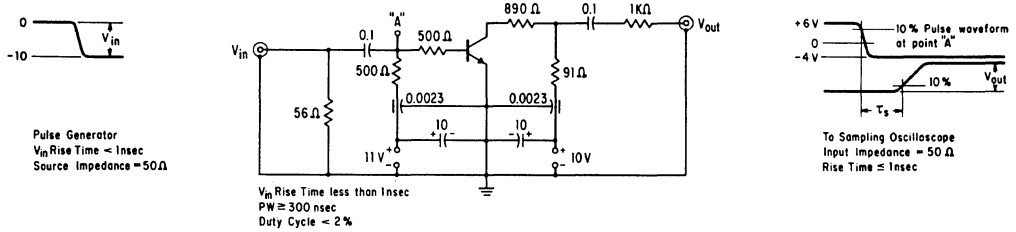
Symbol	Min	Typ	Max	Unit	Conditions
h_{FE}	30	70	120	–	I_C = 10 mA, V_{CE} = 0.35 Volt (Note 5)
h_{FE}	25	75	–	–	I_C = 30 mA, V_{CE} = 0.4 Volt (Note 5)
h_{FE}	12	50	–	–	I_C = 100 mA, V_{CE} = 1.0 Volt (Note 5)
$V_{CE(sat)}$	–	0.17	0.2	Volt	I_C = 10 mA, I_B = 1.0 mA
$V_{CE(sat)}$	–	0.18	0.25	Volt	I_C = 30 mA, I_B = 3.0 mA
$V_{CE(sat)}$	–	0.15	0.3	Volt	I_C = 10 mA, I_B = 1.0 mA
$V_{CE(sat)}$	–	0.3	0.5	Volt	I_C = 100 mA, I_B = 10 mA
$V_{BE(sat)}$	0.72	0.8	0.87	Volt	I_C = 10 mA, I_B = 1.0 mA
$V_{BE(sat)}$	–	0.9	1.15	Volts	I_C = 30 mA, I_B = 3.0 mA
$V_{BE(sat)}$	–	1.1	1.6	Volts	I_C = 100 mA, I_B = 10 mA
h_{fe}	4.0	6.5	–	–	I_C = 20 mA, V_{CE} = 10 Volts
C_{ob}	–	2.3	4.0	pf	I_E = 0, V_{CB} = 5.0 Volts

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

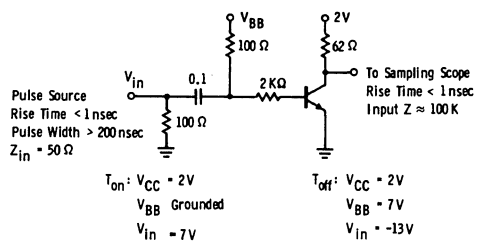
Symbol	Min	Typ	Max	Unit	Conditions
I_{CES}	–	0.05	0.4	μA	V_{CE} = 20 Volts, V_{BE} = 0
I_{CES}(85°C)	–	1.0	10	μA	V_{CE} = 20 Volts, V_{BE} = 0
BV_{CBO}	30	–	–	Volts	I_C = 10 μA, I_E = 0
BV_{CES}	30	–	–	Volts	I_C = 10 μA, V_{EB} = 0
$V_{CEO(sust)}$	12	–	–	Volts	I_C = 10 mA (pulsed), I_B = 0
BV_{EBO}	5.0	–	–	Volts	I_E = 100 μA, I_C = 0
τ_S	–	–	13	nsec	$I_C = I_{B1} \approx$ 10 mA, $I_{B2} \approx -10$ mA (Note 6)
t_{on}	–	–	15	nsec	$I_C \approx$ 30 mA, $I_{B1} \approx$ 3.0 mA (Note 6)
t_{off}	–	–	20	nsec	$I_C \approx$ 30 mA, $I_{B1} \approx$ 3.0 mA, $I_{B2} \approx -3.0$ mA (Note 6)

SCHEMATIC

CHARGE STORAGE TIME — CONSTANT TEST CIRCUIT



t_{on}-t_{off} MEASUREMENT CIRCUIT



Package: TO-18

NPN HIGH-SPEED SILICON SWITCHING AND AMPLIFIER TRANSISTORS

ABSOLUTE MAXIMUM RATINGS

Characteristics	Unit
Collector-Base Voltage	60 Volts
Collector-Emitter Voltage	20 Volts
Emitter-Base Voltage	5 Volts
Collector-Current	600 mA
Total Device Dissipation @ T_A = 25°C	1.8 Watts
Derate above 25°C	12 mW/°C
Total Device Dissipation @ T_A = 25°C	0.4 Watt
Derate above 25°C	2.67 mW/°C
Junction Temperature Range	−65 to +175°C
Storage Temperature Range	−65 to +200°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Min	Max	Unit	Conditions
I_{CBO}	–	0.025	μA	V_{CB} = 50 Volts, I_E = 0
I_{CBO}	–	15	μA	V_{CB} = 50 Volts, I_E = 0, T_A = 150°C
I_{CEX}	–	0.050	μA	V_{CE} = 30 Volts, V_{BE} = 0.5 Volt
I_{BL}	–	0.050	μA	V_{CE} = 30 Volts, V_{BE} = 0.5 Volt
BV_{CBO}	60	–	Volts	I_C = 10 μA, I_E = 0
BV_{CEO}*	20	–	Volts	I_C = 10 mA, pulsed, I_B = 0*
BV_{EBO}	5	–	Volts	I_E = 10 μA, I_C = 0
$V_{CE(sat)}$*	–	0.5	Volt	I_C = 150 mA, I_B = 15 mA*
$V_{BE(sat)}$*	–	1.3	Volts	I_C = 150 mA, I_B = 15 mA*
h_{FE}	40	120	–	I_C = 150 mA, 2N3115
h_{FE}	100	300	–	V_{CE} = 10 Volts, 2N3116
C_{ob}	–	8	pF	V_{CB} = 10 Volts, I_E = 0, f = 100 kHz
t_d	–	20	ns	V_{CC} = 30 Volts, I_{CS} = 150 mA, I_{B1} = 15 mA
t_r	–	75	ns	V_{CC} = 30 Volts, I_{CS} = 150 mA, I_{B1} = 15 mA

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Conditions				Symbol	Min	Max	Unit
t_s	–	300	ns	V_{CC} = 6 Volts, I_{CS} = 150 mA, I_{B1} = 15 mA, I_{B2} = 15 mA			
t_f	–	200	ns	V_{CC} = 6 Volts, I_{CS} = 150 mA, I_{B1} = 15 mA, I_{B2} = 15 mA			
f_T	250	–	MHz	I_C = 20 mA, V_{CE} = 20 Volts, f = 100 MHz			

* Pulse Test: Pulse Width $\leq$ 300 μs; Duty Cycle $\leq$ 2.0%

Package: TO-92

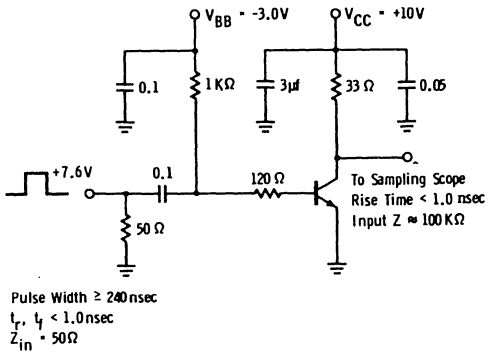
HIGH-SPEED NPN SILICON SATURATED SWITCHING TRANSISTOR

The ITT 2N3646 is an NPN silicon planar epitaxial transistor designed for logic and memory applications to 500 milliamperes. It features the unique combination of 350 Mc f_T minimum with a guaranteed 300 milliampere collector saturation voltage of 0.5 volt.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Characteristics	Unit
Collector-Base Voltage	40 Volts
Collector-Emitter Voltage	40 Volts
Collector-Emitter Voltage (Note 4)	15 Volts
Emitter-Base Voltage	5.0 Volts
Total Dissipation @:	
T_C = 25°C (Notes 2 and 3)	0.5 Watt
T_A = 25°C (Notes 2 and 3)	0.2 Watt
Storage Temperature	−55°C to +125°C
Operating Junction Temperature	+125°C Maximum
Lead Temperature (Soldering, 10 sec Time Limit)	+260°C Maximum

T_{ON} and T_{OFF} TEST CIRCUIT



ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Min	Typ	Max	Unit	Conditions
$V_{CE(sat)}$	–	0.16	0.2	Volt	I_C = 30 mA, I_B = 3.0 mA (Note 5)
$V_{CE(sat)}$	–	0.18	0.28	Volt	I_C = 100 mA, I_B = 10 mA (Note 5)
$V_{CE(sat)}$	–	0.18	0.3	Volt	I_C = 30 mA, I_B = 3.0 mA (Note 5) (T_A = +65°C)
$V_{CE(sat)}$	–	0.39	0.5	Volt	I_C = 300 mA, I_B = 30 mA (Note 5)
h_{fe}	3.5	5.5	–	–	I_C = 30 mA, V_{CE} = 10 Volts
τ_s	–	8.0	18	nsec	$I_C = I_{B1} \approx$ 10 mA, $I_{B2} \approx -10$ mA (Note 6)
t_{on}	–	9.0	18	nsec	$I_C \approx$ 300 mA, $I_{B1} \approx$ 30 mA (Note 6)
t_{off}	–	15	28	nsec	$I_C \approx$ 300 mA, $I_{B1} \approx$ 30 mA, $I_{B2} \approx -30$ mA (Note 6)
C_{obo}	–	3.3	5.0	pf	I_E = 0, V_{CB} = 5.0 Volts

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Min	Typ	Max	Unit	Conditions
C_{ibo}	–	6.6	8.0	pf	I_C = 0, V_{EB} = 0.5 Volt
h_{FE}	30	60	120	–	I_C = 30 mA, V_{CE} = 0.4 Volt (Note 5)
h_{FE}	25	55	–	–	I_C = 100 mA, V_{CE} = 0.5 Volt (Note 5)
h_{FE}	15	–	–	–	I_C = 300 mA, V_{CE} = 1.0 Volt (Note 5)
BV_{CBO}	40	–	–	Volts	I_C = 100 μA, I_E = 0
BV_{CES}	40	–	–	Volts	I_C = 100 μA, V_{EB} = 0
$V_{CEO(sust)}$	15	–	–	Volts	I_C = 10 mA, I_B = 0 (Notes 4 and 5)
BV_{EBO}	5.0	–	–	Volts	I_E = 100 μA, I_C = 0
$V_{BE(sat)}$	0.75	0.82	0.95	Volt	I_C = 30 mA, I_B = 3.0 mA (Note 5)
$V_{BE(sat)}$	–	0.97	1.2	Volts	I_C = 100 mA, I_B = 10 mA (Note 5)
$V_{BE(sat)}$	–	1.3	1.7	Volts	I_C = 300 mA, I_B = 30 mA (Note 5)
I_{CES}	–	0.04	0.5	μA	V_{CE} = 20 Volts, V_{EB} = 0
$I_{CES(65°C)}$	–	0.5	3.0	μA	V_{CE} = 20 Volts, V_{EB} = 0

(1) These ratings are limiting values above which the serviceability of any individual semiconductor device may be impaired.

(2) These are steady state limits. The factory should be consulted on applications involving pulsed or low duty cycle operations.

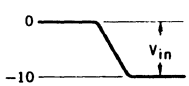
(3) These ratings give a minimum junction temperature of 125°C and junction-to-case thermal resistance of 200°C/watt (derating factor of 5.0 mW/°C); junction-to-ambient thermal resistance of 500°C/watt (derating factor of 2.0 mW/°C).

(4) Rating refers to a high-current point where collector-to-emitter voltage is lowest.

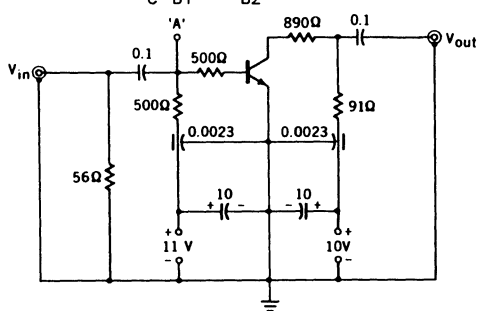
(5) Pulse Conditions: length = 300μsec; duty cycle = 1%.

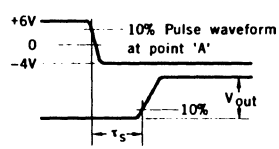
(6) See switching circuits for exact values of I_C, I_{B1}, and I_{B2}.

CHARGE STORAGE TIME MEASUREMENT CIRCUIT



Pulse Generator
V_{in} Rise Time < 1 nsec
Source Impedance = 50Ω
PW ≥ 300 nsec
Duty Cycle < 2%





To Sampling Oscilloscope
Z_{IN} ≈ 100 KΩ
Rise Time ≤ 1 nsec

ABSOLUTE MAXIMUM RATINGS

Characteristics	Unit
Collector-Emitter Voltage	40 Volts
Collector-Base Voltage	60 Volts
Emitter-Base Voltage	6.0 Volts
Collector-Current	200 mA
Total Device Dissipation @ T_A = 25°C	310 mW
Total Device Dissipation @ T_A = 60°C	210 mW
Derate above 25°C	2.81 mW/°C
Operating and Storage Junction Temperature Range	−55 to +135 °C
Thermal Resistance, Junction to Ambient	0.357 °C/mW

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Min	Max	Unit	Conditions
BV_{CBO}	60	–	Volts	I_C = 10 μA, I_E = 0
BV_{CEO}*	40	–	Volts	I_C = 1.0 mA, I_B = 0*
BV_{EBO}	6.0	–	Volts	I_E = 10 μA, I_C = 0
I_{CEX}	–	50	nA	V_{CE} = 30 Volts, $V_{EB(off)}$ = 3.0 Volts
h_{FE}*	20	–	–	I_C = 0.1 mA, V_{CE} = 1.0 Volt (2N3903)
h_{FE}*	40	–	–	I_C = 0.1 mA, V_{CE} = 1.0 Volt* (2N3904)
h_{FE}*	35	–	–	I_C = 1.0 mA, V_{CE} = 1.0 Volt (2N3903)
h_{FE}*	70	–	–	I_C = 1.0 mA, V_{CE} = 1.0 Volt (2N3904)
h_{FE}*	50	150	–	I_C = 10 mA, V_{CE} = 1.0 Volt (2N3903)
h_{FE}*	100	300	–	I_C = 10 mA, V_{CE} = 1.0 Volt (2N3904)
h_{FE}*	30	–	–	I_C = 50 mA, V_{CE} = 1.0 Volt (2N3903)
h_{FE}*	60	–	–	I_C = 50 mA, V_{CE} = 1.0 Volt (2N3904)
h_{FE}*	15	–	–	I_C = 100 mA, V_{CE} = 1.0 Volt (2N3903)
h_{FE}*	30	–	–	I_C = 100 mA, V_{CE} = 1.0 Volt (2N3904)

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Min	Max	Unit	Conditions
$V_{CE(sat)}$*	–	0.2	Volt	I_C = 10 mA, I_B = 1.0 mA*
$V_{CE(sat)}$*	–	0.3	Volt	I_C = 50 mA, I_B = 5.0 mA
$V_{BE(sat)}$*	0.65	0.85	Volt	I_C = 10 mA, I_B = 1.0 mA*
$V_{BE(sat)}$*	–	0.95	Volt	I_C = 50 mA, I_B = 5.0 mA
f_T	250	–	MHz	I_C = 10 mA, V_{CE} = 20 Volts f = 100 MHz (2N3903)
f_T	300	–	MHz	I_C = 10 mA, V_{CE} = 20 Volts f = 100 MHz (2N3904)
C_{ob}	–	4.0	pF	V_{CB} = 5.0 Volts, I_E = 0, f = 100 kHz
C_{ib}	–	8.0	pF	V_{BE} = 0.5 Volt, I_C = 0, f = 100 kHz
h_{ie}	0.5	8.0	k ohms	I_C = 1.0 mA, V_{CE} = 10 Volts, f = 1.0 kHz (2N3903)
h_{ie}	1.0	10	k ohms	I_C = 1.0 mA, V_{CE} = 10 Volts, f = 1.0 kHz (2N3904)
h_{re}	0.1	5.0	X 10^{-4}	I_C = 1.0 mA, V_{CE} = 10 Volts, f = 1.0 kHz (2N3903)
h_{re}	0.5	8.0	X 10^{-4}	I_C = 1.0 mA, V_{CE} = 10 Volts f = 1.0 kHz (2N3904)
h_{fe}	50	200	–	I_C = 1.0 mA, V_{CE} = 10 Volts, f = 1.0 kHz (2N3903)
h_{fe}	100	400	–	I_C = 1.0 mA, V_{CE} = 10 Volts, f = 1.0 kHz (2N3904)
h_{oe}	1.0	40	μmhos	I_C = 1.0 mA, V_{CE} = 10 Volts, f = 1.0 kHz
t_d t_r	– –	35 35	ns ns	V_{CC} = 3.0 Volts, $V_{BE(off)}$ = 0.5 Volt, I_C = 10 mA, I_{B1} = 1.0 mA
t_s	–	175	ns	V_{CC} = 3.0 Volts, I_C = 10 mA, I_{B1} = I_{B2} = 1.0 mA (2N3903)

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Min	Max	Unit	Conditions
t_s	–	200	ns	V_{CC} = 3.0 Volts, I_C = 10 mA, I_{B1} = I_{B2} = 1.0 mA
t_f	–	50	ns	V_{CC} = 3.0 Volts, I_C = 10 mA, I_{B1} = I_{B2} = 1.0 mA

* Pulse Test: Pulse Width = 300μs, Duty Cycle = 2%.

SCHEMATIC

FIGURE 1 – DELAY AND RISE TIME EQUIVALENT TEST CIRCUIT

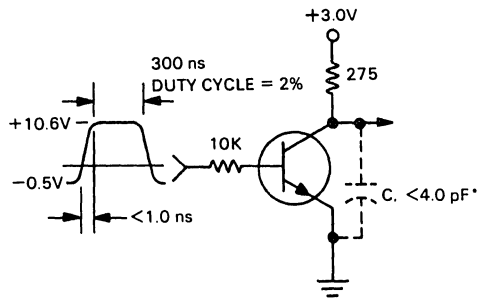
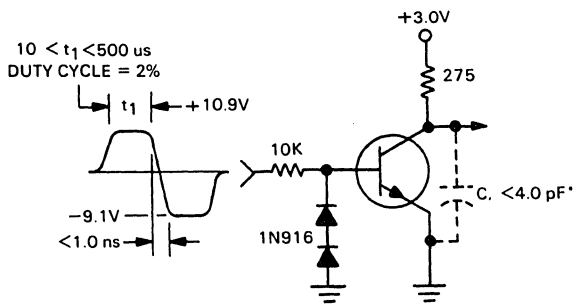


FIGURE 2 – STORAGE AND FALL TIME EQUIVALENT TEST TIME



*Total shunt capacitance of test jig and connectors

2N4123, 2N4124
GENERAL PURPOSE NPN SILICON SWITCHING AND AMPLIFIER TRANSISTORS

Package: To-92

ABSOLUTE MAXIMUM RATINGS

Characteristic	2N4123	2N4124	Unit
Collector-Emitter Voltage	30	25	Vdc
Collector-Base Voltage	40	30	Vdc
Emitter-Base Voltage	5.0		Vdc
Collector Current	200		mAdc
Total Device Dissipation @ T_A = 60°C	210		mW
Total Device Dissipation @ T_A = 25°C	310		mW
Derate above 25°C	2.81		mW/°C
Operating and Storage Junction Temperature Range	-55 to +135		°C
Thermal Resistance, Junction to Ambient	0.357		°C/mW

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Min	Max	Unit	Conditions	
BV_{CEO}*	30	–	Vdc	I_C = 1 mAdc, I_E = 0	2N4123
	25	–			2N4124
BV_{CBO}	40	–	Vdc	I_C = 10 uAdc, I_E = 0	2N4123
	30	–			2N4124
BV_{EBO}	5.0	–	Vdc	I_E = 10 uAdc, I_C = 0	
I_{CBO}	–	50	nAdc	V_{CB} = 20 Vdc, I_E = 0	
I_{EBO}	–	50	nAdc	V_{BE} = 3 Vdc, I_C = 0	
h_{FE}*	50	150	–	I_C = 2 mAdc, V_{CE} = 1 Vdc	2N4123
	120	360			2N4124
	25	–		I_C = 50 mAdc, V_{CE} = 1 Vdc	2N4123
	60	–			2N4124
$V_{CE(sat)}$*	–	0.3	Vdc	I_C = 50 mAdc, I_B = 5 mAdc	
$V_{BE(sat)}$*	–	0.95	Vdc	I_C = 50 mAdc, I_B = 5 mAdc	
$[h_{fe}]$	2.5	–	–	I_C = 10 mAdc, V_{CE} = 20 Vdc, f = 100 MHz	2N4123
	3.0	–			2N4124
f_T	250	–	MHz	I_C = 10 mAdc, V_{CE} = 20 Vdc, f = 100 MHz	2N4123
	300	–			2N4124
C_{ob}	–	4.0	pF	V_{CB} = 5 Vdc, I_E = 0, f = 100 kHz	
C_{ib}	–	8.0	pF	V_{BE} = 0.5 Vdc, I_C = 0, f = 100 kHz	
h_{fe}	50	200	–	I_C = 2 mAdc, V_{CE} = 1 Vdc, f = 1 kHz	2N4123
	120	480			2N4124
NF	–	6.0	dB	I_C = 100 uAdc, V_{CE} = 5 Vdc, R_S = 1 k ohm, Noise Bandwidth = 10 Hz to 15.7 kHz	2N4123
	–	5.0			2N4124
t_d	Typ. 24		ns	Delay Time V_{CC} = 3 Vdc, $V_{EB(off)}$ = 0.5 Vdc,	
t_r	Typ. 13		ns	Rise Time I_C = 10 mAdc, I_{B1} = 1 mAdc	
t_s	Typ. 125		ns	Storage Time V_{CC} = 3 Vdc, I_C = 10 mAdc,	
t_f	Typ. 11		ns	Fall Time $I_{B1} = I_{B2}$ = 1 mAdc	

*Pulse Test: Pulse Width = 300 us, Duty Cycle = 2%.

GENERAL PURPOSE NPN SILICON SWITCHING AND AMPLIFIER TRANSISTOR

Package: To-92

ABSOLUTE MAXIMUM RATINGS

Characteristic	2N4125	2N4126	Unit
Collector-Emitter Voltage	30	25	Vdc
Collector-Base Voltage	30	25	Vdc
Emitter-Base Voltage	4.0		Vdc
Collector Current	200		mAdc
Total Device Dissipation @ T_A = 60°C	210		mW
Total Device Dissipation @ T_A = 25°C	310		mW
Derate above 25°C	2.81		mW/°C
Operating and Storage Junction Temperature Range	-55 to +135		°C
Thermal Resistance, Junction to Ambient	0.357		°C/mW

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Min	Max	Unit	Conditions	
BV_{CEO}*	30	–	Vdc	I_C = 1 mAdc, I_E = 0	2N4125
	25	–			2N4126
BV_{CBO}	30	–	Vdc	I_C = 10 uAdc, I_E = 0	2N4125
	25	–			2N4126
BV_{EBO}	4.0	–	Vdc	I_E = 10 uAdc, I_C = 0	
I_{CBO}	–	50	nAdc	V_{CB} = 20 Vdc, I_E = 0	
I_{EBO}	–	50	nAdc	V_{BE} = 3 Vdc, I_C = 0	
h_{FE}*	50	150	–	I_C = 2 mAdc, V_{CE} = 1 Vdc	2N4125
	120	360			2N4126
	25	–		I_C = 50 mAdc, V_{CE} = 1 Vdc	2N4125
	60	–			2N4126
$V_{CE(sat)}$*	–	0.4	Vdc	I_C = 50 mAdc, I_B = 5 mAdc	
$V_{BE(sat)}$*	–	0.95	Vdc	I_C = 50 mAdc, I_B = 5 mAdc	
h_{fe}	2.0	–	–	I_C = 10 mAdc, V_{CE} = 20 Vdc, f = 100 MHz	2N4125
	2.5	–			2N4126
f_T	200	–	MHz	I_C = 10 mAdc, V_{CE} = 20 Vdc, f = 100 MHz	2N4125
	250	–			2N4126
C_{ob}	–	4.5	pF	V_{CB} = 5 Vdc, I_E = 0, f = 100 kHz	
C_{ib}	–	10	pF	V_{BE} = 0.5 Vdc, I_C = 0, f = 100 kHz	
h_{fe}	50	200	–	I_C = 2 mAdc, V_{CE} = 1 Vdc, f = 1 kHz	2N4125
	120	480			2N4126
NF	–	5.0	dB	I_C = 100 uAdc, V_{CE} = 5 Vdc, R_S = 1 ohm,	
	–				2N4125
	–	4.0		Noise Bandwidth = 10 Hz to 15.7 kHz	
					2N4126
t_d	Typ 25		ns	Delay Time V_{CC} = 3 Vdc, $V_{BE(off)}$ = 0.5 Vdc,	
t_r	Typ 18		ns	Rise Time I_C = 10 mAdc, I_{B1} = 1 mAdc	
t_s	Typ 140		ns	Storage Time V_{CC} = 3 Vdc, I_C = 10 mAdc,	
t_f	Typ 15		ns	Fall Time I_{B1} = I_{B2} = 1 mAdc	

*Pulse Test: Pulse Width = 300 usec, Duty Cycle = 2%.

2N4137Ⓕ

HIGH-SPEED NPN SILICON SATURATED SWITCHING TRANSISTOR

Package: TO-18

- **HIGH FREQUENCY CURRENT GAIN** ..... f_T = 500 MHz Min.
- **HIGH VOLTAGE** ..... LV_{CEO} = 20 Volts Min.
- **LOW CAPACITY** ..... C_{obo} = 4.0 pf Max.
- **LOW CHARGE STORAGE TIME** ..... τ_s = 13 ns Max.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Characteristics	Unit
Collector-Base Voltage	40 Volts
Collector-Emitter Voltage	40 Volts
Collector-Emitter Voltage (Note 4)	20 Volts
Emitter-Base Voltage	4.5 Volts
Collector Current (10 μsec Pulse)	500 mA
DC Collector Current	200 mA
Total Device Dissipation @:	
T_C = 25°C (Notes 2 and 3)	1.2 Watts
T_C = 100°C (Notes 2 and 3)	0.68 Watt
T_A = 25°C (Notes 2 and 3)	0.36 Watt
Storage Temperature	−65°C to +200°C
Operating Temperature	200°C Maximum
Lead Temperature (Soldering, 60 sec Time Limit)	300°C Maximum

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Min	Typ	Max	Unit	Conditions
h_{FE}	40	66	120	–	I_C = 10 mA, V_{CE} = 1.0 Volt (Note 5)
h_{FE}(−55°C)	20	50	–	–	I_C = 10 mA, V_{CE} = 0.35 Volt (Note 5)
$V_{BE(sat)}$	0.72	0.8	0.85	Volt	I_C = 10 mA, I_B = 1.0 mA (Note 5)
$V_{BE(sat)}$	0.59	–	1.02	Volts	I_C = 10 mA, I_B = 1.0 mA (Note 5)
$V_{BE(sat)}$	–	0.9	1.15	Volts	I_C = 30 mA, I_B = 3.0 mA (Note 5)
$V_{BE(sat)}$	–	1.1	1.6	Volts	I_C = 100 mA, I_B = 10 mA (Note 5)
$V_{CE(sat)}$	–	0.19	0.3	Volt	I_C = 10 mA, I_B = 1.0 mA (Note 5)
I_{CES}	–	0.05	0.4	μA	V_{BE} = 0, V_{CE} = 20 Volts
I_{CBO}(150°C)	–	10	30	μA	I_E = 0, V_{CB} = 20 Volts

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Min	Typ	Max	Unit	Conditions
BV_{CES}	40	–	–	Volts	I_C = 10 μA, V_{BE} = 0
BV_{CBO}	40	–	–	Volts	I_C = 10 μA, I_E = 0
$V_{CEO(sust)}$	20	–	–	Volts	I_C = 10 mA (pulsed), I_B = 0 (Notes 4 and 5)
BV_{EBO}	4.5	–	–	Volts	I_E = 10 μA, I_C = 0
h_{FE}	40	63	120	–	I_C = 10 mA, V_{CE} = 0.35 Volt (Note 5)
h_{FE}	30	71	–	–	I_C = 30 mA, V_{CE} = 0.4 Volt (Note 5)
h_{FE}	20	–	–	–	I_C = 100 mA, V_{CE} = 1.0 Volt (Note 5)
$V_{CE(sat)}$	–	0.14	0.2	Volt	I_C = 10 mA, I_B = 1.0 mA (Note 5)
$V_{CE(sat)}$	–	0.12	0.18	Volt	I_C = 10 mA, I_B = 3.3 mA (Note 5)
$V_{CE(sat)}$	–	0.17	0.25	Volt	I_C = 30 mA, I_B = 3.0 mA (Note 5)
$V_{CE(sat)}$	–	0.28	0.5	Volt	I_C = 100 mA, I_B = 10 mA (Note 5)
$V_{BE(sat)}$	0.74	0.85	1.0	Volt	I_C = 10 mA, I_B = 3.3 mA (Note 5)
h_{fe}	5.0	6.75	–	–	I_C = 10 mA, V_{CE} = 10 Volts
C_{ob}	–	2.3	4.0	pf	I_E = 0, V_{CB} = 5.0 Volts
τ_s	–	6.0	13	nsec	$I_C = I_{B1} \approx$ 10 mA, $I_{B2} \approx -10$ mA (Note 6)
t_{on}	–	9.0	12	nsec	$I_C \approx$ 10 mA, $I_{B1} \approx$ 3.3 mA (Note 6)
t_{off}	–	7.0	12	nsec	$I_C \approx$ 10 mA, $I_{B1} \approx$ 3.3 mA, $I_{B2} \approx -3.3$ mA (Note 6)

NOTES:

(1) These ratings are limiting values above which the serviceability of any individual semiconductor device may be impaired.

(2) These are steady state limits. The factory should be consulted on applications involving pulsed or low duty cycle operations.

(3) These ratings give a maximum junction temperature of 200°C and junction-to-case thermal resistance of 146°C/watt (derating factor of 6.85 mW/°C). Junction-to-ambient thermal resistance of 486°C/watt (derating factor of 2.06 mW/°C).

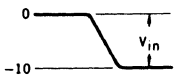
(4) Ratings refer to a high-current point where collector-to-emitter voltage is lowest.

(5) Pulse Conditions: length = 300 μsec; duty cycle = 1%.

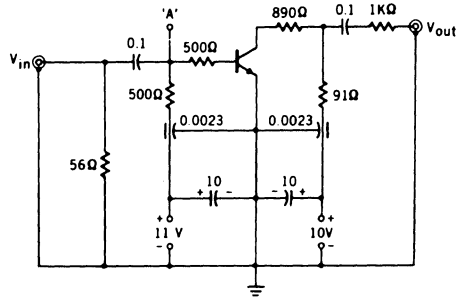
(6) See switching circuits for exact value of I_C, I_{B1}, and I_{B2}.

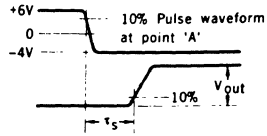
SCHEMATIC

CHARGE STORAGE TIME MEASUREMENT CIRCUIT



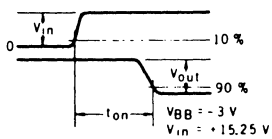
Pulse Generator
V_{in} Rise Time < 1 nsec
Source Impedance = 50Ω
PW ≥ 300 nsec
Duty Cycle < 2 %



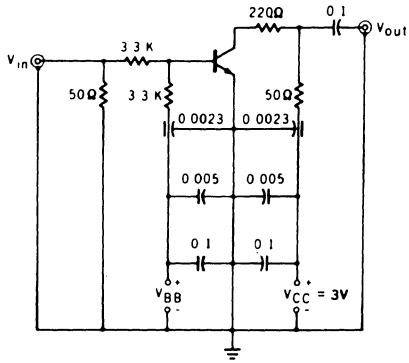


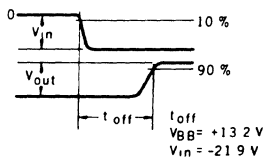
To Sampling Oscilloscope
Input Impedance = 50Ω
Rise Time ≤ 1 nsec

t_{ON} — t_{OFF} MEASUREMENT CIRCUIT



Pulse Generator
V_{in} Rise Time < 1 nsec
Source Impedance = 50Ω
PW ≥ 300 nsec
Duty Cycle < 2 %





To Sampling Oscilloscope
Input Impedance = 50Ω
Rise Time ≤ 1 nsec

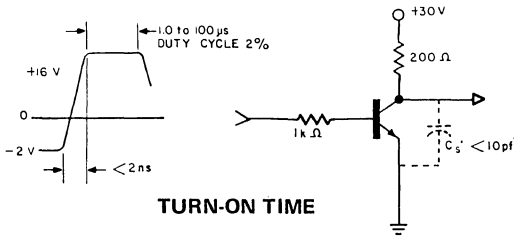
Package: To-92

ABSOLUTE MAXIMUM RATINGS

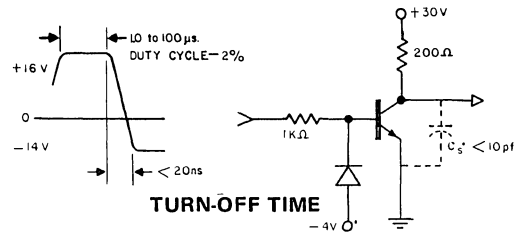
(T_A = 25°C unless otherwise noted)

Characteristic	Unit
Collector-Emitter Voltage	40 Vdc
Collector-Base Voltage	60 Vdc
Emitter-Base Voltage	6.0 Vdc
Collector Current - Continuous	600 mAdc
Total Device Dissipation	
T_A = 25°C	310 mW
Derate above 25°C	2.81 mW/°C
Operating & Storage Junction	
Temperature Range	-55 to +135 °C
Thermal Resistance,	
Junction to Case	0.137 °C/mW
Thermal Resistance,	
Junction to Ambient	0.357 °C/mW

SWITCHING TIME EQUIVALENT TEST CIRCUITS



TURN-ON TIME



TURN-OFF TIME

SCOPE RISE TIME 4ns
*TOTAL SHUNT CAPACITANCE OF TEST JIG, CONNECTORS, AND OSCILLOSCOPE

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Min	Max	Unit	Conditions	
BV_{CEO}*	40	–	Vdc	I_C = 1 mAdc, I_B = 0	
BV_{CBO}	60	–	Vdc	I_C = 0.1 mAdc, I_E = o	
BV_{EBO}	6.0	–	Vdc	I_E = 0.1 mAdc, I_C = 0	
I_{CEX}	–	0.1	*u*Adc	V_{CE} = 35 Vdc, $V_{EB(off)}$ = 0.4 Vdc	
I_{BL}	–	0.1	*u*Adc	V_{CE} = 35 Vdc, $V_{EB(off)}$ = o.4 Vdc	
h_{FE}	20	–	–	I_C = 0.1 mAdc, V_{CE} = 1Vdc	2N4401
	20	–		I_C = 1 mAdc, V_{CE} = 1 Vdc	2N4400
	40	–			2N4401
	40	–		I_C = 10 mAdc, V_{CE} = 1 Vdc	2N4400
	50	–			2N4401
	50	150		I_C = 150 mAdc, V_{CE} = 1 Vdc*	2N4400
	100	300			2N4401
	20	–		I_C = 500 mAdc, V_{CE} = 2 Vdc*	2N4400
	40	–			2N4401
$V_{CE(sat)}$	–	0.4	Vdc	I_C = 150 mAdc, I_B = 15 mAdc	
	–	0.75		I_C = 500 mAdc, I_B = 50 mAdc	
$V_{BE(sat)}$	0.75	0.95	Vdc	I_C = 150 mAdc, I_B = 15 mAdc	
	–	1.2		I_C = 500 mAdc, I_B = 50 mAdc	
f_T	200	–	MHz	I_C = 20 mAdc, V_{CE} = 10 Vdc, f = 100 MHz	2N4400
	250	–			2N4401

*Pulse Test: Pulse Width ≤ 300 us, Duty Cycle ≤ 2%.

ELECTRICAL CHARACTERISTICS ($T_A = 25°C$)

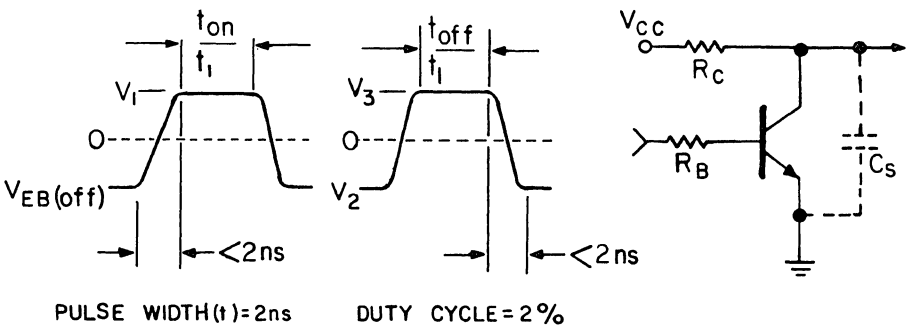
SYMBOL	MIN.	MAX.	UNITS	CONDITIONS	
C_{cb}	–	6.5	pF	V_{CB} = 5 Vdc, I_E = 0, f - 100 kHz, emitter guarded	
C_{eb}	–	30	pF	V_{BE} = 0.5 Vdc, I_C = 0, f = 100 kHz, Collector guarded	
h_{ie}	0.5	7.5	k ohms	I_C = 1 mAdc, V_{CE} = 10 Vdc, f = kHz	2N4400
	1.0	15			2N4401
h_{re}	0.1	8.0	x 10^4	I_C = 1 mAdc, V_{CE} = 10 Vdc, f = 1 kHz	
h_{fe}	20	250	–	I_C = 1 mAdc, V_{CE} = 10 Vdc, f = 1 kHz	2N4400
	40	500			2N4401
h_{oe}	1.0	30	*u*mhoe	I_C = 1 mAdc, V_{CE} = 10 Vdc, f = 1 kHz	
t_d	–	15	ns	V_{CC} = 30 Vdc, $V_{EB(off)}$ = 2 Vdc,	
t_r	–	20	ns	I_C = 150 mAdc, I_{B1} = 15 mAdc	
t_s	–	225	ns	V_{CC} = 30 Vdc, I_C = 150 mAdc,	
t_f	–	30	ns	$I_{B1} = I_{B2}$ = 15 mAdc	

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Characteristic	2N4418	2N4419	Unit
Collector-Emitter Voltage	15	12	Vdc
Collector-Base Voltage	30		Vdc
Emitter-Base Voltage	6.0		Vdc
Collector Current	200		mAdc
Total Device Dissipation @ T_A = 60°C	210		mW
Total Device Dissipation @ T_A = 25°C	310		mW
Derate above 25°C	2.81		mW/°C
Operating and Storage Junction Temperature Range	-55 to +135		°C
Thermal Resistance, Junction to Ambient	0.357		°C/mW

TEST CONDITION	I_C	V_{CC}	R_B	R_C	$C_{S(max)}$	$V_{EB(off)}$	V_1	V_2	V_3
	mA	V	Ω	Ω	pF	V	V	V	V
A	10	3	3300	270	4	−15	10.55	−4.15	10.70
B	10	10	560	960	4	–	–	−4.65	6.55
C	100	10	560	96	12	−2.0	6.35	−4.65	6.55

Figure 1 — Switching Time Equivalent Test Circuit



ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Min	Max	Unit	Conditions	
BV_{CEO}	15	–	Vdc	I_C = 1 mAdc, I_E = 0	2N4418
	12	–			2N4419
BV_{CBO}	30	–	Vdc	I_C = 10 uAdc, I_E = 0	
I_{CEX}	–	100	nAdc	V_{CE} = 12 Vdc, $V_{EB(off)}$ = 0.25 Vdc	
I_{BL}	–	0.1	uAdc	V_{CE} = 12 Vdc, $V_{EB(off)}$ = 0.25 Vdc	
	–	10		V_{CE} = 10 Vdc, $V_{EB(off)}$ = 0.25 Vdc, T_A = 100°C	
h_{FE}	25	–	–	I_C = 1 mAdc, V_{CE} = 1 Vdc	2N4418
	50	–			2N4419
	40	160		I_C = 10 mAdc, V_{CE} = 1 Vdc	2N4418
	100	400			2N4419
	20	–		I_C = 10 mAdc, V_{CE} = 1 Vdc,	2N4418
	45	–		T_A = 55°C	2N4419
	40	–		I_C = 30 mAdc, V_{CE} = 1 Vdc	2N4418
	90	–			2N4419
	30	–		I_C = 100 mAdc, V_{CE} = 1 Vdc	2N4418
	55	–			2N4419
	20	–		I_C = 200 mAdc, V_{CE} = 1 Vdc	2N4418
	35	–			2N4419
$V_{CE(sat)}$	–	0.22	Vdc	I_C = 10 mAdc, I_B = 1 mAdc	
	–	0.35		I_C = 100 mAdc, I_B = 10 mAdc	
$V_{BE(sat)}$	0.65	0.80	Vdc	I_C = 10 mAdc, I_B = 1 mAdc	
	0.75	0.95		I_C = 100 mAdc, I_B = 10 mAdc	
f_T	300	–	MHz	I_C = 10 mAdc, V_{CE} = 10 Vdc, f = 100 MHz	
C_{ob}	–	4.0	pF	V_{CB} = 5 Vdc, I_E = 0, f = 100 kHz	
C_{ib}	–	8.0	pF	V_{BE} = 0.5 Vdc, I_C = 0, f = 100 kHz	
t_{on}	–	25	ns	Turn-On Time	Figure 1, Test Condition A V_{CC} = 3 Vdc, $V_{EB(off)}$ = 1.5 Vdc, I_C = 10 mAdc, I_{B1} = 3 mAdc
t_{off}	–	35	ns	Turn-Off Time	Figure 1, Test Condition A V_{CC} = 3 Vdc, I_C = 10 mAdc, I_{B1} = 3 mAdc, I_{B2} = 1.5 mAdc
t_s	–	20	ns	Storage Time	Figure 1, Test Condition B V_{CC} = 10 Vdc, I_C = 10 mAdc, I_{B1} = I_{B2} = 10 mAdc
t_d	–	8.0	ns	Delay Time	Figure 1, Test Condition C V_{CC} = 10 Vdc, $V_{EB(off)}$ = 2 Vdc,
t_r	–	15	ns	Rise Time	I_C = 100 mAdc, I_{B1} = 10 mAdc
t_s	–	20	ns	Storage Time	Figure 1, Test Condition C V_{CC} = 10 Vdc, I_C = 100 mAdc,
t_f	–	15	ns		I_{B1} = I_{B2} = 10 mAdc
Q_T	–	80	pC	Total Control Charge	V_{CC} = 3 Vdc, I_C = 10 mAdc, I_B = mAdc

HIGH-SPEED NPN SILICON SATURATED SWITCHING TRANSISTORS

ABSOLUTE MAXIMUM RATINGS

Characteristics	Unit
Collector-Base Voltage	40 Vdc
Collector-Emitter Voltage	40 Vdc
Collector-Emitter Voltage Applicable 0. 01-200 mA	15 Vdc
Emitter-Base Voltage	5.0 Vdc
Collector Current	200 mA
Collector Current (10 μs pulse)	500 mA
Total Device Dissipation @ T_A = 25°C	200 mW
Derate above 25°C	2.0 mW/°C
Total Device Dissipation @ T_C = 25°C	500 mW
Derate above 25°C	5.0 mW/°C
Operating Junction Temperature	125 °C
Storage Temperature Range	-55 to +125 °C

FIGURE 1–t_{on} and t_{off} TEST CIRCUIT

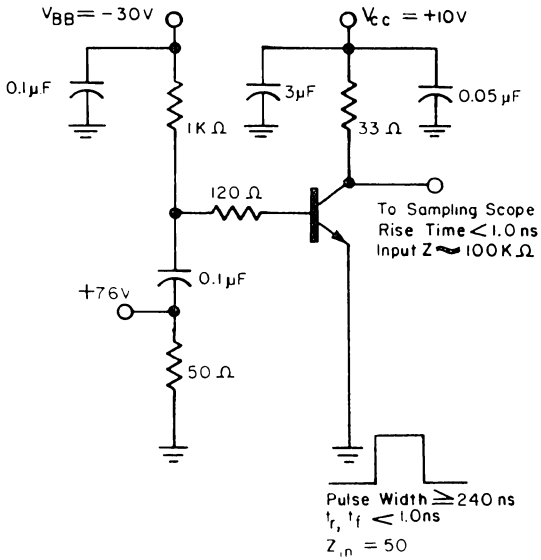
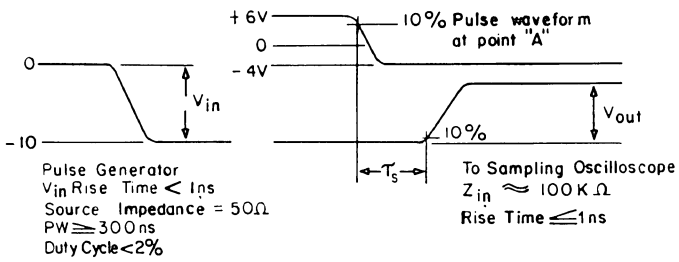
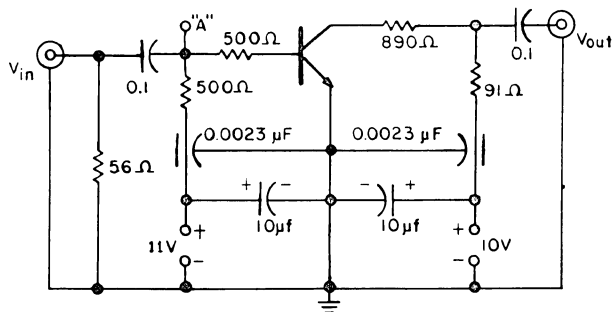


FIGURE 2–CHARGE STORAGE TIME MEASUREMENT CIRCUIT





ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified.)

Symbol	Min	Max	Unit	Conditions
BV_{CBO}	40	–	Vdc	I_C = 100 uAdc, I_E = 0
BV_{CES}	40	–	Vdc	I_C = 100 uAdc, V_{BE} = 0
$V_{CEO(sus)}$*	15	–	Vdc	I_C = 10 mAdc
BV_{EBO}	5.0	–	Vdc	I_E = 100 uAdc, I_C = 0
$V_{CE(sat)}$*	–	0.2	Vdc	I_C = 30 mAdc, I_B = 3.0 mAdc
	–	0.3		I_C = 30 mAdc, I_B = 3.0 mAdc, T_A = +65 C
	–	0.28		I_C = 100 mAdc, I_B = 10 mAdc
	–	0.5		I_C = 300 mAdc, I_B = 30 mAdc
$V_{BE(sat)}$*	0.75	0.95	Vdc	I_C = 30 mAdc, I_B = 3.0 mAdc
	–	1.2		I_C = 100 mAdc, I_B = 10 mAdc
	–	1.7		I_C = 300 mAdc, I_B = 30 mAdc
h_{FE}*	30	120	–	I_C = 30 mAdc, V_{CE} = 0.4 Vdc
	25	–		I_C = 100 mAdc, V_{CE} = 0.5 Vdc
	15	–		I_C = 300 mAdc, V_{CE} = 1.0 Vdc
I_{CES}	–	0.5	uAdc	V_{CE} = 20 Vdc, V_{EB} = 0
	–	3.0		V_{CE} = 20 Vdc, V_{EB} = 0, T_A = +65 C
I_B	–	0.5	uAdc	V_{CE} = 20 Vdc, V_{EB} = 0
C_{ob}	–	5.0	pF	V_{CB} = 5.0 V, I_E = 0, f = 140 kHz
C_{ib}	–	8.0	pF	V_{BE} = 0.5 V, I_C = 0, f = 140 kHz
h_{fe}	3.5	–	–	I_C = 30 mA, V_{CE} = 10 V, f = 100 MHz
t_d	–	10	ns	V_{CC} = +10 V, I_{CS} = 300 mA, I_{B1} = 30 mA, $V_{BE(off)}$ = -3.0 V (Fig. 1)
t_r	–	15	ns	V_{CC} = +10 V, I_{CS} = 300 mA, I_{B1} = 30 mA, $V_{BE(off)}$ = -3.0 V (Fig. 1)
t_{on}	–	18	ns	I_C = 300 mA, I_{B1} = 30 mA, $V_{BE(off)}$ = -3.0 V (Fig. 1)
t_s	–	20	ns	V_{CC} = +10 V, I_{CS} = 300 mA, I_{B1} = 30 mA, I_{B2} = -30 mA (Fig. 1)
t_f	–	15	ns	V_{CC} = +10 V, I_{CS} = 300 mA, I_{B1} = 30 mA, I_{B2} = -30 mA (Fig. 1)
t_{off}	–	28	ns	I_C = 300 mA, I_{B1} = 30 mA, I_{B2} = -30 mA (Fig. 1)
T_S	–	18	ns	I_C = 10 mA, I_{B1} = 10 mA, I_{B2} = -10 mA (Fig. 2)

*Pulse Conditions: PW $\leq$ 300 us; Duty Cycle $\leq$ 1%.

Package: To-92

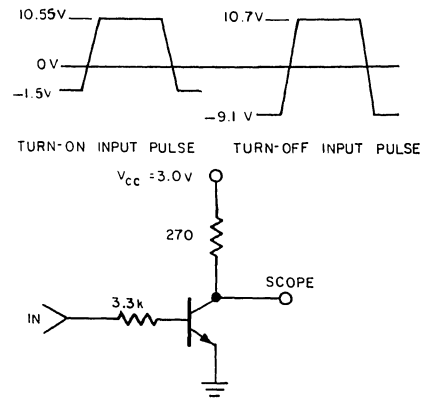
2N5224

GENERAL PURPOSE NPN SILICON LOW-LEVEL SWITCHING TRANSISTOR

ABSOLUTE MAXIMUM RATINGS

Characteristic	Unit
Collector-Emitter Voltage	12 Vdc
Collector-Base Voltage	25 Vdc
Emitter-Base Voltage	5.0 Vdc
Total Device Dissipation @ T_A = 25°C	310 mW
Derate above 25°C	2.81 mW/°C
Operating and Storage Junction Temperature Range	-55 to +135 °C
Thermal Resistance, Junction to Ambient	0.357 °C/mW

Figure 1 — Switching Time Test Circuit



ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Min	Max	Unit	Conditions
BV_{CEO}*	12	—	Vdcq	I_C = 10 mAdc, I_B = 0
BV_{CBO}	25	—	Vdc	I_C = 100 *u*Adc, I_E = 0
BV_{EBO}	5.0	—	Vdc	I_E = 100 *u*Adc, I_C = 0
I_{CBO}	—	500	nAdc	V_{CB} = 15 Vdc, I_E = 0
I_{EBO}	—	100	*u*Adc	V_{BE} = 4.0 Vdc, I_C = 0
h_{FE}	40	400	—	I_C = 10 mAdc, V_{CE} = 1.0 Vdc
	15	—		I_C = 100 mAdc, V_{CE} = 1.0 Vdc
$V_{CE(sat)}$	—	0.35	Vdc	I_C = 10 mAdc, I_B = 3.0 mAdc
$V_{BE(sat)}$	—	0.9	Vdc	I_C = 10 mAdc, I_B = 3.0 mAdc
f_T	250	—	MHz	I_C = 10 mAdc, V_{CE} = 10 Vdc, f = 100 MHz
C_{cb}	—	4.0	pF	V_{CB} = 5.0 Vdc, I_E = 0, f = 1.0 MHz
t_d	—	25	ns	Delay Time See Figure 1
t_r	—	20	ns	Rise Time See Figure 1
t_s	—	35	ns	Storage Time See Figure 1
t_f	—	25	ns	Fall Time See Figure 1

*Pulse Test: Pulse Width = 300 us, Duty Cycle = 2.0%.

HIGH-SPEED NPN SILICON LOW-LEVEL SWITCHING TRANSISTORS

ABSOLUTE MAXIMUM RATINGS

Characteristic	MPS706	MPS706A	Unit
Collector-Emitter Voltage (R_{BE} = 10 Ohms)	20		Vdc
Collector-Base Voltage	25		Vdc
Emitter-Base Voltage	3.0	5.0	Vdc
Total Device Dissipation @ T_A = 25°C	310		mW
Derate above 25°C	2.81		mW/°C
Operating and Storage Junction Temperature Range	-55 to +135		°C

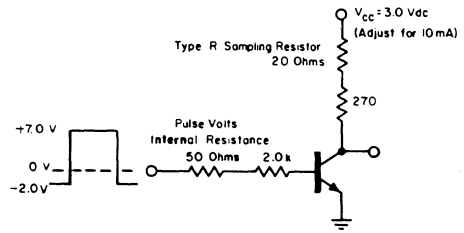


Figure 1 — Switching Time Test Circuit

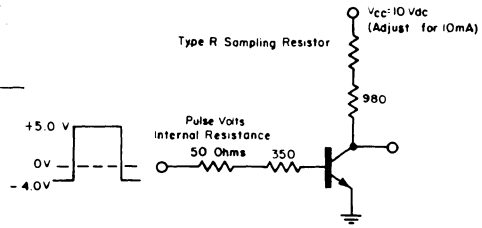


Figure 2 — Storage Time Test Circuit

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Min	Max	Unit	Conditions
BV_{CEO}*	15	–	Vdc	I_C = 10 mAdc, I_B = 0
BV_{CER}	20	–	Vdcq	I_C = 10 mAdc, R_{BE} = 10 Ohms
I_{CBO}	–	0.5	*u*Adc	V_{CB} = 15 Vdc, I_E = 0
I_{EBO}	–	10	*u*Adc	V_{EB} = 3.0 Vdc, I_C = 0
h_{FE}*	20	–	–	I_C = 10 mAdc, V_{CE} = 1.0 Vdc MPS706
	20	60		MPS706A
$V_{CE(sat)}$*	–	0.6	Vdc	I_C = 10 mAdc, I_B = 1.0 mAdc
$V_{BE(sat)}$*	–	0.9	Vdc	I_C = 10 mAdc, I_B = 1.0 mAdc MPS706
	0.7	0.9		MPS706A
f_T	200	–	MHz	I_C = 10 mAdc, V_{CE} = 15 Vdc, f = 100 MHz
C_{ob}	–	6.0	pF	V_{CB} = 10 Vdc, I_E = 0, f = 100 kHz
r_b	–	50	Ohms	I_E = 10 mAdc, V_{CE} = 15 Vdc, f = 300 MHz
t_{on}**	–	40	ns	Turn-On Time See Figure 1
t_{off}**	–	75	ns	Turn-Off Time See Figure 1
T_S**	–	60	ns	Charge Storage Time Constant ** See Figure 2 MPS706
	–	25		MPS706A

*Pulse Test: Pulse Width ≤ 12 ns, Duty Cycle ≤ 2.0%.
**Measured with Tektronix Type R Plug-In (50-Ohm Internal Impedance) and circuits shown.

Package: To-92

HIGH-SPEED NPN SILICON SWITCHING TRANSISTOR

ABSOLUTE MAXIMUM RATINGS

Characteristic	Unit
Collector-Emitter Voltage	30 Vdc
Collector-Base Voltage	40 Vdc
Emitter-Base Voltage	5.0 Vdc
Collector Current	200 mAdc
Total Device Dissipation @ T_A = 25°C	310 mW
Derate above 25°C	2.81 mW/°C
Total Device Dissipation @ T_C = 25°C	500 mW
Derate above 25°C	4.55 mW/°C
Operating and Storage Junction Temperature Range	-55 to +135 °C

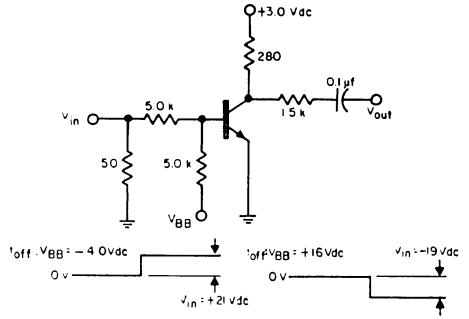


Figure 1 — Turn-On and Turn-Off Time Measurement Circuit

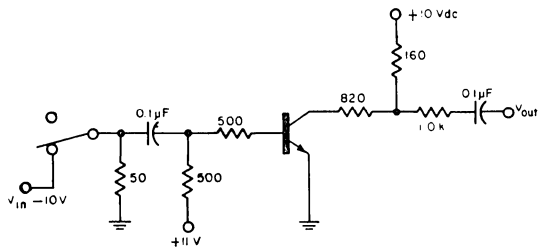


Figure 2 — Charge Storage Time Constant Measurement Circuit

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Min	Max	Unit	Conditions
BV_{CBO}	40	—	Vdc	I_C = 10 uAdc, I_E = 0
BV_{EBO}	5.0	—	Vdc	I_E = 10 uAdc, I_C = 0
I_{CES}	—	10	uAdc	V_{CE} = 30 Vdc, V_{BE} = 0
I_{CBO}	—	0.5	uAdc	V_{CB} = 20 Vdc, I_E = 0
h_{FE}*	25	—	—	I_C = 10 mAdc, V_{CE} = 1.0 Vdc
$V_{CE(sat)}$*	—	0.25	Vdc	I_C = 10 mAdc, I_B = 1.0 mAdc
	—	0.4		I_C = 50 mAdc, I_B = 5.0 mAdc
$V_{BE(sat)}$*	—	0.9	Vdc	I_C = 10 mAdc, I_B = 1.0 mAdc
f_T	350	—	MHz	I_C = 10 mAdc, V_{CE} = 20 Vdc, f = 100 MHz
C_{ob}	—	4.0	pF	V_{CB} = 10 Vdc, I_E = 0, f = 100 kHz
t_{on}	—	16	ns	Turn-On Time I_C = 10 mAdc, I_{B1} = 3.0 mAdc, I_{B2} = 1.0 mAdc See Figure 1
t_{off}	—	30	ns	Turn-Off Time I_C = 10 mAdc, I_{B1} = 3.0 mAdc, I_{B2} = 1.0 mAdc See Figure 1
t_s	—	25	ns	Storage Time I_C = 10 mAdc, I_{B1} = I_{B2} = 10 mAdc See Figure 2

*Pulse Test: Pulse Width ≥ 12 ns, Duty Cycle ≥ 2.0%.

MPS2369

Package: To-92

HIGH-SPEED NPN SILICON SWITCHING TRANSISTOR

ABSOLUTE MAXIMUM RATINGS

Characteristics	Unit
Collector-Emitter Voltage	15 Vdc
Collector-Emitter Voltage	40 Vdc
Collector-Base Voltage	40 Vdc
Emitter-Base Voltage	4.5 Vdc
Collector Current-Peak	500 mAdc
Total Device Dissipation	
@ T_A = 25°C	310 mW
Derate above 25°C	2.81 mW/°C
Operating and Storage Junction	
Temperature Range	-55 to +135 °C
Thermal Resistance, Junction	
to Ambient	0.355 °C/mW

Figure 1 – t_{on} Circuit

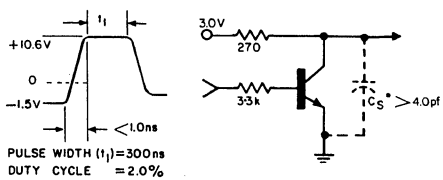


Figure 2 – t_{off} Circuit

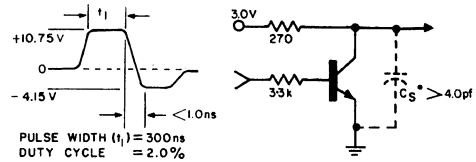
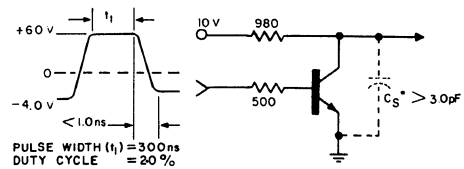


Figure 3 – Storage Test Circuit



*Total shunt capacitance of test jig and connectors

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Min	Max	Unit	Conditions
BV_{CEO}*	15	–	Vdc	I_C = 10 mAdc, I_B = 0
BV_{CES}	40	–	Vdc	I_C = 10 uAdc, V_{BE} = 0
BV_{CBO}	40	–	Vdc	I_C = 10 uAdc, I_E = 0
BV_{EBO}	4.5	–	Vdc	I_E = 10 uAdc, I_C = 0
I_{CBO}	–	0.4	uAdc	V_{CB} = 20 Vdc, I_E = 0
	–	30		V_{CB} = 20 Vdc, I_E = 0, T_A = 125°C
h_{FE}*	40	120	–	I_C = 10 mAdc, V_{CE} = 1.0 Vdc
	20	–		I_C = 10 mAdc, V_{CE} = 1.0 Vdc, T_A = 55°C
	20	–		I_C = 100 mAdc, V_{CE} = 2.0 Vdc
$V_{CE(sat)}$	–	0.25	Vdc	I_C = 10 mAdc, I_B = 1.0 mAdc
$V_{BE(sat)}$*	0.70	0.85	Vdc	I_C = 10 mAdc, I_B = 1.0 mAdc
C_{ob}	–	4.0	pF	V_{CB} = 5.0 Vdc, I_E = 0, f = 140 kHz
h_{fe}	5.0	–	–	I_C = 10 mAdc, V_{CE} = 10 Vdc, f = 100 MHz
t_{on}	–	12	ns	V_{CC} = 3.0 Vdc, $V_{BE(off)}$ = 1.5 Vdc, I_C = 10 mAdc, I_{B1} = 3.0 mAdc Figure 1
t_{off}	–	18	ns	V_{CC} = 3.0 Vdc, I_C = 10 mAdc, I_{B1} = 3.0 mAdc, I_{B2} = 1.5 mAdc Figure 2
t_s	–	13	ns	I_{B1} = I_{B2} = I_C = 10 mAdc Figure 3

*Pulse Test: Pulse Width = 300 us, Duty Cycle = 2.0%.

MPS2713, MPS2714

GENERAL PURPOSE LOW-LEVEL NPN SILICON SWITCHING TRANSISTOR

ABSOLUTE MAXIMUM RATINGS

Characteristic	Unit
Collector-Base Voltage	18 Vdc
Collector-Emitter Voltage	18 Vdc
Emitter-Base Voltage	5.0 Vdc
Collector Current	200 mAdc
Total Device Dissipation @ T_A = 60°C	210 mW
Total Device Dissipation @ T_A = 25°C	310 mW
Derate above 25°C	2.81 mW/°C
Thermal Resistance, Junction to Ambient	0.357 °C/mW
Junction Operating Temperature	135 °C
Storage Temperature Range	-55 to +135 °C

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Min	Typ	Max	Unit	Conditions
I_{CBO}	–	–	0.5	uAdc	V_{CB} = 18 Vdc, I_E = 0
	–	–	15		V_{CB} = 18 Vdc, I_E = 0, T_A = 100°C
I_{EBO}	–	–	0.5	uAdc	V_{EB} = 5 Vdc, I_C = 0
h_{FE}	30	60	90	–	I_C = 2 mAdc, V_{CE} = 4.5 Vdc MPS2713
	75	150	225		MPS2714
$V_{CE(sat)}$	–	0.16	0.3	Vdc	I_C = 50 mAdc, I_B = 3 mAdc
$V_{BE(sat)}$	0.6	0.75	1.3	Vdc	I_C = 50 mAdc, I_B = 3 mAdc
h_{fe}	30	–	120	–	I_C = 2 mAdc, V_{CE} = 4.5 Vdc, f = 1 kHz MPS2713
	80	–	300		MPS2714
f_T	–	250	–	MHz	I_C = 10 mAdc, V_{CE} = 10 Vdc, f = 100 MHz
C_{ob}	–	2.5	–	pF	V_{CB} = 10 Vdc, I_E = 0, f = 100 kHz
h_{ie}	–	3000	–	ohms	I_C = 0.5 mAdc, V_{CE} = 1 Vdc, f = 1 kHz
t_d	–	7.0	–	ns	Delay Time I_C = 10 mA, I_{B1} = 3 mA,
t_r	–	6.0	–	ns	Rise Time V_{CC} = 10 V
t_s	–	12	–	ns	Storage Time I_C = 10 mA, I_{B1} = 3 mA,
t_f	–	9.0	–	ns	Fall Time I_{B2} = 1 mA, V_{CC} = 10 V

MPS3646

Package: To-92

HIGH-SPEED NPN SILICON SATURATED SWITCHING TRANSISTOR

ABSOLUTE MAXIMUM RATINGS

Characteristic	Unit
Collector-Base Voltage	40 Vdc
Collector-Emitter Voltage	40 Vdc
Collector-Emitter Voltage Applicable 0. 01-200 mA	15 Vdc
Emitter-Base Voltage	5.0 Vdc
Collector Current	200 mA
Collector Current (10 us pulse)	500 mA
Total Device Dissipation @ T_A = 25°C	200 mW
Derate above 25°C	2.0 mW/°C
Total Device Dissipation @ T_A = 25°C	500 mW
Derate above 25°C	5.0 mW/°C
Operating Junction Temperature	125 °C
Storage Temperature Range	-55 to +125 °C

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified.)

Symbol	Min	Max	Unit	Conditions
BV_{CBO}	40	–	Vdc	I_C = 100 uAdc, I_E = 0
BV_{CES}	40	–	Vdc	I_C = 100 uAdc, V_{BE} = 0
$V_{CEO(sus)}$*	15	–	Vdc	I_C = 10 mAdc
BV_{EBO}	5.0	–	Vdc	I_E = 100 uAdc, I_C = 0
$V_{CE(sat)}$*	–	0.2	Vdc	I_C = 30 mAdc, I_B = 3.0 mAdc
	–	0.3		I_C = 30 mAdc, I_B = 3.0 mAdc, T_A = +65 C
	–	0.28		I_C = 100 mAdc, I_B = 10 mAdc
	–	0.5		I_C = 300 mAdc, I_B = 30 mAdc
$V_{BE(sat)}$*	0.75	0.95	Vdc	I_C = 30 mAdc, I_B = 3.0 mAdc
	–	1.2		I_C = 100 mAdc, I_B = 10 mAdc
	–	1.7		I_C = 300 mAdc, I_B = 30 mAdc
h_{FE}*	30	120	–	I_C = 30 mAdc, V_{CE} = 0.4 Vdc
	25	–		I_C = 100 mAdc, V_{CE} = 0.5 Vdc
	15	–		I_C = 300 mAdc, V_{CE} = 1.0 Vdc
I_{CES}	–	0.5	uAdc	V_{CE} = 20 Vdc, V_{EB} = 0
	–	3.0		V_{CE} = 20 Vdc, V_{EB} = 0, T_A = +65 C
I_B	–	0.5	uAdc	V_{CE} = 20 Vdc, V_{EB} = 0
C_{ob}	–	5.0	pF	V_{CB} = 5.0 V, I_E = 0, f = 140 kHz
C_{ib}	–	8.0	pF	V_{BE} = 0.5 V, I_C = 0, f = 140 kHz
h_{fe}	3.5	–	–	I_C = 30 mA, V_{CE} = 10 V, f = 100 MHz
t_d	–	10	ns	V_{CC} = +10 V, I_{CS} = 300 mA, I_{B1} = 30 mA, $V_{BE(off)}$ = -3.0 V (Fig. 1)
t_r	–	15	ns	V_{CC} = +10 V, I_{CS} = 300 mA, I_{B1} = 30 mA, $V_{BE(off)}$ = -3.0 V (Fig. 1)
t_{on}	–	18	ns	I_C = 300 mA, I_{B1} = 30 mA, $V_{BE(off)}$ = -3.0 V (Fig. 1)
t_s	–	20	ns	V_{CC} = +10 V, I_{CS} = 300 mA, I_{B1} = 30 mA, I_{B2} = -30 mA (Fig. 1)
t_f	–	15	ns	V_{CC} = +10 V, I_{CS} = 300 mA, I_{B1} = 30 mA, I_{B2} = -30 mA (Fig. 1)
t_{off}	–	28	ns	I_C = 300 mA, I_{B1} = 30 mA, I_{B2} = -30 mA (Fig. 1)
T_S	–	18	ns	I_C = 10 mA, I_{B1} = 10 mA, I_{B2} = -10 mA (Fig. 2)

*Pulse Conditions: PW ≤ 300 us; Duty Cycle ≤ 1%.

Figure 1 – t_{on} and t_{off} Test Circuit

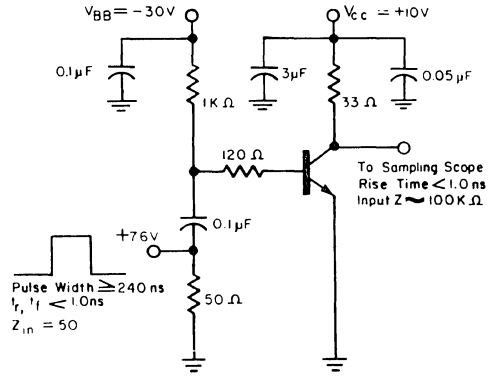
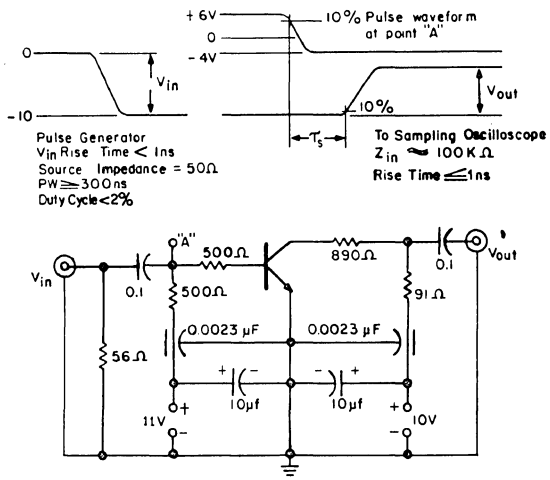


Figure 2 – Charge Storage Time Measurement Circuit



2N2205, 2N2206 Ⓕ

HIGH-SPEED NPN SILICON SWITCHING TRANSISTORS

Packages:
2N2205, TO-18
2N2206, TO-46

ABSOLUTE MAXIMUM RATINGS (Note 1)

Characteristics	Unit
Storage Temperature	−65°C to +300°C
Operating Junction Temperature	−65°C to +175°C
Lead Temperature (Soldering, 10 sec time limit)	+235°C
Total Device Dissipation	
@ T_C = 25°C (Notes 2 and 3)	1.0 Watt
@ T_A = 25°C (Notes 2 and 3)	0.3 Watt
V_{CBO} Collector-Base Voltage	25 Volts
V_{CEO} Collector-Emitter Voltage (Note 4)	12 Volts
V_{EBO} Emitter-Base Voltage	3.0 Volts
I_C Collector Current	200 mA

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Min	Max	Unit	Conditions
h_{FE}	20	–	–	(2N2205) I_C = 10 mA, V_{CE} = 1.0 Volt
	40	120	–	(2N2206)
$V_{BE(sat)}$	0.7	0.9	Volt	(2N2205) I_C = 10 mA, I_B = 1.0 mA
	0.7	0.9	Volt	(2N2206)
$V_{CE(sat)}$	–	0.22	Volt	(2N2205) I_C = 10 mA, I_B = 1.0 mA
	–	0.22	Volt	(2N2206)
$V_{CE(sat)}$	–	0.35	Volt	(2N2205) I_C = 50 mA, I_B = 5.0 mA
	–	0.35	Volt	(2N2206)
h_{fe}	2.0	–	–	(2N2205) I_C = 10 mA, V_{CE} = 10 Volts
	2.0	–	–	(2N2206)
C_{obo}	–	6.0	pf	(2N2205) I_E = 0, V_{CB} = 10 Volts
	–	6.0	pf	(2N2206)
I_{CBO}	–	0.025	μA	(2N2205) I_E = 0, V_{CB} = 15 Volts
	–	0.025	μA	(2N2206)
I_{CBO}(150°C)	–	15	μA	(2N2205) I_E = 0, V_{CB} = 15 Volts
	–	15	μA	(2N2206)
I_{CEX}	–	15	μA	(2N2205) V_{CE} = 10 Volts, V_{BE} = 0.25 Volt
	–	15	μA	(2N2206)

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Min	Max	Unit	Conditions
I_{EBO}	–	100	μA	(2N2205) I_C = 0, V_{EB} = 3.0 Volts
	–	100	μA	(2N2206)
BV_{CBO}	25	–	Volts	(2N2205) I_E = 0, I_C = 100μA
	25	–	Volts	(2N2206)
V_{CEO}	12	–	Volts	(2N2205) I_B = 0, I_C = 10 mA (pulsed)
	12	–	Volts	(2N2206) (Notes 4 and 5)
BV_{EBO}	3.0	–	Volts	(2N2205) I_C = 0, I_E = 100μA
	3.0	–	Volts	(2N2206)
τ_s	–	25	nsec	(2N2205) $I_C \approx 10$ mA, $I_{B1} \approx 10$ mA,
	–	35	nsec	(2N2206) $I_{B2} \approx -10$ mA (Note 6)
t_{on}	–	40	nsec	(2N2205) $I_C \approx 10$ mA, $I_{B1} \approx 3.0$ mA,
	–	40	nsec	(2N2206) $I_{B2} \approx -1.0$ mA (Note 7)
t_{off}	–	75	nsec	(2N2205) $I_C \approx 10$ mA, $I_{B1} \approx 3.0$ mA,
	–	75	nsec	(2N2206) $I_{B2} \approx -1.0$ mA (Note 7)

NOTES:

(1) These ratings are limiting values above which the serviceability of any individual semiconductor device may be impaired.

(2) These are steady state limits. The factory should be consulted on applications involving pulsed or low duty cycle operations.

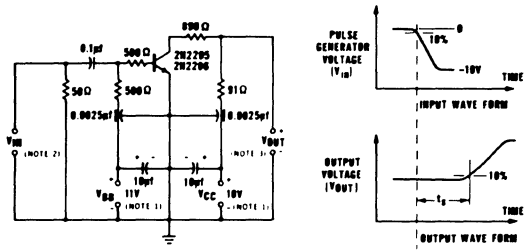
(3) These ratings give a maximum junction temperature of 175°C and junction-to-case thermal resistance of 150°C/Watt (derating factor of 6.7 mW/°C); junction-to-ambient thermal resistance of 500°C/Watt (derating factor of 2.0 mW/°C).

(4) Rating refers to a high-current point where collector-to-emitter voltage is lowest.

(5) Pulse Conditions: length <6 msec; duty cycle <30%.

(6) See Fig. 1 for exact value of I_C, I_{B1}, and I_{B2}.

(7) See Fig. 2 for exact value of I_C, I_{B1}, and I_{B2}.



NOTES:

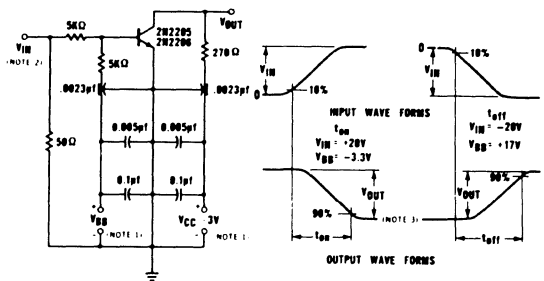
(1) With certain types of power supplies, it may be necessary to connect 25-μf decoupling capacitors across the power-supply terminals for V_{CC} and V_{BB}

(2) Input voltage (V_{IN}) obtained from a pulse generator having an output impedance of 50 ohms. V_{IN} rise time <1 nsec; pulse duration >300 nsec, and duty factor <2%

(3) Input and output waveforms, shown above, monitored by means of a sampling oscilloscope or other indicating device having rise time <0 5 nsec, input capacitance of probe <2.5 pf with shunt resistance >1000 ohms.

FIGURE 1

CIRCUIT USED TO MEASURE STORAGE TIME (t_s).



NOTES:

(1) With certain types of power supplies, it may be necessary to connect 25-μf decoupling capacitors across the power-supply terminals for V_{CC} and V_{BB}

(2) Input voltage (V_{IN}) obtained from a pulse generator having an output impedance of 50 ohms. V_{IN} rise time <1 nsec; pulse duration >300 nsec, and duty factor <2%.

(3) Input and output waveforms, shown above, monitored by means of a sampling oscilloscope or other indicating device having rise time <0 5 nsec, input capacitance of probe <2.5 pf with shunt resistance >3000 ohms.

FIGURE 2

CIRCUIT USED TO MEASURE "TURN-ON" TIME (t_{on}) AND "TURN-OFF" TIME (t_{off}).

PNP MEDIUM FREQUENCY AMPLIFIER SILICON TRANSISTOR

ABSOLUTE MAXIMUM RATINGS (Note 1)

Characteristics	Unit
Collector-Base Voltage	−50 Volts
Collector-Emitter Voltage ($R_{BE} \leq 10$ ohms) (Note 4)	−50 Volts
Collector-Emitter Voltage (Note 4)	−35 Volts
Emitter-Base Voltage	−5.0 Volts
Total Dissipation @ :	
T_C = 25°C (Notes 2 and 3)	2.0 Watts
T_C = 100°C (Notes 2 and 3)	1.0 Watt
T_A = 25°C	0.6 Watt
Storage Temperature	−65°C to +200°C
Operating Junction Temperature	175°C Maximum

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Min	Max	Unit	Conditions
h_{FE}	75	200	-	I_C = −150 mA, V_{CE} = −10 Volts (Note 5)
h_{FE}	75	-	-	I_C = −5.0 mA, V_{CE} = −10 Volts (Note 5)
$V_{BE(sat)}$	-	−1.3	Volts	I_C = −150 mA, I_B = −15 mA
$V_{CE(sat)}$	-	−1.5	Volts	I_C = −150 mA, I_B = −15 mA
h_{fe}	3.0	-	-	I_C = −50 mA, V_{CE} = −10 Volts, f = 20mHz
C_{ob}	-	45	pF	I_E = 0, V_{CB} = −10 Volts
I_{CBO}	-	1.0	μA	I_E = 0, V_{CB} = −30 Volts
$I_{CBO(150°C)}$	-	100	μA	I_E = 0, V_{CB} = −30 Volts
$V_{CER(sust)}$	−50	-	Volts	I_C = −100 mA, $R_{BE} \leq 10$ ohms
$V_{CEO(sust)}$	−35	-	Volts	I_C = −100 mA, I_B = 0

NOTES:

(1) These ratings are limiting values above which the serviceability of any semiconductor device may be impaired.

(2) These are steady state limits. The factory should be consulted on applications involving pulsed or low duty cycle operations.

(3) These ratings give a maximum junction temperature of 175°C and junction-to-case thermal resistance of 75°C/watt (derating factor of 13.3 mW/°C).

(4) Rating refers to a high-current point where collector-to-emitter voltage is lowest.

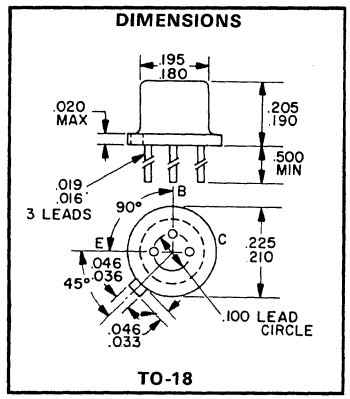
(5) Pulse Conditions: length = 300 usec; duty cycle = 1%.

2N2894 2N3209 Ⓕ

SILICON SWITCHING TRANSISTORS

HIGH SPEED PNP SILICON PLANAR EPITAXIAL SATURATED SWITCH AND RF AMPLIFIER

- **Fast t_{on} : 23 nsec typ. @ 30 mA**
- **Fast t_{off} : 34 nsec typ. @ 30 mA**
- **High f_T : 600 MHz typ.**
- **Low saturation : 0.25V typ. V_{CE} @ 100 mA**
- **Low C_{ob} : 3.3pF typ. @ 5V**



TO-18

The ITT 2N2894 and 2N3209 are PNP diffused silicon planar epitaxial transistors designed for saturated and non-saturated switching at high currents. Both are ideal for RF and IF applications, and 100 MHz oscillator converter circuits.

ABSOLUTE MAXIMUM RATINGS

CHARACTERISTICS	2N2894	2N3209	UNITS
Collector-to-Base Voltage	−12	−20	Volts
Collector-to-Emitter Voltage (open base)	−12	−20	Volts
Emitter-to-Base Voltage	−4	−4	Volts
Collector Current (10 μsec pulse)	200	200	mA
Junction Temperature (op. and stg.)	−65 to 200		°C
Total Power Dissipation @ T_C = 25°C	1.2	1.2	Watts
(derate 6.8mW/°C above 25°C)			
@ T_C = 100°C	0.72	0.68	Watts
Total Power Dissipation @ T_A = 25°C	0.36	0.36	Watts
(derate 2.06mW/°C above 25°C)			

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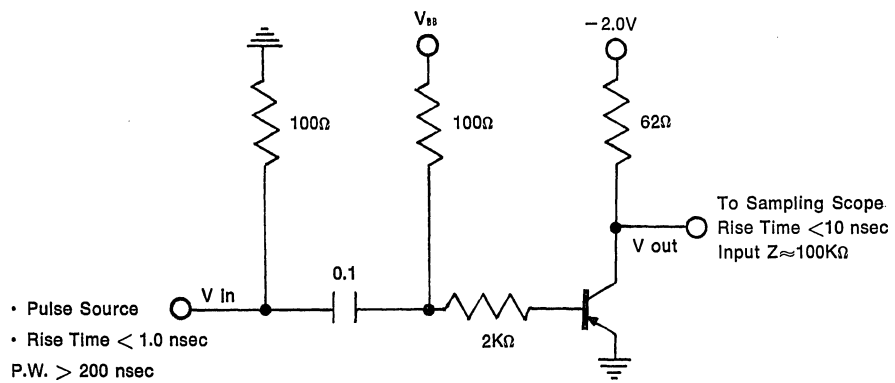
ELECTRICAL CHARACTERISTICS @ 25°C unless otherwise noted.

	2N2894			2N3209				
SYMBOL	**MIN.**	**TYP.**	**MAX.**	**MIN.**	**TYP.**	**MAX.**	**UNIT**	**CONDITIONS**
BV_{CBO}	−12			−20			Vdc	$I_C = 10\mu A$
BV_{CES}				−20			Vdc	$I_C = 10\mu A$
LV_{CEO} [1, 2]	**−12**			**−20**			**Vdc**	**$I_C = 10mA$**
BV_{EBO}	−4.0			−4.0			Vdc	$I_E = 100\mu A$
h_{FE} [1]	40	75	150	30	75	120		$I_C = 30mA$ $V_{CE} = -0.5V$
	30	55		25	67			$I_C = 10mA$ $V_{CE} = -0.3V$
	25			15	30			$I_C = 100mA$ $V_{CE} = -1.0V$
	17	43		12	43			$I_C = 30mA$ $V_{CE} = -0.5V$ $T_A = -55°C$
V_{CE} (sat)[1]		**−0.07**	**−0.15**		**−0.07**	**−0.15**	Vdc	$I_C = 10mA$ $I_B = 1.0mA$
		−0.10	**−0.20**		**−0.10**	**−0.20**	Vdc	$I_C = 30mA$ $I_B = 3.0mA$
		−0.25	**−0.50**		**−0.28**	**−0.60**	**Vdc**	**$I_C = 100mA$ $I_B = 10mA$**
V_{BE} (sat)[1]	−0.78	−0.92	−0.98	−0.78	−0.92	−0.98	Vdc	$I_C = 10mA$ $I_B = 1.0mA$
	−0.85	−1.10	−1.20	−0.85	−1.10	−1.20	Vdc	$I_C = 30mA$ $I_B = 3.0mA$
		−1.40	−1.70		−1.40	−1.70	Vdc	$I_C = 100mA$ $I_B = 10mA$
I_{CES}		0.05	80		0.05	80	nA	$V_{CE} = -6V$ and $-10V$ respectively
I_{CBO}		0.025	10		0.025	10	μA	Same as above $T_A = 125°C$
C_{ob}		**3.3**	**6.0**		**3.0**	**5.0**	**pF**	**$V_{CB} = -5.0V$**
C_{ib}		3.8	6.0		3.8	6.0	pF	$V_{EB} = -0.5V$
h_{fe}	4.0	**5.5**		4.0	5.5			**$I_C = 30mA$ $V_{CE} = -10V$ $f = 100MHz$**
t_{on}		**23**	**60**		**23**	**60**	**nsec**	**$I_C \approx 30mA$ $I_{B1} \approx 1.5mA$**
t_{off}		**34**	**90**		**34**	**90**	**nsec**	**$I_C \approx 30mA$ $I_{B1} \approx 1.5mA$ $I_{B2} \approx 1.5mA$**

NOTES: 1. Pulsed measurement: width $\leq 300\ \mu sec$, duty cycle $\leq 2\%$.
2. Rating is where collector to emitter voltage is lowest.

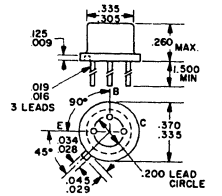
$t_{on} - t_{off}$ TEST CIRCUIT



t_{on}	t_{off}
$V_{CC} = -2.0V$	$V_{CC} = -2.0V$
$V_{BB} = 3.0V$	$V_{BB} = -4.0V$
$V_{in} = -7.0V$	$V_{in} = +6.0V$

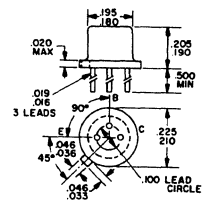
GENERAL PURPOSE PNP SILICON PLANAR EPITAXIAL TRANSISTORS

DIMENSIONS
2N2904A, 5A



TO-5

DIMENSIONS
2N2906A, 7A



TO-18

- **High Voltage: −60V min.**
- **Low V_{CE} (sat): 0.4V @ 150 mA**
- **h_{FE} guaranteed from 100 μA to 500mA**

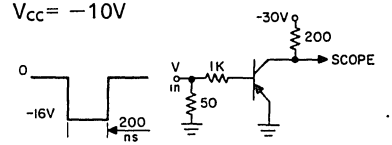
The ITT 2N2904A-7A are PNP silicon planar epitaxial general purpose transistors for applications at current ranges from 0.1 to 500 mA. Low saturation voltage and fast switching times make the 2N2904A, 5A ideal for core driving. The flat gain over a wide current range gives good linearity in amplifier circuits. High breakdown voltage allows large signal swing in switching and amplifier circuits. Designed to complement the ITT 2N2217 thru 2N2222 NPN types.

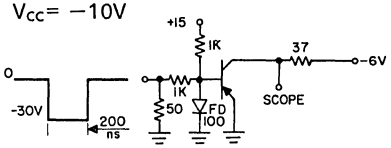
ABSOLUTE MAXIMUM RATINGS

CHARACTERISTICS	2N2904A 2N2905A	2N2906A 2N2907A	UNITS
Collector-to-Base Voltage	−60	−60	Volts
Collector-to-Emitter Voltage (open base)	−60	−60	Volts
Emitter-to-Base Voltage	−5	−5	Volts
Collector Current (continuous)	600	600	mA
Junction Temperature (storage)	−65 to 200		°C
Total Power Dissipation @ T_C=25°C	3.0	1.8	Watts
Derating factor above 25°C	17.3	10.3	mW/°C
Total Power Dissipation @ T_A=25°C	0.6	0.4	Watts
Derating factor above 25°C	3.43	2.28	mW/°C

ELECTRICAL CHARACTERISTICS @ 25°C unless otherwise noted.

SYMBOL	2N2904A 2N2906A MIN.	2N2904A 2N2906A MAX.	2N2905A 2N2907A MIN.	2N2905A 2N2907A MAX.	UNIT	CONDITIONS	
BV_{CBO}	−60		−60		Vdc	I_C= −10μA	
LV_{CEO}[1,2]	−60		−60		Vdc	I_C= −10mA	
BV_{EBO}	−5		−5		Vdc	I_E= −10μA	
h_{FE}[1]	40		75			I_C= −100μA	V_{CE}= −10V
	40		100			I_C= −1mA	V_{CE}= −10V
	40		100			I_C= −10mA	V_{CE}= −10V
	40	120	100	300		I_C= −150mA	V_{CE}= −10V
	40		50			I_C= −500mA	V_{CE}= −10V
$V_{CE}(sat)$[1]		−0.4		−0.4	Vdc	I_C= −150mA	I_B= −15mA
		−1.6		−1.6	Vdc	I_C= −500mA	I_B= −50mA
$V_{BE}(sat)$[1]		−1.3		−1.3	Vdc	I_C= −150mA	I_B= −15mA
		−2.6		−2.6	Vdc	I_C= −500mA	I_B= −50mA
I_{CBO}		10		10	nA	V_{CB}= −50V	
		10		10	μA	V_{CB}= −50V	T_A=150°C
I_{CEX}		50		50	nA	V_{CE}= −30V	V_{BE}=0.5V
I_B		50		50	nA	V_{CE}= −30V	V_{BE}=0.5V
C_{ob}		8		8	pF	V_{CB}= −10V	f=100KHz
C_{ib}		30		30	pF	V_{EB}= −2V	f=100KHz
h_{fe}	2		2			I_C= −50mA f=100MHz	V_{CE}= −20V
t_d		10		10	ns	I_C= −150mA V_{CC}= −10V	I_{B1}= −15mA
t_r		40		40	ns		
t_s				80	ns	I_C= −150mA V_{CC}= −10V	I_{B1}=I_{B2} =15mA
t_f				30	ns		





Notes: 1. Pulsed width ≤300 μsec; duty cycle ≤2%.
2. Lowest emitter to collector voltage.

2N3012Ⓕ

HIGH-SPEED PNP SILICON SWITCHING AND RF AMPLIFIER TRANSISTOR

Package: TO-18

The ITT 2N3012 is a 600 mc PNP silicon planar epitaxial transistor designed for saturated and non-saturated switching circuits requiring up to 200 milliamperes of collector current. It is suitable for 20 mc amplifiers, 10.7 mc IF amplifiers, and 100 mc oscillator converter circuits.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Characteristics	Unit
Collector-Base Voltage	−12 Volts
Collector-Emitter Voltage (Note 4)	−12 Volts
Collector-Emitter Voltage	−12 Volts
Emitter-Base Voltage	−4.0 Volts
Total Dissipation @:	
T_C = 25°C (Notes 2 and 3)	1.2 Watts
T_A = 25°C (Notes 2 and 3)	0.36 Watt
Storage Temperature	−65°C to +200 °C
Operating Junction Temperature	200°C Maximum
Lead Temperature (Soldering, 60 sec Time Limit)	300°C Maximum

SCHEMATIC

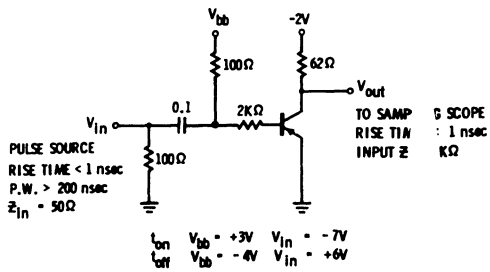


FIGURE 1 – SWITCHING TIME TEST CIRCUI

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Min	Typ	Max	Unit	Conditions
h_{FE}	30	70	120	–	I_C = 30 mA, V_{CE} = −0.5 Volt (Note 5)
h_{FE}	25	50	–	–	I_C = 10 mA, V_{CE} = −0.3 Volt (Note 5)
h_{FE}	20	40	–	–	I_C = 100 mA, V_{CE} = −1.0 Volt (Note 5)
$V_{CE(sat)}$	–	−0.07	−0.15	Volt	I_C = 10 mA, I_B = 1.0 mA
$V_{CE(sat)}$	–	−0.1	−0.2	Volt	I_C = 30 mA, I_B = 3.0 mA
$V_{CE(sat)}$	–	−0.15	−0.4	Volt	I_C = 30 mA, I_B = 3.0 mA
$V_{CE(sat)}$	–	−0.25	−0.5	Volt	I_C = 100 mA, I_B = 10 mA
$V_{BE(sat)}$	−0.78	−0.90	−0.98	Volt	I_C = 10 mA, I_B = 1.0 mA
$V_{BE(sat)}$	−0.85	−1.12	−1.2	Volts	I_C = 30 mA, I_B = 3.0 mA
$V_{BE(sat)}$	–	−1.4	−1.7	Volts	I_C = 100 mA, I_B = 10 mA
h_{fe}	4.0	5.5	–	–	I_C = 30 mA, V_{CE} = −10 Volts
C_{ob}	–	3.3	6.0	pf	I_E = 0, V_{CB} = −5.0 Volts
C_{TE}	–	3.8	6.0	pf	I_C = 0, V_{EB} = −0.5 Volt

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Min	Typ	Max	Unit	Conditions
I_{CES}	–	0.05	80	nA	V_{CE} = −6.0 Volts, V_{BE} = 0
I_{CES}(85°C)	–	0.003	5.0	μA	V_{CE} = −6.0 Volts, V_{BE} = 0
BV_{CBO}	−12	–	–	Volts	I_C = 10 μA, I_E = 0
BV_{CES}	−12	–	–	Volts	I_C = 10 μA, I_E = 0
$V_{CEO(sust)}$	−12	–	–	Volts	I_C = 10 mA (pulsed), I_B = 0 (Notes 4 and 5)
BV_{EBO}	−4.0	–	–	Volts	I_E = 100 μA, I_C = 0
t_{on}	–	25	60	nsec	$I_C \approx$ 30 mA, I_{B1} ≈ 1.5 mA (Note 6)
t_{off}	–	35	75	nsec	$I_C \approx$ 30 mA, $I_{B1} \approx$ 1.5 mA, $I_{B2} \approx$ −1.5 mA (Note 6)

NOTES:

(1) These ratings are limiting values above which the serviceability of any individual semiconductor device may be impaired.

(2) These are steady state limits. The factory should be consulted on applications involving pulsed or low duty cycle operations.

(3) These ratings give a maximum junction temperature of 200°C and junction-to-case thermal resistance of 146°C/watt (derating factor of 6.85 mW/°C); junction-to-ambient thermal resistance of 486°C/watt (derating factor of 2.06 mW/°C).

(4) Rating refers to a high-current point where collector-to-emitter voltage is lowest.

(5) Pulse Conditions: length = 300 μsec; duty cycle = 1%.

(6) See switching circuit for exact values of I_C, I_{B1}, and I_{B2}.

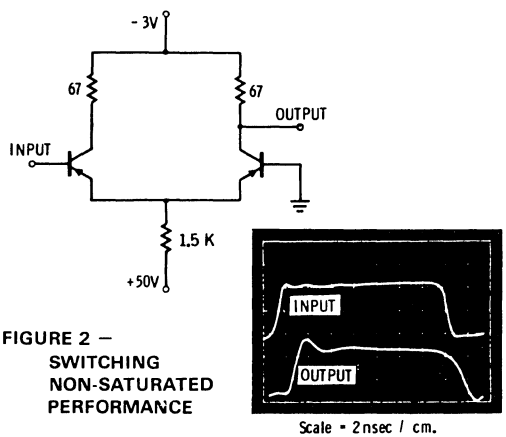


FIGURE 2 – SWITCHING NON-SATURATED PERFORMANCE

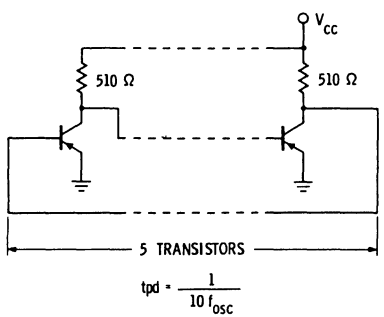


FIGURE 3 – FIVE STAGE RING OSCILLATOR FOR MEASUREMENT OF PROPAGATION DELAY

2N3502, 2N3503, 2N3504, 2N3505Ⓕ

PNP SILICON HIGH CURRENT SWITCHING TRANSISTORS

Packages:
2N3502/03, TO-5
2N3504/05, TO-18

These ITT PNP silicon planar epitaxial transistors are designed for digital and analog applications at current levels up to 500 milliamperes. Their high beta, high f_T at high current, high LV_{CEO}, and low noise figure make them ideal for use as line drivers, memory applications and low-noise amplifiers.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Characteristics	Unit
Storage Temperature	−65°C to +200°C
Operating Junction Temperature	200°C Maximum
Total Device Dissipation @:	
T_C = 25°C (Notes 2 and 3)	
(2N3502, 2N3503)	3.0 Watts
(2N3504, 2N3505)	1.3 Watts
T_A = 25°C (Notes 2 and 3)	
(2N3502, 2N3503)	0.7 Watt
(2N3504, 2N3505)	0.4 Watt
Collector-Base Voltage	
(2N3503, 2N3505)	−60 Volts
(2N3502, 2N3504)	−45 Volts
Collector-Emitter Voltage (Note 4)	
(2N3503, 2N3505)	−60 Volts
(2N3502, 2N3504)	−45 Volts
Emitter-Base Voltage	
(2N3503, 2N3505)	−5.0 Volts
(2N3502, 2N3504)	−5.0 Volts
Collector Current (Note 2)	
(2N3502, 2N3503, 2N3504, 2N3505)	600 mA

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol		Min	Typ	Max	Unit	Conditions
h_{FE}	2N3503, 2N3505, 2N3502, 2N3504	80	120	-	-	I_C = 10μA, V_{CE} = −10 Volts
h_{FE}	2N3503, 2N3505, 2N3502, 2N3504	120	-	-	-	I_C = 100μA, V_{CE} = −10 Volts
h_{FE}	2N3503, 2N3505, 2N3502, 2N3504	135	200	-	-	I_C = 1.0 mA, V_{CE} = −10 Volts
h_{FE}	2N3503, 2N3505, 2N3502, 2N3504	140	270	-	-	I_C = 10 mA, V_{CE} = −10 Volts (Note 5)
h_{FE}	2N3503, 2N3505, 2N3502, 2N3504	100	150	300	-	I_C = 150 mA, V_{CE} = −10 Volts (Note 5)

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol		Min	Typ	Max	Unit	Conditions
h_{FE}	2N3503, 2N3505, 2N3502, 2N3504	50	70	-	-	I_C = 500 mA, V_{CE} = −10 Volts (Note 5)
h_{FE}	2N3503, 2N3505, 2N3502, 2N3504	115	160	300	-	I_C = 50 mA, V_{CE} = −1.0 Volt
$V_{BE(sat)}$	2N3503, 2N3505, 2N3502, 2N3504	-	−0.9	−1.0	Volt	I_C = 50 mA, I_B = 2.5 mA (Pulsed, see Note 1)
$V_{BE(sat)}$	2N3503, 2N3505, 2N3502, 2N3504	-	−1.0	−1.3	Volts	I_C = 150 mA, I_B = 15 mA (Pulsed, see Note 1)
$V_{CE(sat)}$	2N3503, 2N3505, 2N3502, 2N3504	-	−0.08	−0.25	Volt	I_C = 50 mA, I_B = 2.5 mA (Pulsed, see Note 1)
$V_{CE(sat)}$	2N3503, 2N3505, 2N3502, 2N3504	-	−0.18	−0.4	Volt	I_C = 150 mA, I_B = 15 mA (Pulsed, see Note 1)
h_{fe}	2N3503, 2N3505, 2N3502, 2N3504	2.0	2.50	-	-	I_C = 50 mA, V_{CE} = −20 Volts (f = 100 mc)
$V_{CEO(sust)}$	2N3503, 2N3505, 2N3502, 2N3504	−60 −45	- -	- -	Volts Volts	I_C = 10 mA (pulsed), I_B = 0 (Notes 4 and 5)
t_{on}	2N3503, 2N3505, 2N3502, 2N3504	-	20	40	nsec	$I_C \approx$ 300 mA, $I_{B1} \approx$ 30 mA (Note 6)
t_{off}	2N3503, 2N3505, 2N3502, 2N3504	-	40	100	nsec	$I_C \approx$ 300 mA, $I_{B1} \approx$ 30 mA, $I_{B2} \approx$ −30 mA (Note 6)
$h_{FE}(-55°C)$	2N3503, 2N3505, 2N3502, 2N3504	50	100	-	-	I_C = 50 mA, V_{CE} = −1.0 Volt
I_{CES}	2N3503, 2N3505	-	0.07	10	nA	V_{CE} = −50 Volts, V_{BE} = 0
I_{CES}	2N3502, 2N3504	-	0.05	10	nA	V_{CE} = −30 Volts, V_{BE} = 0
BV_{CBO}	2N3503, 2N3505 2N3502, 2N3504	−60 −45	- -	- -	Volts Volts	I_C = 10μA, I_E = 0
BV_{EBO}	2N3503, 2N3505, 2N3502, 2N3504	−5.0	-	-	Volts	I_E = 10μA, I_C = 0
C_{ob}	2N3503, 2N3505, 2N3502, 2N3504	-	4.5	8.0	pf	I_E = 0, V_{CB} = −10 Volts
C_{TE}	2N3503, 2N3505, 2N3502, 2N3504	-	15	25	pf	I_C = 0, V_{EB} = −0.5 Volt

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol		Min	Typ	Max	Unit	Conditions
NF	2N3503, 2N3505, 2N3502, 2N3504	-	1.0	4.0	dB	I_C = 30μA, V_{CE} = −5.0 Volts (Note 7)
I_{CBO}(+150)	2N3503, 2N3505	-	-	10	μA	V_{CB} = −50 Volts, I_E = 0
I_{CBO}(+150)	2N3502, 2N3504	-	-	10	μA	V_{CB} = −30 Volts, I_E = 0
$V_{CE(sat)}$	2N3503, 2N3505, 2N3502, 2N3504	-	−0.5	−1.6	Volts	I_C = 500 mA, I_B = 50 mA (Pulsed, see Note 5)
$V_{BE(sat)}$	2N3503, 2N3505, 2N3502, 2N3504	-	-	−2.0	Volts	I_C = 500 mA, I_B = 50 mA (Pulsed, see Note 5)

SMALL SIGNAL CHARACTERISTICS (f = 1kc)

Symbol	Min	Typ	Max	Unit	Conditions
h_{ie}	-	1050	2300	Ohms	I_C = 10 mA, V_{CE} = −10 Volts
h_{oe}	-	110	800	umhos	I_C = 10 mA, V_{CE} = −10 Volts
h_{re}	-	240	1500	$x10^{-6}$	I_C = 10 mA, V_{CE} = −10 Volts
h_{fe}	135	200	420	-	I_C = 10 mA, V_{CE} = −10 Volts

NOTES:

(1) These ratings are limiting values above which the serviceability of any individual semiconductor may be impaired.

(2) These are steady state limits. The factory should be consulted on applications involving pulsed or low duty cycle operations.

(3) These ratings give a maximum junction temperature of 200°C and junction-to-case thermal resistance of 58.3°C/watt (derating factor of 17.2 mW/°C) for the 2N3502 and 2N3503, and 146°C/watt (derating factor of 6.85 mW/°C) for the 2N3504 and 2N3505; junction-to-ambient thermal resistance of 250°C/watt (derating factor of 4.0 mW/°C) for the 2N3502 and 2N3503, and 438°C/watt (derating factor of 2.28 mW/°C) for the 2N3504 and 2N3505.

(4) Rating refers to a high-current point where collector-to-emitter voltage is lowest.

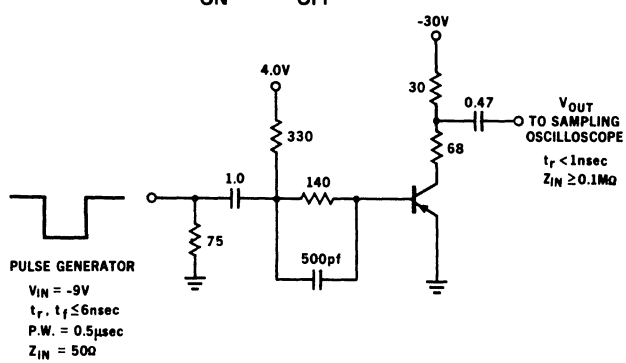
(5) Pulse Conditions: length = 300μsec; duty cycle = 1%.

(6) See switching circuit for exact values of I_C, I_{B1}, and I_{B2}.

(7) f = 1.0 Kc; R_S = 10 KΩ.

SCHEMATIC

FIGURE 1 − T_{ON} AND T_{OFF} TEST CIRCUIT



Packages:
2N3671, TO-5
2N3672, TO-18
2N3673, TO-46

2N3671, 2N3672, 2N3673®

HIGH-SPEED PNP SILICON SWITCH AND CORE DRIVER TRANSISTORS

ABSOLUTE MAXIMUM RATINGS (Note 1)

Characteristics	Unit
Storage Temperature	−65°C to +200°C
Operating Junction Temperature	200°C Maximum
Total Device Dissipation (Notes 2 and 3):	
@ T_C = 25°C (2N3671)	3.0 Watts
(2N3672)	1.8 Watts
(2N3673)	3.0 Watts
@ T_A = 25°C (2N3671)	0.6 Watt
(2N3672)	0.4 Watt
(2N3673)	0.35 Watt
Collector-Base Voltage	−60 Volts
Collector-Emitter Voltage (Note 4)	−50 Volts
Emitter-Base Voltage	−5.0 Volts
Collector Current (Note 2)	600 mA

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Min	Max	Unit	Conditions
h_{FE}	75	225	–	I_C = 150 mA, V_{CE} = −10 Volts (Note 5)
h_{FE}	75	–	–	I_C = 1.0 mA, V_{CE} = −10 Volts
h_{FE}	75	–	–	I_C = 10 mA, V_{CE} = −10 Volts (Note 5)
h_{FE}	55	–	–	I_C = 0.1 mA, V_{CE} = −10 Volts
h_{FE}	40	–	–	I_C = 500 mA, V_{CE} = −10 Volts (Note 5)
h_{FE}	20	–	–	I_C = 150 mA, V_{CE} = −0.6 Volt (Note 5)
$V_{CE(sat)}$	–	−0.4	Volt	I_C = 150 mA, I_B = 15 mA (Note 5)
$V_{CE(sat)}$	–	−1.6	Volts	I_C = 500 mA, I_B = 50 mA (Note 5)
$V_{BE(sat)}$	–	−1.3	Volts	I_C = 150 mA, I_B = 15 mA (Note 5)
$V_{BE(sat)}$	–	−2.6	Volts	I_C = 500 mA, I_B = 50 mA (Note 5)
t_d	–	10	ns	I_{CS} = 150 mA, I_{B1} = 15 mA (See Fig. 1)
t_r	–	40	ns	I_{CS} = 150 mA, I_{B1} = 15 mA (See Fig. 1)
t_s	–	80	ns	I_{CS} = 150 mA, I_{B1} = 15 mA, I_{B2} = −15 mA (See Fig. 2)

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Min	Max	Unit	Conditions
t_f	–	30	ns	I_{CS} = 150 mA, I_{B1} = 15 mA, I_{B2} = −15 mA (See Fig. 2)
t_{on}	–	45	ns	I_{CS} = 150 mA, I_{B1} = 15 mA (See Fig. 1)
t_{off}	–	100	ns	I_{CS} = 150 mA, I_{B1} = 15 mA, I_{B2} = −15 mA (See Fig. 2)
h_{fe}	2.0	–	–	I_C = 50 mA, V_{CE} = −20 Volts
I_{CBO}	–	10	nA	I_E = 0, V_{CB} = −50 Volts
I_{CBO}(150°C)	–	10	μA	I_E = 0, V_{CB} = −50 Volts
I_{CEX}	–	50	nA	V_{CE} = −30 Volts, V_{BE} = +0.5 Volt
I_B	–	50	nA	V_{CE} = −30 Volts, V_{BE} = +0.5 Volt
C_{obo}	–	9.0	pF	I_E = 0, V_{CB} = −10 Volts
C_{ibo}	–	30	pF	I_C = 0, V_{EB} = −2.0 Volts
BV_{CBO}	−60	–	Volts	I_C = 10μA, I_E = 0
$V_{CEO(sust)}$	−50	–	Volts	I_C = 10 mA (pulsed), I_B = 0 (Notes 4 and 5)
BV_{EBO}	−5.0	–	Volts	I_C = 0, I_E = 10μA

NOTES:

(1) These ratings are limiting values above which the serviceability of any individual semiconductor device may be impaired.

(2) These are steady state limits. The factory should be consulted on applications involving pulsed or low duty cycle operations.

(3) These ratings give a maximum junction temperature of 200°C and junction to case thermal resistance of 58.3°C/watt (derating factor of 17.2 mW/°C); junction to ambient thermal resistance of 292°C/watt (derating factor of 3.43 mW/°C) for the 2N3671. Junction to case thermal resistance of 97.3°C/watt (derating factor of 10.3 mW/°C) junction to ambient thermal resistance of 437°C/watt (derating factor of 2.28 mW/°C for the 2N3672. Junction to case thermal resistance of 58.3°C/watt (derating factor of 17.2 mW/°C); junction to ambient thermal resistance of 500°C/watt (derating factor of 2.0 mW/°C).

(4) Rating refers to a high-current point where collector to emitter voltage is lowest.

(5) Pulse Conditions: length = 300 μsec; duty cycle = 1%.

CIRCUIT DIAGRAM

FIGURE 1

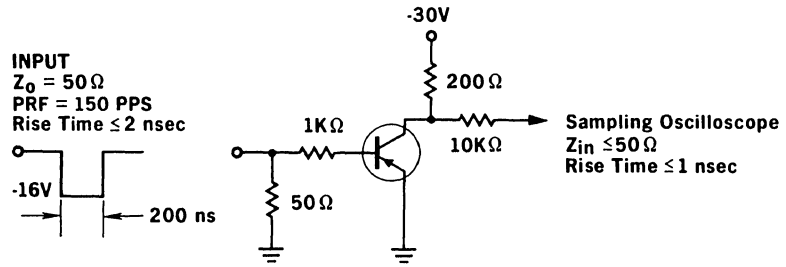
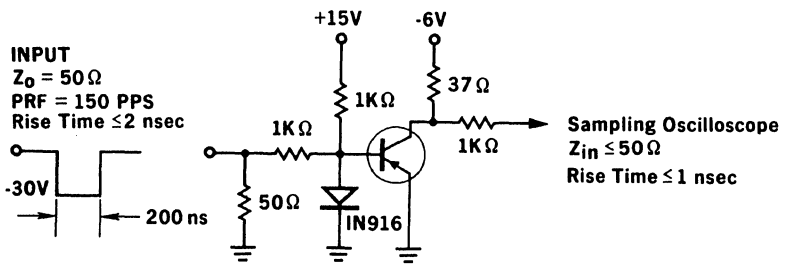


FIGURE 2



2N3962, 2N3963, 2N3964, 2N3965 Ⓕ

PNP SILICON LOW-LEVEL, LOW-NOISE TYPE TRANSISTORS

Package: TO-18

- **LOW NOISE FIGURE** ..... NF = 2.0 dB (MAX) AT 1.0 kHz
  NF = 4.0 dB (MAX) AT 100 Hz
- **HIGH CURRENT GAIN** ..... h_{FE} = 180 (MIN) AT 1.0 μA
  h_{FE} = 250 - 500 AT 10 μA
  h_{FE} = 250 - 600 AT 1.0 mA
- **HIGH BREAKDWON VOLTAGE** ..... LV_{CEO} = 45, 60 AND 80 VOLTS
- **EXCELLENT BETA LINEARITY** ..... FROM 1.0 μA TO 50 mA

ABSOLUTE MAXIMUM RATINGS (Note 1)

Characteristics	Unit
Collector-Base Voltage	
(2N3962, 2N3965)	−60 Volts
(2N3963)	−80 Volts
(2N3964)	−45 Volts
Collector-Emitter Voltage (Note 4)	
(2N3962, 2N3965)	−60 Volts
(2N3963)	−80 Volts
(2N3964)	−45 Volts
Emitter-Base Voltage	
(2N3962, 2N3963, 2N3964, 2N3965)	−6.0 Volts
Total Device Dissipation @:	
T_C = 25°C	1.2 Watts
T_A = 25°C	0.36 Watt
Storage Temperature	−65°C to +200 °C
Operating Junction Temperature	200°C
Lead Temperature	
(Soldering, 60 sec Time Limit)	300 °C

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol		Min	Typ	Max	Unit	Conditions
h_{FE}	2N3962, 2N3963	60	175	–	–	I_C = 1.0 μA, V_{CE} = −5.0 Volts
	2N3964, 2N3965	180	300	–	–	
h_{FE}	2N3962, 2N3963	100	210	300	–	I_C = 10 μA, V_{CE} = −5.0 Volts
	2N3964, 2N3965	250	320	500	–	
h_{FE}	2N3962, 2N3963	100	240	–	–	I_C = 100 μA, V_{CE} = −5.0 Volts
	2N3964, 2N3965	250	330	–	–	
h_{FE}	2N3962, 2N3963	100	260	450	–	I_C = 1.0 mA, V_{CE} = −5.0 Volts
	2N3964, 2N3965	250	330	600	–	

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol		Min	Typ	Max	Unit	Conditions
h_{FE}	2N3962, 2N3963	100	280	–	–	I_C = 10 mA, V_{CE} = −5.0 Volts (Note 5)
	2N3964, 2N3965	200	300	–	–	
h_{FE}	2N3962, 2N3963	90	260	–	–	I_C = 50 mA, V_{CE} = −5.0 Volts (Note 5)
	2N3964, 2N3965	180	315	–	–	
h_{FE}(−55°C)	2N3962, 2N3963	40	90	–	–	I_C = 10μA, V_{CE} = −5.0 Volts
	2N3964, 2N3965	100	160	–	–	
h_{FE}(−55°C)	2N3962, 2N3963	45	150	–	–	I_C = 50 mA, V_{CE} = −5.0 Volts (Note 5)
	2N3964, 2N3965	90	190	–	–	
h_{FE}(+100°C)	2N3962, 2N3963	–	375	600	–	I_C = 1.0 mA, V_{CE} = −5.0 Volts
	2N3964, 2N3965	–	400	800	–	
BV_{CBO}	2N3962	−60	–	–	Volts	I_C = 10μA, I_E = 0
	2N3964	−45	–	–	Volts	
BV_{CBO}	2N3963	−80	–	–	Volts	I_C = 10μA, I_E = 0
	2N3965	−60	–	–	Volts	
BV_{CES}	2N3962	−60	–	–	Volts	I_C = 10μA, I_B = 0
	2N3964	−45	–	–	Volts	
BV_{CES}	2N3963	−80	–	–	Volts	I_C = 10μA, I_B = 0
	2N3965	−60	–	–	Volts	
$V_{CEO(sust)}$	2N3962	−60	–	–	Volts	I_C = 5.0 mA (pulsed), I_B = 0 (Notes 4 and 5)
	2N3964	−45	–	–	Volts	
$V_{CEO(sust)}$	2N3963	−80	–	–	Volts	I_C = 5.0 mA (pulsed), I_B = 0 (Notes 4 and 5)
	2N3965	−60	–	–	Volts	
BV_{EBO}	2N3962, 2N3963	−6.0	–	–	Volts	I_C = 0, I_E = 10μA
	2N3964, 2N3965					
NF	2N3962, 2N3963	–	1.0	3.0	dB	I_C = 20μA, V_{CE} = −5.0 Volts
	2N3964, 2N3965	–	0.7	2.0	dB	R_S = 10 k ohms, BW = 15.7 kHz
NF	2N3962, 2N3963	–	0.8	3.0	dB	I_C = 20μA, V_{CE} = −5.0 Volts,
	2N3964, 2N3965	–	0.5	2.0	dB	R_S = 10 k ohms, BW = 1.5 kHz
NF	2N3962, 2N3963	–	0.8	3.0	dB	I_C = 20μA, V_{CE} = −5.0 Volts,
	2N3964, 2N3965	–	0.5	2.0	dB	R_S = 10 k ohms, BW = 150 Hz
NF	2N3962, 2N3963	–	3.0	10	dB	I_C = 20μA, V_{CE} = −5.0 Volts,
	2N3964, 2N3965	–	1.8	4.0	dB	R_S = 10 k ohms, BW = 15 Hz
NF	2N3964, 2N3965	–	3.5	8.0	dB	I_C = 20μA, V_{CE} = −5.0 Volts, R_S = 10 k ohms, BW = 2.0 Hz
I_{CES}	2N3962	–	0.5	10	nA	V_{CE} = −50 Volts, V_{EB} = 0
	2N3965					

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol		Min	Typ	Max	Unit	Conditions
I_{CES}	2N3963	-	0.5	10	nA	V_{CE} = −70 Volts, V_{EB} = 0
I_{CES}	2N3964	-	0.5	10	nA	V_{CE} = −40 Volts, V_{EB} = 0
I_{CES}(+150°C)	2N3962	-	2.0	10	μA	V_{CE} = −50 Volts, V_{EB} = 0
	2N3965	-	0.5	10	μA	
I_{CES}(+150°C)	2N3963	-	2.0	10	μA	V_{CE} = −70 Volts, V_{EB} = 0
I_{CES}(+150°C)	2N3964	-	2.0	10	μA	V_{CE} = −40 Volts, V_{EB} = 0
I_{EBO}	2N3962, 2N3963 2N3964, 2N3965	-	-	10	nA	I_C = 0, V_{EB} = −4.0 Volts
$V_{CE(sat)}$	2N3962, 2N3963 2N3964, 2N3965	-	−0.1	−0.25	Volt	I_C = 10 mA, I_B = 0.5 mA
$V_{CE(sat)}$	2N3962, 2N3963 2N3964, 2N3965	-	−0.16	−0.4	Volt	I_C = 50 mA, I_B = 5.0 mA (Note 5)
$V_{BE(sat)}$	2N3962, 2N3963 2N3964, 2N3965	-	−0.72	−0.9	Volt	I_C = 10 mA, I_B = 0.5 mA
$V_{BE(sat)}$	2N3962, 2N3963 2N3964, 2N3965	-	−0.81	−0.95	Volt	I_C = 50 mA, I_B = 5.0 mA (Note 5)
h_{ie}	2N3962, 2N3963	2.5	8.0	17	k ohms	I_C = 1.0 mA, V_{CE} = −5.0 Volts
	2N3964, 2N3965	6.0	10	20	k ohms	
h_{oe}	2N3962, 2N3963	5.0	19	40	μmho	I_C = 1.0 mA, V_{CE} = −5.0 Volts
	2N3964, 2N3965	5.0	25	50	μmho	
h_{re}	2N3962, 2N3963 2N3964, 2N3965	-	-	10	X 10^{-4}	I_C = 1.0 mA, V_{CE} = −5.0 Volts
h_{fe}	2N3962, 2N3963	100	300	550	-	I_C = 1.0 mA, V_{CE} = −5.0 Volts
	2N3964, 2N3965	250	360	700	-	
h_{fe}	2N3962, 2N3963	2.0	-	8.0	-	I_C = 0.5 mA, V_{CE} = −5.0 Volts
	2N3964, 2N3965	2.5	-	8.0	-	
C_{obo}	2N3962, 2N3963 2N3964, 2N3965	-	-	6.0	pF	I_E = 0, V_{CB} = −5.0 Volts
C_{ibo}	2N3962, 2N3963 2N3964, 2N3965	-	-	15	pF	I_C = 0, V_{EB} = −0.5 Volt

NOTES:

(1) These ratings are limiting values above which the serviceability of any individual semiconductor device may be impaired.

(2) These are steady state limits. The factory should be consulted on applications involving pulsed or low duty cycle operations.

(3) These ratings give a maximum junction temperature of 200°C and junction-to-case thermal resistance of 146°C/watt (derating factor of 6.85 mW/°C); junction-to-ambient thermal resistance of 486°C/watt (derating factor of 2.06 mW/°C).

(4) This rating refers to a high-current point where collector-to-emitter voltage is lowest.

(5) Pulse Conditions: length = 300μs; duty cycle = 1%.

Package: To-92

GENERAL PURPOSE PNP SILICON AMPLIFIER TRANSISTORS

ABSOLUTE MAXIMUM RATINGS

Characteristics	2N4059/62	2N4058	Unit
Collector-Emitter Voltage	40	25	V
Collector-Base Voltage	40	25	V
Emitter-Base Voltage	4.0		V
Collector Current	100		mA

Total Device Dissipation @ T_A = 60°C	210	mW
@ T_A = 25°C	310	
Junction Temperature	135	°C
Thermal Resistance, Junction to Ambient	0.357	°C/mW

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Min	Typ	Max	Unit	Conditions
BV_{CEO}	40	–	–	Vdc	2N4059/62 } I_C = 0.5 mAdc, I_B = 0
	25	–	–		2N4058 }
BV_{EBO}	4.0	–	–	Vdc	I_B = 10 uAdc, I_C = 0
I_{CBO}	–	–	0.05	uAdc	2N4059/62 V_{CB} = 30 Vdc, I_E = 0
	–	–	0.05		2N4058 V_{CB} = 20 Vdc, I_E = 0
	–	–	1.0		2N4059/62 V_{CB} = 30 Vdc, I_E = 0, T_A = 60°C
	–	–	1.0		2N4058 V_{CB} = 20 Vdc, I_E = 0, T_A = 60°C
h_{FE}	100	–	–	–	2N4058 I_C = 100 uAdc, V_{CE} = 10 Vdc
	50	–	100		2N4059/60 }
	90	–	180		2N4061 }
	150	–	300		2N4062 } I_C = 2 mAdc, V_{CE} = 10 Vdc
	200	–	400		2N4058 }
	30	–	–		2N4059/60 }
	60	–	–		2N4061 }
	90	–	–		2N4062 }
$V_{CE(sat)}$	–	–	0.5	Vdc	I_C = 50 mAdc, I_B = 5 mAdc
f_T	–	200	–	MHz	2N4059/61 } I_C = 2 mAdc, V_{CE} = 10 Vdc
	–	340	–		2N4062 }
	–	340	–		2N4058 }
	–	270	–		2N4059/61 } I_C = 10 mAdc, V_{CE} = 10 Vdc
	–	420	–		2N4062 }
	–	420	–		2N4058 }
C_{ob}	–	–	4.0	pF	2N4059/62 } V_{CB} = 10 Vdc, I_E = 0, f = 100 kHz
	–	–	4.0		2N4058 }
NF	–	1.8	3.0	dB	V_{CE} = 5 Vdc, I_C = 10 uAdc, R_S = 10 kohms, 2N4058 Power Bandwidth = 15.7 kHz, 3dB points @ 10 Hz and 10 kHz

*Pulse Test: Pulse Width ≤ 30 us, duty cycle ≤ 2%.

2N4248, 2N4249, 2N4250®

PNP SILICON LOW LEVEL, LOW NOISE AMPLIFIER TRANSISTORS

Package: TO-92

- **Low Noise Figure** ..... 2.0 dB (max) at 1.0 kHz
- **High Current Gain** ..... 250-700 at 100 μA
- **High Breakdown** ..... 40 and 60 Volts (min) LV_{CEO}
- **Excellent Beta Linearity** ..... From 1 μA to 50 mA

ABSOLUTE MAXIMUM RATINGS (Note 1)

Characteristics	Unit
Storage Temperatures	−55°C to 125°C
Operating Junction Temperatures	125°C
Lead Temperature (Soldering, 10 seconds time limit)	260°C
Total Device Dissipation (Notes 2 and 3)	
@ T_C = 25°C	0.5 Watt
@ T_A = 25°C	0.2 Watt
Collector-Base Voltage	
(2N4248, 2N4250)	−40 Volts
(2N4249)	−60 Volts
Collector-Emitter Voltage	
(2N4248, 2N4250)	−40 Volts
(2N4249)	−60 Volts
Emitter-Base Voltage	
(2N4248, 2N4250)	−5.0 Volts
(2N4249)	−5.0 Volts

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol		Min	Typ	Max	Unit	Conditions
NF	2N4248	–	0.7	–	dB	I_C = 20 μA, V_{CE} = −5.0 Volts
	2N4249	–	0.7	3.0	dB	(Note 6)
	2N4250	–	0.5	2.0	dB	
NF	2N4248	–	1.0	–	dB	I_C = 20 μA, V_{CE} = −5.0 Volts
	2N4249	–	1.0	3.0	dB	(Note 7)
	2N4250	–	0.7	2.0	dB	
NF	2N4248	–	0.8	–	dB	I_C = 250 μA, V_{CE} = −5.0 Volts
	2N4249	–	0.8	3.0	dB	(Note 8)
	2N4250	–	0.7	2.0	dB	
h_{FE}	2N4248	–	90	–	–	I_C = 10 μA, V_{CE} = −5.0 Volts
	2N4249	–	190	–	–	
	2N4250	–	300	–	–	
h_{FE}	2N4248	50	100	–	–	I_C = 100 μA, V_{CE} = −5.0 Volts
	2N4249	100	240	300	–	
	2N4250	250	350	700	–	

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol		Min	Typ	Max	Unit	Conditions
h_{FE}	2N4248	50	110	–	–	I_C = 1.0 mA, V_{CE} = −5.0 Volts
	2N4249	100	250	–	–	
	2N4250	250	350	–	–	
h_{FE}	2N4248	50	120	–	–	I_C = 10 mA, V_{CE} = −5.0 Volts
	2N4249	100	280	–	–	(Note 5)
	2N4250	250	350	–	–	
BV_{CBO}	2N4248, 2N4250	−40	–	–	Volts	I_C = 10μA, I_E = 0
	2N4249	−60	–	–	Volts	
BV_{CES}	2N4248, 2N4250	−40	–	–	Volts	I_C = 10μA
	2N4249	−60	–	–	Volts	
$V_{CEO(sust)}$	2N4248, 2N4250	−40	–	–	Volts	I_C = 5.0 mA (pulsed), I_B = 0
	2N4249	−60	–	–	Volts	(Notes 4 and 5)
BV_{EBO}	2N4248, 2N4249, 2N4250	−5.0	–	–	Volts	I_C = 0, I_E = 10μA
I_{CBO}	2N4248, 2N4249, 2N4250	–	–	10	nA	I_E = 0, V_{CB} = −40 Volts
$I_{CBO(65°C)}$	2N4248, 2N4249, 2N4250	–	–	3.0	μA	I_E = 0, V_{CB} = 40 Volts
I_{EBO}	2N4248, 2N4249, 2N4250	–	–	20	nA	I_C = 0, V_{BE} = 3.0 Volts
$V_{CE(sat)}$	2N4248, 2N4249, 2N4250	–	–	−0.25	Volt	I_C = 10 mA, I_B = 0.5 mA (Note 5)
$V_{BE(sat)}$	2N4248, 2N4249, 2N4250	–	–	−0.9	Volt	I_C = 10 mA, I_B = 0.5 mA (Note 5)
h_{fe}	2N4248	50	–	–	–	I_C = 1.0 mA, V_{CE} = −5.0 Volts
	2N4249	100	250	550	–	
	2N4250	250	350	800	–	
h_{fe}	2N4248, 2N4249	2.0	–	–	–	I_C = 0.5 mA, V_{CE} = −5.0 Volts
	2N4250	2.5	–	–	–	
C_{obo}	2N4248, 2N4249, 2N4250	–	–	6.0	pF	I_E = 0, V_{CB} = −5.0 Volts
C_{ibo}	2N4248, 2N4249, 2N4250	–	–	16	pF	I_C = 0, V_{BE} = 0.5 Volt

SMALL SIGNAL CHARACTERISTICS (f = 1 kHz)

Symbol		Min	Typ	Max	Unit	Conditions
h_{ie}	2N4249	2.5	8.0	17	k ohms	I_C = 1.0 mA, V_{CE} = 5.0 Volts
	2N4250	6.0	10	20	k ohms	
h_{oe}	2N4249	5.0	19	40	μmho	I_C = 1.0 mA, V_{CE} = −5.0 Volts
	2N4250	5.0	25	50	μmho	
h_{re}	2N4249, 2N4250	–	–	10	$x10^{-4}$	I_C = 1.0 mA, V_{CE} = −5.0 Volts
h_{fe}	2N4249	100	250	550	–	I_C = 1.0 mA, V_{CE} = −5.0 Volts
	2N4250	250	350	800	–	

NOTES:

(1) These ratings are limiting values above which the serviceability of any individual semiconductor device may be impaired.

(2) These are steady state limits. The factory should be consulted on applications involving pulsed or low-duty cycle operations.

(3) These ratings give a maximum junction temperature of 125°C and junction-to-case thermal resistance of 200°C/watt (derating factor of 5.0 mW/°C); junction-to-ambient thermal resistance of 500°C/watt (derating factor of 2.0 mW/°C).

(4) This rating refers to a high-current point where collector to emitter voltage is lowest.

(5) Pulse Conditions: length = 300 μs; duty cycle = 1%.

(6) R_S = 10 kΩ, Power Bandwidth of 150 Hz.

(7) R_S = 10 kΩ, Power Bandwidth of 15.7 kHz with 3.0 dB points at 10 Hz and 10 kHz.

(8) R_S = 1.0 kΩ, Power Bandwidth of 150 Hz.

2N5086, 2N5087

LOW-LEVEL, LOW-NOISE PNP SILICON AMPLIFIER TRANSISTORS

ABSOLUTE MAXIMUM RATINGS

Characteristic	Unit
Collector-Emitter Voltage	50 Vdc
Collector-Base Voltage	50 Vdc
Emitter-Base Voltage	3.0 Vdc
Collector Current - Continuous	50 mAdc
Peak	100 mAdc

Total Device Dissipation @ T_A = 25°C	310 mW
Derate above 25°C	2.81 mW/°C
Operating and Storage Junction Temperature Range	-55 to +135 °C
Thermal Resistance, Junction to Ambient	0.357 °C/mW

ELECTRICAL CHARACTERISTICS T_A = 25°C unless otherwise noted

Symbol	Min	Typ	Max	Unit	Conditions
BV_{CEO}	50	–	–	Vdc	I_C = 1.0 mAdc, I_B = 0
BV_{CBO}	50	–	–	Vdc	I_C = 100 uAdc, I_E = 0
I_{CBO}	–	–	10	nAdc	V_{CB} = 10 Vdc, I_E = 0
	–	–	50		V_{CB} = 35 Vdc, I_E = 0
I_{EBO}	–	–	50	nAdc	V_{BE} = 3.0 Vdc, I_C = 0
h_{FE}	150	–	500	–	I_C = 100 uAdc, V_{CE} = 5.0 Vdc 2N5086
	250	–	800		2N5087
	150	–	–		I_C = 1.0 mAdc, V_{CE} = 5.0 Vdc 2N5086
	250	–	–		2N5087
	150	–	–		I_C = 10 mAdc, V_{CE} = 5.0 Vdc 2N5086
	250	–	–		2N5087
$V_{CE(sat)}$	–	–	0.3	Vdc	I_C = 10 mAdc, I_B = 1.0 mAdc
$V_{BE(on)}$	–	–	0.85	Vdc	I_C = 1.0 mAdc, V_{CE} = 5.0 Vdc
f_T	40	120	–	MHz	I_C = 500 uAdc, V_{CE} = 5.0 Vdc, f = 20 MHz 2N5086
	40	150	–		2N5087
C_{ob}	–	–	4.0	pF	V_{CB} = 5.0 Vdc, I_E = 0, f = 100 kHz
h_{fe}	150	–	600	–	I_C = 1.0 mAdc, V_{CE} = 5.0 Vdc, f = 1.0 kHz 2N5086
	250	–	900		2N5087
NF	–	–	3.0	dB	I_C = 20 uAdc, V_{CE} = 5.0 Vdc, R_S = 10 k ohms, f = 10 Hz to 15.7 kHz 2N5086
	–	–	2.0		2N5087
	–	1.2	3.0		I_C = 100 uAdc, V_{CE} = 5.0 Vdc, R_S = 3.0 k ohmn, f = 1.0 kHz 2N5086
	–	1.0	2.0		2N5087

2N5221

Package: To-92

LOW-POWER GENERAL PURPOSE PNP SILICON AMPLIFIER TRANSISTOR

ABSOLUTE MAXIMUM RATINGS

Characteristic	Unit
Collector-Emitter Voltage	15 Vdc
Collector-Base Voltage	15 Vdc
Emitter-Base Voltage	3.0 Vdc
Collector Current	500 mAdc
Total Device Dissipation @ T_A = 25°C	310 mW
Derate above 25°C	2.81 mW/°C
Operating and Storage Junction Temperature Range	-55 to +135 °C
Thermal Resistance, Junction to Ambient	0.357 °C/mW

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Min	Max	Unit	Conditions
BV_{CEO}	15	–	Vdc	I_C = 10 mAdc, I_B = 0
BV_{CBO}	15	–	Vdc	I_C = 100 μAdc, I_E = 0
BV_{EBO}	3.0	–	Vdc	I_E = 100 μAdc, I_C = 0
I_{CBO}	–	100	nAdc	V_{CB} = 10 Vdc, I_E = 0
I_{EBO}	–	100	nAdc	V_{BE} = 3.0 Vdc, I_C = 0
h_{FE}	25	–	–	I_C = 10 mAdc, V_{CE} = 10 Vdc
	30	600		I_C = 50 mAdc, V_{CE} = 10 Vdc
$V_{CE(sat)}$	–	0.5	Vdc	I_C = 150 mAdc, I_B = 15 mAdc
$V_{BE(sat)}$	–	1.1	Vdc	I_C = 150 mAdc, I_B = 15 mAdc
f_T	100	–	MHz	I_C = 20 mAdc, V_{CE} = 10 Vdc
C_{cb}	–	15	pF	V_{CB} = 5.0 Vdc, I_E = 0, f = 1.0 MHz
h_{fe}	30	1800	–	I_C = 50 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz

Package: To-92

MEDIUM POWER PNP SILICON AMPLIFIER TRANSISTOR

ABSOLUTE MAXIMUM RATINGS

Characteristic	Unit
Collector-Emitter Voltage	25 Vdc
Collector-Base Voltage	25 Vdc
Emitter-Base Voltage	4.0 Vdc
Collector Current	500 mAdc
Total Device Dissipation @ T_A = 25°C	310 mW
Derate above 25°C	2.81 mW/°C
Operating and Storage Junction Temperature Range	-55 to +135 °C
Thermal Resistance, Junction to Ambient	0.357 °C/mW

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Min	Max	Unit	Conditions
BV_{CEO}	25	–	Vdc	I_C = 10 mAdc, I_B = 0
BV_{CBO}	25	–	Vdc	I_C = 100 μAdc, I_E = 0
BV_{EBO}	4.0	–	Vdc	I_E = 100 μAdc, I_C = 0
I_{CBO}	–	300	nAdc	V_{CB} = 15 Vdc, I_E = 0
I_{EBO}	–	500	nAdc	V_{BE} = 4.0 Vdc, I_C = 0
h_{FE}	25	–	–	I_C = 10 mAdc, V_{CE} = 10 Vdc
	30	600		I_C = 50 mAdc, V_{CE} = 10 Vdc
$V_{CE(sat)}$	–	0.8	Vdc	I_C = 100 mAdc, I_B = 10 mAdc
$V_{BE(sat)}$	–	1.0	Vdc	I_C = 100 mAdc, I_B = 10 mAdc
f_T	50	–	MHz	I_C = 20 mAdc, V_{CE} = 10 Vdc
C_{cb}	–	20	pF	V_{CB} = 5.0 Vdc, I_E = 0, f = 1.0 MHz
h_{fe}	30	1800	–	I_C = 50 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz

2N5227

Package: To-92

GENERAL PURPOSE PNP SILICON LOW-LEVEL AMPLIFIER TRANSISTOR

ABSOLUTE MAXIMUM RATINGS

Characteristic	Unit
Collector-Emitter Voltage	30 Vdc
Collector-Base Voltage	30 Vdc
Emitter-Base Voltage	3.0 Vdc
Collector Current	50 mAdc
Total Device Dissipation @ T_A = 25°C	310 mW
Derate above 25°C	2.81 mW/°C
Operating and Storage Junction Temperature Range	-55 to +135 °C
Thermal Resistance, Junction to Ambient	0.357 °C/mW

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Min	Max	Unit	Conditions
BV_{CEO}	30	–	Vdc	I_C = 1.0 mAdc, I_B = 0
BV_{CBO}	30	–	Vdc	I_C = 100 uAdc, I_E = 0
BV_{EBO}	3.0	–	Vdc	I_E = 100 uAdc, I_C = 0
I_{CBO}	–	100	nAdc	V_{CB} = 10 Vdc, I_E = 0
I_{EBO}	–	500	nAdc	V_{BE} = 2.0 Vdc, I_C = 0
h_{FE}	30	–	–	I_C = 100 uAdc, V_{CE} = 10 Vdc
	50	700		I_C = 2.0 mAdc, V_{CE} = 10 Vdc
$V_{CE(sat)}$	–	0.4	Vdc	I_C = 10 mAdc, I_B = 1.0 mAdc
$V_{BE(sat)}$	–	1.0	Vdc	I_C = 10 mAdc, I_B = 1.0 mAdc
f_T	100	–	MHz	I_C = 10 mAdc, V_{CE} = 10 Vdc
C_{cb}	–	5.0	pF	V_{CB} = 10 Vdc, I_E = 0
h_{fe}	50	1500	–	I_C = 2.0 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz

Package TO-92

GENERAL PURPOSE PNP SILICON TRANSISTORS

ABSOLUTE MAXIMUM RATINGS @ 25°C (free air)

Characteristics	Unit
Storage temperature range	-55 to +150 °C
Operating Collector Junction Temperature	+150 °C
Lead temperature 1/16" from case 10 seconds max.	+260 °C
Collector current	500 mA
Continuous device dissipation at or below 25°C free-air temperature	360 mW
Linear derating factor above 25°C	2.87 mW/°C
Emitter-base voltage	5 V
Collector-base voltage	60 V
Collector-base voltage (2N5375)	40 V
Collector-emitter voltage (Applicable from I_C = 0 mA to I_C - 10 mA	30 V

ELECTRICAL CHARACTERISTICS @ 25°C free-air temperature

Symbol	Min	Max	Unit	Conditions	
I_{CBO}	–	50	nA	2N5372, 2N5373, 2N5374	V_{CB} = 40 V, I_E = 0
	–	50	nA	2N5375	V_{CB} = 30 V, I_E = 0
I_{EBO}	–	50	nA	V_{EB} = 3 V, I_C = 0	
BV_{CBO}	60	–	V	2N5372, 2N5373, 2N5374	I_C = 10 uA, I_E = 0
	40	–	V	2N5375	I_C = 10 uA, I_E = 0
BV_{EBO}	5	–	V	I_E = 10 uA, I_C = 0	
BV_{CEO}	30	–	V	I_C = 10 mA, I_B = 0 (Note 1)	
h_{FE}	20	–	–	2N5372	V_{CE} = 10 V, I_C = 1 mA
	50	–	–	2N5373	
	100	–	–	2N5374	
	20	–	–	2N5375	
h_{FE}	30	–	–	2N5372	V_{CE} = 10 V, I_C = 10 mA (Note 1)
	75	–	–	2N5373	
	150	–	–	2N5374	
	30	–	–	2N5375	
h_{FE}	40	120	–	2N5372	V_{CE} = 10 V, I_C = 150 mA (Note 1)
	100	300	–	2N5373	
	200	400	–	2N5374	
	40	400	–	2N5375	
V_{BE}	–	1.2	V	V_{CE} = 10 V, I_C = 150 mA (Note 1)	
$V_{BE(sat)}$	–	1.3	V	I_C = 150 mA, I_B = 15 mA (Note 1)	
$V_{CE(sat)}$	–	0.3	V	I_C = 150 mA, I_B = 15 mA (Note 1)	
C_{cb}	–	10	pF	V_{CB} = 10 V, I_E = 0, f = 1 MHz (Note 2)	
$[h_{fe}]$	1.5	–	–	V_{CE} = 10 V, I_C = 20 mA, f = 100 MHz	
t_{on}	–	50	nsec	I_C = 150 mA, V_{CC} = 30 V, I_{B1} = 15 mA, (see fig. 1)	
t_{off}	–	150	nsec	2N5372, 2N5373	I_C = 150 mA, V_{CC} = 6 V,
	–	175	usec	2N5374, 2N5375	I_{B1} = I_{B2} = 15 mA (see fig. 2)

NOTES: 1. Pulse test: PW = 300 usec, duty cycle ≤ 2%.
2. C_{cb} measurement employs a three-terminal capacitance bridge incorporating a guard circuit. The emitter terminal shall be connected to the guard terminal of the bridge.

2N5378, 2N5379

Package: To-92

GENERAL PURPOSE PNP SILICON TRANSISTORS

ABSOLUTE MAXIMUM RATINGS @ 25°C (free air)

Characteristics	Unit
Storage temperature range	-55 to +150 °C
Operating Collector Junction Temperature	+150 °C
Lead temperature 1/16" from case 10 seconds max.	+260 °C
Emitter-base voltage	5 V
Collector-base voltage	40 V
Collector-emitter voltage (Applicable from I_C = 0 mA to I_C = 10 mA)	30 V
Collector current	500 mA
Continuous device dissipation at or below 25°C free-air temperature	360 mW
Linear derating factor above 25°C	2.87 mW/°C

ELECTRICAL CHARACTERISTICS @ 25°C free-air temperature

Symbol	Min	Max	Unit	Conditions
I_{CBO}	–	10	nA	V_{CB} = 30 V, I_E = 0
BV_{CBO}	40	–	V	I_C = 10 uA, I_E = 0
BV_{EBO}	5	–	V	I_E = 100 nA, I_C = 0
BV_{CEO}	30	–	V	I_C = 10 mA, I_B = 0 (Note 1)
h_{FE}	100	500	–	2N5378 V_{CE} = 5 V, I_C = 10 uA
	40	200	–	2N5379 V_{CE} = 5 V, I_C = 10 uA
h_{FE}	120	600	–	2N5378 V_{CE} = 5 V, I_C = 1 mA
	100	500	–	2N5379 V_{CE} = 5 V, I_C = 1 mA
h_{FE}	150	–	–	2N5378 V_{CE} = 5 V, I_C = 10 mA (Note 1)
	120	–	–	2N5379
$V_{BE(sat)}$	0.65	0.80	V	I_C = 10 mA, I_B = 1 mA
$V_{CE(sat)}$	–	0.2	V	I_C = 10 mA, I_B = 1 mA
h_{ib}	20	32	Ohms	I_C = 1 mA, V_{CE} = 5 V, f = 1 kHz
h_{ob}	0.06	0.5	umhos	I_C = 1 mA, V_{CE} = 5 V, f = 1 kHz
h_{fe}	120	1000	–	2N5378 I_C = 1 mA, V_{CE} = 5 V, f = 1 kHz
	100	900	–	2N5379
C_{cb}	–	10	pF	V_{CB} = 10 V, I_E = 0, f = 1 Mhz (Note 2)
$[h_{fe}]$	20	100	–	V_{CE} = 5 V, I_C = 500 uA, f = 10 MHz
NF	–	2.0	dB	2N5378 I_C = 10 uA, V_{CE} = 5 V, Rg = 10 K Ohms,
	–	3.0	dB	2N5379 Bandwidth = 10 Hz to 15.7 kHz

NOTES:
1. Pulse: tPulse width = 300 usec, duty cycle ≤ 2%.
2. C_{cb} measurement employs a three-terminal capacitance bridge incorporating a guard circuit. The emitter terminal shall be connected to the guard terminal of the bridge.

Package: To-92

PNP SILICON AMPLIFIER TRANSISTORS

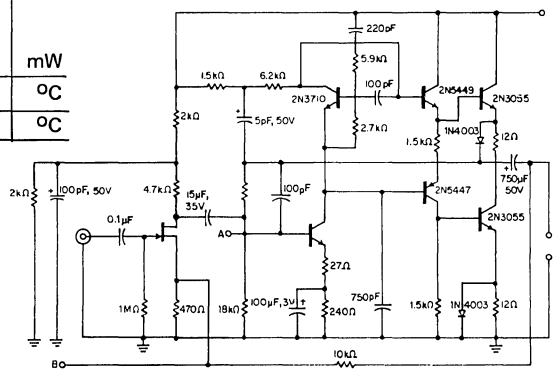
***ABSOLUTE MAXIMUM RATINGS** at 25°C free-air temperature (unless otherwise noted)

Characteristic	2N5447	2N5448	Unit
Collector-Base Voltage	−40	−50	V
Collector-Emitter Voltage (See Note 1)	−25	−30	V
Emitter-Base Voltage	−5	−5	V
Continuous Collector Current	200		mA
Continuous Device Dissipation at (or below) 25°C Free-Air Temperature (See Note 2)	360		mW
Continuous Device Dissipation at (or below) 25°C Lead Temperature (See Note 3)	500		mW
Storage Temperature Range	−65 to 150		°C
Junction Temperature-Operating	260		°C

NOTES:

1. These values apply when the base-emitter diode is open-circuited.
2. Derate linearly to 150°C free-air temperature at the rate of 2.88 mW/deg.
3. Derate linearly to 150°C lead temperature at the rate of 4 mW/deg. Lead temperature is measured on the collector lead 1/16 inch from the case.

SILICON 15-WATT QUASI-COMPLEMENTARY POWER AMPLIFIER



ELECTRICAL CHARACTERISTICS at 25°C free-air temperature

Symbol	2N5447 Min	2N5447 Max	2N5448 Min	2N5448 Max	Unit	Test Conditions
$V_{(BR)CBO}$	−40		−50		V	I_C = −100 uA, E_E = 0
$V_{(BR)CEO}$	−25		−30		V	I_C = −10 mA, I_B = 0, See Note 4
$V_{(BR)EBO}$	−5		−5		V	I_E = −100 uA, I_C = 0
I_{CBO}		−100		−100	nA	V_{CB} = 20 V, I_E = 0
I_{EBO}		−100		−100	nA	V_{EB} = −3 V, I_C = 0
h_{FE}	60	300	30	150		V_{CE} = −5 V, I_C = −50 mA, See Note 4
V_{BE}	−0.6	−1	−0.6	−1	V	V_{CE} = −5 V, I_C = −50 mA, See Note 4
V_{CE}		−0.25		−0.25	V	I_B = −5 mA, I_C = −50 mA, See Note 4
$[h_{fe}]$	5		5			V_{CE} = −5 V, I_C = −50 mA, f = 20 MHz
C_{cb}		12		12	pF	V_{CB} = 10 V, I_E = 0, f = 1 MHz See Note 5

NOTES: 4. These parameters must be measured using pulse techniques. t_p = 300 us, duty cycle ≤ 2%.
5. C_{cb} is measured using three-terminal measurement techniques with the emitter guarded.

MPS-A55

PNP SILICON AMPLIFIER TRANSISTOR

Package: To-92

ABSOLUTE MAXIMUM RATINGS

Characteristic		Unit
Collector-Emitter Voltage	60	Vdc
Collector-Base Voltage	60	Vdc
Emitter-Base Voltage	4.0	Vdc
Collector Current - Continuous	500	mAdc
Total Device Dissipation @ T_A = 25°C	500	mW
Derate above 25°C	4.54	mW/°C
Total Device Dissipation @ T_C = 25°C	800	mW
Derate above 25°C	7.27	mW/°C
Operating and Storage Junction Temperature Range	-55 to +135	°C
Thermal Resistance, Junction to Case	0.137	°C/mW
Thermal Resistance, Junction to Ambient	0.220	°C/mW

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Min	Typ	Max	Unit	Conditions
BV_{CEO}	60	–	–	Vdc	I_C = 1.0 mAdc, I_B = 0
BV_{EBO}	4.0	–	–	Vdc	I_E = 100 uAdc, I_C = 0
I_{CBO}	–	–	100	nAdc	V_{CB} = 60 Vdc, I_E = 0
h_{FE}	50	150	–	–	I_C = 10 mAdc, V_{CE} = 1.0 Vdc
	50	125	–		I_C = 100 mAdc, V_{CE} = 1.0 Vdc
	–	80	–		I_C = 350 mAdc, V_{CE} = 1.0 Vdc
$V_{CE(sat)}$	–	0.09	0.25	Vdc	I_C = 100 mAdc, I_B = 10 mAdc
$V_{BE(sat)}$	–	0.78	–	Vdc	I_C = 100 mAdc, I_B = 10 mAdc
$V_{BE(on)}$	–	0.73	1.2	Vdc	I_C = 100 mAdc, V_{CE} = 1.0 Vdc
f_T	50	100	–	MHz	I_C = 100 mAdc, V_{CE} = 1.0 Vdc, f = 100 MHz
C_{ob}	–	6.5	–	pF	V_{CB} = 10 Vdc, I_E = 0, f = 100 kHz
C_{ib}	–	20	–	pF	V_{BE} = 0.5 Vdc, I_C = 0, f = 100 kHz

Package: To-92

GENERAL PURPOSE PNP SILICON AMPLIFIER TRANSISTORS

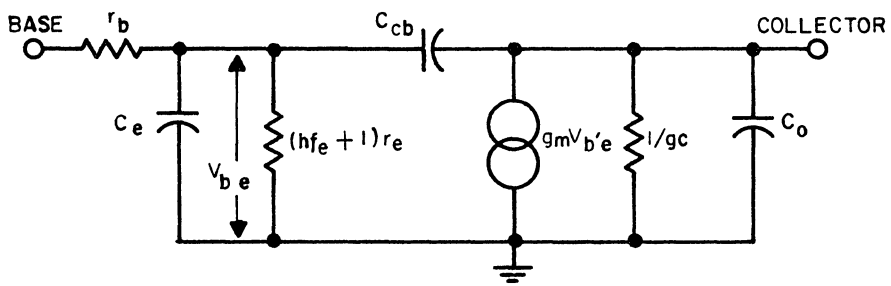
ABSOLUTE MAXIMUM RATINGS

Characteristics	Unit
Collector-Emitter Voltage	40 Vdc
Emitter-Base Voltage	4.0 Vdc
Collector Current - Continuous	100 mAdc
Total Device Dissipation @ T_A = 25°C	300 mW
Derate above 25°C	2.73 mW/°C
Operating and Storage Junction Temperature Range	-55 to +135 °C
Thermal Resistance, Junction to Ambient	0.367 °C/mW

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Min	Max	Unit	Conditions
BV_{CEO}	40	–	Vdc	I_C = 1.0 mAdc, I_B = 0
BV_{EBO}	4.0	–	Vdc	I_E = 100 uAdc, I_C = 0
I_{CBO}	–	100	nAdc	V_{CB} = 30 Vdc, I_E = 0
h_{FE}	40	400	–	I_C = 5.0 mAdc, V_{CE} = 10 Vdc
$V_{CE(sat)}$	–	0.25	Vdc	I_C = 10 mAdc, I_B = 1.0 mAdc
f_T	125	–	MHz	I_C = 5.0 mAdc, V_{CE} = 10 Vdc, f = 100 MHz
C_{ob}	–	4.0	pF	V_{CB} = 10 Vdc, I_E = 0, f = 100 kHz

Figure 1—Simplified AC Equivalent Circuit (Common Emitter)



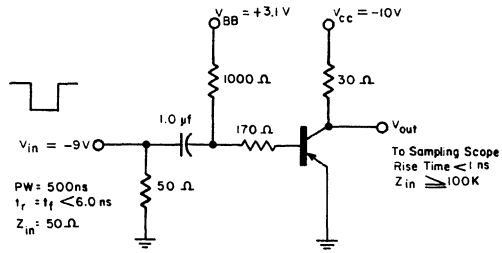
MPS3638, MPS3638A
PNP SILICON TRANSISTOR

Package: To-92

ABSOLUTE MAXIMUM RATINGS

Characteristics	Unit
Collector-Emitter Voltage	25 Vdc
Collector-Emitter Voltage	25 Vdc
Collector-Base Voltage	25 Vdc
Emitter-Base Voltage	4.0 Vdc
Collector Current	500 mAdc
Total Device Dissipation @ T_A = 25°C	310 mW
Derate above 25°C	2.81 mW/°C
Operating and Storage Junction Temperature Range	-55 to +135 °C
Thermal Resistance, Junction to Ambient	0.357 °C/mW

Figure 1



ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Min	Max	Unit	Conditions
BV_{CEO}*	25	–	Vdc	I_C = 10 mAdc, I_B = 0
BV_{CES}	25	–	Vdc	I_C = 100 uAdc, V_{BE} = 0
BV_{CBO}	25	–	Vdc	I_C = 100 uAdc, I_E = 0
BV_{EBO}	4.0	–	Vdc	I_E = 100 uAdc, I_C = 0
I_{CES}	–	0.035	uAdc	V_{CE} = 15 Vdc, V_{BE} = 0
	–	2.0		V_{CE} = 15 Vdc, V_{BE} = 0, T_A = 65°C
I_B	–	0.035	uAdc	V_{CE} = 15 Vdc, V_{BE} = 0
h_{FE}*	80	–	–	I_C = 1 mAdc, V_{CE} = 10 Vdc MPS3638A
	20	–		I_C = 10 mAdc, V_{CE} = 10 Vdc MPS3638
	100	–		MPS3638A
	30	–		I_C = 50 mAdc, V_{CE} = 1 Vdc MPS3638
	100	–		MPS3638A
	20	–		I_C = 300 mAdc, V_{CE} = 2 Vdc MPS3638
	20	–		MPS3638A
$V_{CE(sat)}$*	–	0.25	Vdc	I_C = 50 mAdc, I_B = 2.5 mAdc
	–	1.0		I_C = 300 mAdc, I_B = 30 mAdc
$V_{BE(sat)}$*	–	1.1	Vdcq	I_C = 50 mAdc, I_B = 2.5 mAdc
	0.80	2.0		I_C = 300 mAdc, I_B = 30 mAdc
f_T	100	–	MHz	V_{CE} = 3 Vdc, I_C = 50 mAdc, f = MHz MPS3638
	150	–		MPS3638A
C_{ob}	–	20	pF	V_{CB} = 10 Vdc, I_E = 0, f = 140 kHz MPS3638
	–	10		MPS3638A

ELECTRICAL CHARACTERISTICS $T_A = 25°C$ unless otherwise specified

SYMBOL	MIN	MAX	UNIT	CONDITIONS
C_{ib}	–	65	pF	V_{CE} = 0.5 Vdc, I_C = 0, f = 140 kHz MPS3638
	–	25		MPS3638A
h_{fe}	25	180	–	I_C = 10 mAdc, V_{CE} = 10 Vdc, F = 1.0 kHz MPS3638
	100	–		MPS3638A
h_{oe}	–	1.2	mmhos	I_C = 10 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz
h_{ie}	–	1500	Ohms	I_C = 10 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz MPS3638
	–	2000		MPS3638A
h_{re}	–	26	X10-4	I_C = 10 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz MPS3638
	–	15		MPS3638A
t_d	–	20	ns	Delay Time V_{CC} = 10 Vdc, I_C = 300 mAdc,
t_r	–	70	ns	Rise Time I_{B1} = 30 mAdc, $V_{BE(off)}$ = 3.1 Vdc
t_s	–	140	ns	Storage Time V_{CC} = 10 Vdc, I_C = 300 mAdc,
t_f	–	70	ns	Fall Time I_{B1} = 30 mAdc, I_{B2} = 30 mAdc
t_{on}	–	75	ns	Turn-On Time I_C = 300 mAdc, I_{B1} = 30 mAdc
t_{off}	–	170	ns	Turn-Off Time I_C = 300 mAdc, I_{B1} = 30 mAdc, I_{B2} = 30 mAdc

*Pulse Test: Pulse Width = 300 us; Duty Cycle = 1%.

ABSOLUTE MAXIMUM RATINGS

Characteristics	MPS3702	MPS3703	Unit
Collector-Emitter Voltage	25	30	Vdc
Collector-Base Voltage	40	50	Vdc
Emitter-Base Voltage	5.0		Vdc
Collector Current - Continuous	200		mAdc
Total Device Dissipation @ T_A = 25°C	310		mW
Derate above 25°C	2.81		mW/°C
Operating and Storage Junction Temperature Range	-55 to +135		°C
Thermal Resistance, Junction to Ambient	0.357		°C/mW

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Min	Max	Unit	Conditions	
BV_{CEO}*	25	–	Vdc	I_C = 10 mAdc, I_B = 0	MPS3702
	30	–			MPS3702
BV_{CBO}	40	–	Vdc	I_C = 100 uAdc, I_E = 0	MPS3702
	50	–			MPS3703
BV_{EBO}	5.0	–	Vdc	I_E = 100 uAdc, I_C = 0	
I_{CBO}	–	100	nAdc	V_{CB} = 20 Vdc, I_E = 0	
I_{EBO}	–	100	nAdc	V_{BE} = 3 Vdc, I_C = 0	
h_{FE}*	60	300	–	I_C = 50 mAdc, V_{CE} = 5 Vdc	MPS3702
	30	150			MPS3703
$V_{CE(sat)}$*	–	0.25	Vdc	I_C = 50 mAdc, I_B = 5 mAdc	
$V_{BE(on)}$*	0.6	1.0	Vdc	I_C = 50 mAdc, V_{CE} = 5 Vdc	
f_T	100	–	MHz	I_C = 50 mAdc, V_{CE} = 5 Vdc, f = 20 MHz	
C_{ob}	–	12	pF	V_{CB} = 10 Vdc, f = 1 MHz	

*Pulse Test: Pulse Width = 300 us; Duty Cycle = 2%.

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Characteristic			Unit
Collector-Base Voltage			
MPS6533, MPS6534		40	Vdc
MPS6535		39	
Collector-Emitter Voltage			
MPS6533, MPS6534		40	
MPS6535		30	

Emitter-Base Voltage	5.0	4.0	Vdc
Collector Current	600	600	mAdc
Total Device Dissipation			
@ T_A = 60°C	210	210	mW
@ T_A = 25°C	310	310	
Thermal Resistance, Junction to Ambient	0.357	0.357	°C/mW
Junction Temperature	135	135	°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Min	Typ	Max	Unit	Conditions	
BV_{CBO}	40	–	–	Vdc	I_C = 10 uAdc, I_E = 0	MPS6533, MPS6534
	30	–	–			MPS6535
BV_{CEO}	40	–	–	Vdc	I_C = 10 mAdc, I_B = 0	MPS6533, MPS6534
	30	–	–			MPS6535
BV_{EBO}	4.0	–	–	Vdc	I_B = 10 uAdc, I_C = 0	
I_{CBO}	–	–	0.05	uAdc	V_{CB} = 30 Vdc, I_E = 0	MPS6533, MPS6534
	–	–	0.1		V_{CB} = 20 Vdc, I_E = 0	MPS6535
	–	–	2.0		V_{CB} = 30 Vdc, I_E = 0,	MPS6533,
					T_A = 60°C	MPS6534
	–	–	5.0		V_{CB} = 20 Vdc, I_E = 0, T_A = 60°C	MPS6535
h_{FE}	30	70	–	–	I_C = 10 mAdc, V_{CE} = 1 Vdc	MPS6533
	60	110	–			MPS6534
	40	85	120		I_C = 100 mAdc, V_{CE} = 1 Vdc	MPS6533
	90	140	270			MPS6534
	30	–	–			MPS6535
	25	55	–		I_C = 500 mAdc, V_{CE} = 10 Vdc	MPS6533
	50	70	–			MPS6534
$V_{CE(sat)}$	–	0.2	0.5	Vdc	I_C = 100 mAdc, I_B = 10 mAdc	MPS6533, MPS6535
	–	0.13	0.3			MPS6534
$V_{BE(sat)}$	–	0.84	1.0	Vdc	I_C = 100 mAdc, I_B = 10 mAdc	MPS6533, MPS6534
	–	0.87	1.2			MPS6535
C_{ob}	–	4.8	6.0	pF	V_{CB} = 10 Vdc, I_E = 0, f = 100 kHz	
f_T	–	260	–	MHz	I_C = 50 mAdc, V_{CE} = 10 Vdc	

2N2696Ⓔ

Package TO-18

PNP VHF AMPLIFIERS, HIGH CURRENT SWITCHES

The ITT 2N2696, ia a PNP silicon PLANAR epitaxial transistor designed for digital and analog applications at current levels to 500 milliamperes. The high gain-bandwidth product, f_t, at high currents, makes them excellent units for line driving and memory applications.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Characteristics	Units
Collector-Base Voltage	−25 Volts
Collector-Emitter Voltage (Note 4)	−25 Volts
Emitter-Base Voltage	−4.0 Volts
Collector Current (Note 2)	500 mA
Total Dissipation @:	
T_C = 25°C (Notes 2 and 3)	1.2 Watts
T_C = 100°C (Notes 2 and 3)	0.68 Watt
T_A = 25°C (Notes 2 and 3)	0.36 Watt
Storage Temperature	−65°C to +200°C
Operating Junction Temperature	200°C Maximum
Lead Temperature (Soldering, 60 sec Time Limit)	300°C Maximum

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Min	Max	Unit	Conditions
h_{FE}	30	130	–	I_C = 50 mA, V_{CE} = −1.0 Volt (Note 5)
h_{FE}	20	–	–	I_C = 300 mA, V_{CE} = −2.0 Volts (Note 5)
$h_{FE(-55°C)}$	12	–	–	I_C = 50 mA, V_{CE} = −1.0 Volt (Note 5)
$V_{BE(sat)}$	–	−1.1	Volts	I_C = 50 mA, I_B = 2.5 mA
$V_{BE(sat)}$	–	−2.0	Volts	I_C = 300 mA, I_B = 30 mA
$V_{CE(sat)}$	–	−0.25	Volt	I_C = 50 mA, I_B = 2.5 mA
$V_{CE(sat)}$	–	−1.0	Volt	I_C = 300 mA, I_B = 30 mA
h_{fe}	1.0	–	–	I_C = 50 mA, V_{CE} = −3.0 Volts f=100MHz
C_{ob}	–	20	pF	I_E = 0, V_{CB} = −10 Volts
I_{CBO}	–	25	nA	I_E = 0, V_{CB} = −10 Volts
$I_{CBO(150°C)}$	–	5.0	μA	I_E = 0, V_{CB} = −10 Volts

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Min	Max	Unit	Conditions
BV_{CBO}	−25	–	Volts	I_C = 100 μA, I_E = 0
$V_{CEO(sust)}$	−25	–	Volts	I_C = 30 mA (pulsed), I_B = 0
BV_{EBO}	−4.0	–	Volts	I_C = 0, I_E = 100 μA
T_{on}	–	75	nsec	$I_C \approx$ 300 mA, $I_{B1} \approx$ 30 mA
T_{off}	–	170	nsec	$I_C \approx$ 300 mA, $I_{B1} \approx$ 30 mA, $I_{B2} \approx$ 30 mA

NOTES:

(1) These ratings are limiting values above which the serviceability of any individual semiconductor may be impaired.

(2) These are steady state limits. The factory should be consulted on applications involving pulsed or low duty cycle operations.

(3) These ratings give a maximum junction temperature of 200°C and junction-to-case thermal resistance for the 2N2696 of 145°C/watt (derating factor of 6.9 mW/°C). Junction-to-ambient thermal resistance of 486°C/watt (derating factor 2.1 mW/°C).

(4) Rating refers to a high-curent point where collector-to-emitter voltage is lowest.

(5) Pulse Conditions: length = 300 usec; duty cycle = 1%.

2N2801, 2N2837

NPN SILICON SWITCHING TRANSISTOR

Packages:
2N2801, TO-5
2N2837, TO-18

ABSOLUTE MAXIMUM RATINGS

Characteristics	Unit
Collector-Base Voltage	50 Volts
Collector-Emitter Voltage	35 Volts
Emitter-Base Voltage	5 Volts
Collector Current	800 mA
Total Device Dissipation @ $T_A = 25°C$	
(2N2801)	0.8 Watt
Derate above 25°C	4.57 mW/°C
(2N2837)	0.5 Watt
Derate above 25°C	2.86 mW/°C
Total Device Dissipation @ $T_C = 25°C$	
(2N2801)	3 Watts
Derate above 25°C	17.3 mW/°C
(2N2837)	1.8 Watts
Derate above 25°C	10.3 mW/°C
Junction Temperature, Operating	+200 °C
Storage Temperature	−65°C to +200 °C

ELECTRICAL CHARACTERISTICS ($T_A = 25°C$ unless otherwise noted)

Symbol	Min	Max	Unit	Conditions
BV_{CBO}	50	–	Volts	$I_C = 10\mu A$, $I_E = 0$
BV_{EBO}	5	–	Volts	$I_E = 100\mu A$, $I_C = 0$
BV_{CEO}	35	–	Volts	$I_C = 100$ mA, $I_B = 0$
I_{CEX}	–	100	nA	$V_{CE} = 25$ Volts, $V_{BE} = 0.5$ Volt
I_{BL}	–	100	nA	$V_{CE} = 25$ Volts, $V_{BE} = 0.5$ Volt
h_{FE}	20	–	–	$I_C = 0.1$ mA, $V_{CE} = 10$ Volts (2N2837)
h_{FE}	30	–	–	$I_C = 0.1$ mA, $V_{CE} = 10$ Volts (2N2801)
h_{FE}	30	90	–	$I_C = 150$ mA, $V_{CE} = 10$ Volts* (2N2837)
h_{FE}	75	225	–	$I_C = 150$ mA, $V_{CE} = 10$ Volts* (2N2801)
h_{FE}	15	–	–	$I_C = 150$ mA, $V_{CE} = 1$ Volt* (2N2837)
h_{FE}	30	–	–	$I_C = 150$ mA, $V_{CE} = 1$ Volt* (2N2801)

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Min	Max	Unit	Conditions
h_{FE}	25	–	–	I_C = 500 mA, V_{CE} = 10 Volts* (2N2837)
h_{FE}	40	–	–	I_C = 500 mA, V_{CE} = 10 Volts* (2N2801)
$V_{CE(sat)}$	–	0.4	Volt	I_C = 150 mA, I_B = 15 mA
$V_{CE(sat)}$	–	1.2	Volts	I_C = 500 mA, I_B = 50 mA
$V_{BE(sat)}$	–	1.3	Volts	I_C = 150 mA, I_B = 15 mA
$V_{BE(sat)}$	–	1.8	Volts	I_C = 500 mA, I_B = 50 mA
C_{ob}	–	25	pF	V_{CB} = 10 Volts, f = 100 kHz
f_T	120	–	MHz	I_C = 50 mA, V_{CE} = 10 Volts, f = 100 MHz

* Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%

SWITCHING CHARACTERISTICS
(At 25°C unless otherwise noted)

Characteristics	Typ	Max	Unit
Delay Time	9	25	ns
Rise Time	25	45	ns
Storage Time	100	225	ns
Fall Time	30	45	ns

SCHEMATIC

FIGURE 1 – DELAY AND RISE TIME TEST CIRCUIT

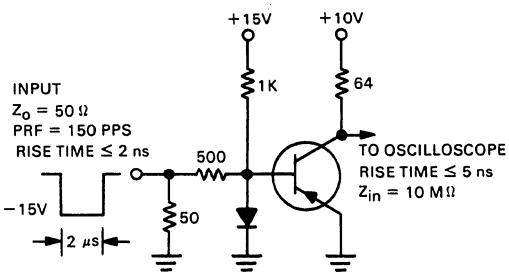
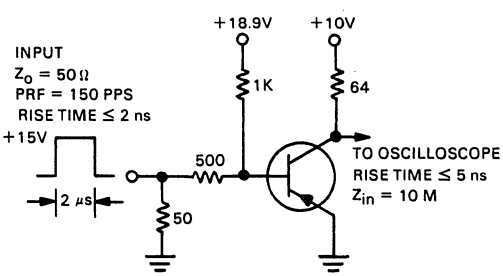


FIGURE 2 – STORAGE AND FALL TIME TEST CIRCUIT



2N3134
HIGH-SPEED NPN SILICON SWITCHING AND AMPLIFIER TRANSISTOR

Package: TO-5

ABSOLUTE MAXIMUM RATINGS

Characteristics	Unit
Collector-Base Voltage	50 Volts
Collector-Emitter Voltage	35 Volts
Emitter-Base Voltage	4 Volts
Collector Current	600 mA
Total Device Dissipation @ $T_C = 25°C$	3 Watts
Derate above 25°C	17.3 mW/°C
Total Device Dissipation @ $T_A = 25°C$	0.6 Watts
Derate above 25°C	3.43 mW/°C
Junction Temperature	−65 to +200 °C
Storage Temperature	−65 to +200 °C

ELECTRICAL CHARACTERISTICS ($T_A = 25°C$ unless otherwise noted)

Symbol	Min	Max	Unit	Conditions
I_{CBO}	–	0.05	μA	$V_{CB} = 30$ Volts, $I_E = 0$
I_{CBO}	–	30	μA	$V_{CB} = 30$ Volts, $I_E = 0$, $T_A = 150°C$
I_{CEX}	–	0.1	μA	$V_{CE} = 30$ Volts, $V_{BE} = 0.5$ Volt
I_{BL}	–	0.1	μA	$V_{CE} = 30$ Volts, $V_{BE} = 0.5$ Volt
BV_{CBO}	50	–	Volts	$I_C = 10$ uA, $I_E = 0$
BV_{CEO}*	35	–	Volts	$I_C = 10$ mA, $I_B = 0$*
BV_{EBO}	4	–	Volts	$I_E = 10$ uA, $I_C = 0$
$V_{CE(sat)}$*	–	0.6	Volt	$I_C = 150$ mA, $I_B = 15$ mA*
$V_{BE(sat)}$*	–	1.5	Volts	$I_C = 150$ mA, $I_B = 15$ mA*
h_{FE}	50	–	–	$I_C = 1.0$ mA, $V_{CE} = 10$ Volts
h_{FE}	100	300	–	$I_C = 150$ mA, $V_{CE} = 10$ Volts*
C_{ob}	–	10	pF	$V_{CB} = 10$ Volts, $I_E = 0$, f = 100 kHz
C_{ib}	–	40	pF	$V_{BE} = 2$ Volts, $I_C = 0$, f = 100 kHz
f_T	200	–	MHz	$I_C = 50$ mA, $V_{CE} = 20$ Volts, f = 100 MHz

* Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%

Package: TO-18

HIGH-SPEED PNP SILICON SWITCHING TRANSISTOR

ABSOLUTE MAXIMUM RATINGS

Characteristics	Unit
Collector-Base Voltage	15 Volts
Collector-Emitter Voltage	12 Volts
Emitter-Base Voltage	4.5 Volts
Total Device Dissipation @ T_A = 25°C	0.36 Watt
Derate above 25°C	2.06 mW/°C
Total Device Dissipation @ T_C = 25°C	1.2 Watts
Derate above 25°C	6.9 mW/°C
Operating Junction Temperature	200 °C
Storage Temperature Range	−65 to +200 °C
Thermal Resistance, Junction to Ambient	0.49 °C/mW
Thermal Resistance, Junction to Case	0.15 °C/mW

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Min	Max	Unit	Conditions
I_{CBO}	–	0.010	μA	V_{CB} = 10 Volts
I_{CBO}	–	10	μA	V_{CB} = 10 Volts, T_A = 150°C
I_{CEX}	–	0.010	μA	V_{CE} = 10 Volts, $V_{BE(off)}$ = 3 Volts
I_{BL}	–	0.10	μA	V_{CE} = 10 Volts, $V_{BE(off)}$ = 3 Volts
BV_{CBO}	15	–	Volts	I_C = 10μA, I_E = 0
BV_{EBO}	4.5	–	Volts	I_E = 10μA, I_C = 0
BV_{CEO}*	12	–	Volts	I_C = 10 mA, I_B = 0*
$V_{CE(sat)}$*	–	0.15	Volt	I_C = 10 mA, I_B = 1 mA*
$V_{CE(sat)}$*	–	0.25	Volt	I_C = 50 mA, I_B = 5 mA*
$V_{CE(sat)}$*	–	0.50	Volt	I_C = 100 mA, I_B = 10 mA
$V_{BE(sat)}$*	0.7	0.9	Volt	I_C = 10 mA, I_B = 1 mA
$V_{BE(sat)}$*	0.8	1.3	Volts	I_C = 50 mA, I_B = 5 mA
$V_{BE(sat)}$*	–	1.6	Volts	I_C = 100 mA, I_B = 10 mA
h_{FE}*	20	–	–	I_C = 1.0 mA, V_{CE} = 1 Volt*
h_{FE}*	30	120	–	I_C = 10 mA, V_{CE} = 1 Volt
h_{FE}*	15	–	–	I_C = 10 mA, V_{CE} = 1 Volt, T_A = −55°C

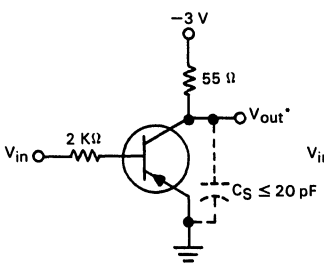
ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

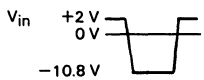
Symbol	Min	Max	Unit	Conditions
h_{FE}*	25	–	–	I_C = 50 mA, V_{CE} = 1 Volt
h_{FE}*	15	–	–	I_C = 100 mA, V_{CE} = 1 Volt
C_{ob}	–	6	pF	V_{CB} = 10 Volts, I_E = 0, f = 1 MHz
C_{ib}	–	5	pF	V_{BE} = 0.5 Volt, I_C = 0, f = 1 MHz
f_T	700	–	MHz	I_C = 10 mA, V_{CE} = 10 Volts, f = 100 MHz
Q_T	–	400	pC	I_C = 50 mA, I_B = 5 mA, V_{CC} = 3 Volts
t_d	–	10	ns	I_C = 50 mA, I_B = 5 mA,
t_r	–	15	ns	V_{BE} = 2 Volts, V_{CC} = 3 Volts
t_s	–	20	ns	I_C = 50 mA, I_{B1} = I_{B2} = 5 mA,
t_f	–	15	ns	V_{CC} = 3 Volts
t_{on}	–	40	ns	(See Figure 3,4,5)
t_{off}	–	30	ns	

* Pulse Test: PW = 300 μs, Duty Cycle ≤ 2%

CIRCUIT DIAGRAM

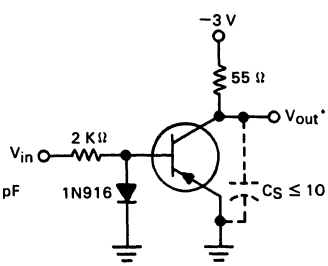
FIGURE 1
DELAY AND RISE TIME
EQUIVALENT TEST CIRCUIT

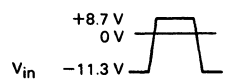




PULSE WIDTH = 200 ns
RISE TIME ≤ 2 ns
DUTY CYCLE ≤ 10%

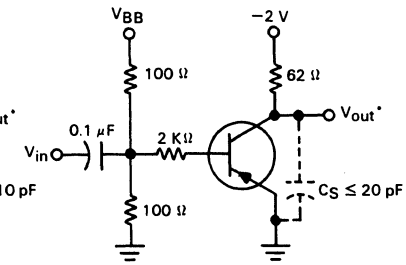
FIGURE 2
STORAGE AND FALL TIME
EQUIVALENT TEST CIRCUIT





PULSE WIDTH = 200 ns
RISE TIME ≤ 2 ns
DUTY CYCLE ≤ 10%

FIGURE 3
SWITCHING TIME TEST CIRCUIT



PULSE WIDTH > 200 ns
RISE TIME < 1 ns
Z_{in} = 50 Ω

t_{on}: V_{BB} = +3 V, V_{in} = −7 V
t_{off}: V_{BB} = −4 V, V_{in} = +6 V

*OSCILLOSCOPE RISE TIME ≤ 1 ns

ABSOLUTE MAXIMUM RATINGS

Characteristics	Unit
Collector-Emitter Voltage	40 Volts
Collector-Base Voltage	40 Volts
Emitter-Base Voltage	5.0 Volts
Collector Current	200 mA
Total Device Dissipation @ T_A = 25°C	310 mW
Total Device Dissipation @ T_A = 60°C	210 mW
Derate above 25°C	2.81 mW/°C
Operating and Storage Junction Temperature Range	−55 to +135 °C
Thermal Resistance, Junction to Ambient	0.357 °C/mW

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Min	Max	Unit	Conditions
BV_{CBO}	40	–	Volts	I_C = 10μA, I_E = 0
BV_{CEO}*	40	–	Volts	I_C = 1.0 mA, I_B = 0
BV_{EBO}	5.0	–	Volts	I_E = 10μA, I_C = 0
I_{CEX}	–	50	nA	V_{CE} = 30 Volts, $V_{BE(off)}$ = 3.0 Volts
I_{BL}	–	50	nA	V_{CE} = 30 Volts, $V_{BE(off)}$ = 3.0 Volts
h_{FE}*	30	–	–	(2N3905) I_C = 0.1 mA, V_{CE} = 1.0 Volt
	60	–	–	(2N3906)
h_{FE}*	40	–	–	(2N3905) I_C = 1.0 mA, V_{CE} = 1.0 Volt
	80	–	–	(2N3906)
h_{FE}*	50	150	–	(2N3905) I_C = 10 mA, V_{CE} = 1.0 Volt
	100	300	–	(2N3906)
h_{FE}*	30	–	–	(2N3905) I_C = 50 mA, V_{CE} = 1.0 Volt
	60	–	–	(2N3906)
h_{FE}*	15	–	–	(2N3905) I_C = 100 mA, V_{CE} = 1.0 Volt
	30	–	–	(2N3906)
$V_{CE(sat)}$*	–	0.25	Volt	I_C = 10 mA, I_B = 1.0 mA
	–	0.4	Volt	I_C = 50 mA, I_B = 5.0 mA

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Min	Max	Unit	Conditions
$V_{BE(sat)}$*	0.65	0.85	Volt	I_C = 10 mA, I_B = 1.0 mA
	–	0.95	Volt	I_C = 50 mA, I_B = 5.0 mA
f_T	200	–	MHz	(2N3905) I_C = 10 mA, V_{CE} = 20 Volts,
	250	–	MHz	(2N3906) f = 100 MHz
C_{ob}	–	4.5	pF	V_{CB} = 5.0 Volts, I_E = 0, f = 100 kHz
C_{ib}	–	10	pF	V_{BE} = 0.5 Volt, I_C = 0, f = 100 kHz
h_{ie}	0.5	8.0	k ohms	(2N3905) I_C = 1.0 mA, V_{CE} = 10 Volts,
	2.0	12	k ohms	(2N3906) f = 1.0 kHz
h_{re}	0.1	5.0	X 10^{-4}	(2N3905) I_C = 1.0 mA, V_{CE} = 10 Volts,
	1.0	10	X 10^{-4}	(2N3906) f = 1.0 kHz
h_{fe}	50	200	–	(2N3905) I_C = 1.0 mA, V_{CE} = 10 Volts,
	100	400	–	(2N3906) f = 1.0 kHz
h_{oe}	1.0	40	μmhos	(2N3905) I_C = 1.0 mA, V_{CE} = 10 Volts,
	3.0	60	μmhos	(2N3906) f = 1.0 kHz
NF	–	5.0	dB	(2N3905) I_C = 100 μA, V_{CE} = 5.0 Volts,
	–	4.0	dB	(2N3906) R_S = 1.0 k ohm, f = 10 Hz to 15.7 kHz
t_d	–	35	ns	V_{CC} = 3.0 Volts, $V_{BE(off)}$ = 0.5 Volt,
t_r	–	35	ns	I_C = 10 mA, I_{B1} = 1.0 mA
t_s	–	200	ns	(2N3905) V_{CC} = 3.0 Volts, I_C = 10 mA,
	–	225	ns	(2N3906) I_{B1} = I_{B2} = 1.0 mA
t_f	–	60	ns	(2N3905) V_{CC} = 3.0 Volts, I_C = 10 mA,
	–	75	ns	(2N3906) I_{B1} = I_{B2} = 1.0 mA

* Pulse Test: Pulse Width = 300 μs, Duty Cycle = 2.0%.

SCHEMATIC

FIGURE 1 – DELAY AND RISE TIME EQUIVALENT TEST CIRCUIT

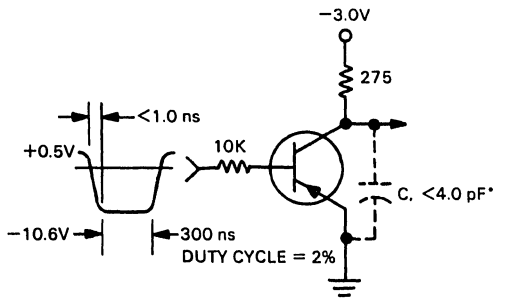
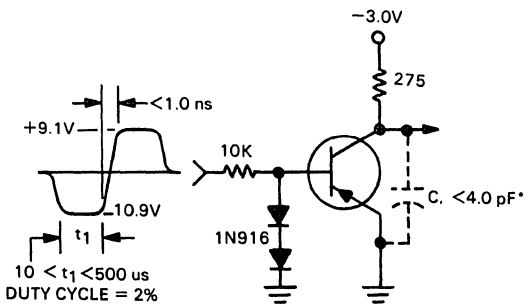


FIGURE 2 – STORAGE AND FALL TIME EQUIVALENT TEST CIRCUIT



*Total shunt capacitance of test jig and connectors

2N4026, 2N4027, 2N4028, 2N4029®

PNP SILICON HIGH-VOLTAGE GENERAL PURPOSE AMPLIFIER TRANSISTORS

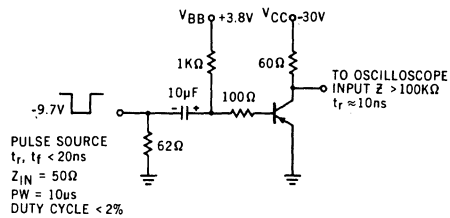
Package: TO-18

- **HIGH BETA** ..... 100 - 300 @ 100 mA
- **HIGH VOLTAGE** ..... 60 AND 80 VOLTS LV_{CEO}
- **LOW $V_{CE(sat)}$** ..... 1.0 VOLT (MAX) @ 1.0 A
- **EXCELLENT BETA LINEARITY** ..... FROM 100 μA TO 500 mA

ABSOLUTE MAXIMUM RATINGS (Note 1)

Characteristics	Unit
Collector-Base Voltage	
(2N4026, 2N4028)	−60 Volts
(2N4027, 2N4029)	−80 Volts
Collector-Emitter Voltage (Note 4)	
(2N4026, 2N4028)	−60 Volts
(2N4027, 2N4029)	−80 Volts
Emitter-Base Voltage	
(2N4026, 2N4027, 2N4028, 2N4029)	−5.0 Volts
Total Device Dissipation @:	
T_C = 25°C (Notes 2 and 3)	2.0 Watts
T_{AF} = 25°C (Notes 2 and 3)	0.5 Watt
Storage Temperature	−65°C to +200°C
Operating Junction Temperature	+200°C Maximum
Lead Temperature (Soldering, 60 sec Time Limit)	+300°C Maximum

T_{on} AND T_{off} TEST CIRCUIT



ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol		Min	Typ	Max	Unit	Conditions
h_{FE}	2N4026, 2N4027	30	80	-	-	I_C = 100 μA, V_{CE} = −5.0 Volts (Note 5)
	2N4028, 2N4029	75	150	-	-	
h_{FE}	2N4026, 2N4027	40	80	120	-	I_C = 100 mA, V_{CE} = −5.0 Volts (Note 5)
	2N4028, 2N4029	100	160	300	-	
h_{FE}	2N4026, 2N4027	25	60	-	-	I_C = 500 mA, V_{CE} = −5.0 Volts (Note 5)
	2N4028, 2N4029	70	110	-	-	
h_{FE}	2N4026	15	-	-	-	I_C = 1.0 A, V_{CE} = −5.0 Volts (Note 5)
	2N4028	40	-	-	-	
h_{FE}	2N4027	10	-	-	-	I_C = 1.0 A, V_{CE} = −5.0 Volts (Note 5)
	2N4029	25	-	-	-	
$h_{FE(-55°C)}$	2N4026, 2N4027	15	50	-	-	I_C = 100 mA, V_{CE} = −5.0 Volts (Note 5)
	2N4028, 2N4029	40	100	-	-	
h_{fe}	2N4026, 2N4027	1.0	1.5	4.0	-	I_C = 50 mA, V_{CE} = −10 Volts
	2N4028, 2N4029	1.5	2.0	5.0	-	

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol		Min	Typ	Max	Unit	Conditions
C_{obo}	2N4026, 2N4027 2N4028, 2N4029	-	15	20	pF	I_E = 0, V_{CB} = −10 Volts
C_{ibo}	2N4026, 2N4027 2N4028, 2N4029	-	75	110	pF	I_C = 0, V_{EB} = −0.5 Volt
t_{on}	2N4026, 2N4027 2N4028, 2N4029	-	30 23	100 100	ns ns	$I_C \approx$ 500 mA, $I_{B1} \approx$ 50 mA (Note 6)
t_s	2N4026, 2N4027 2N4028, 2N4029	-	150 175	350 350	ns ns	$I_C \approx$ 500 mA, $I_{B1} \approx$ 50 mA, $I_{B2} \approx$ −50 mA (Note 6)
t_f	2N4026, 2N4027 2N4028, 2N4029	-	25 22	50 50	ns ns	$I_C \approx$ 500 mA, $I_{B1} \approx$ 50 mA, $I_{B2} \approx$ −50 mA (Note 6)
$V_{CE(sat)}$	2N4026, 2N4028 2N4027, 2N4029		−0.1	−0.15	Volts	I_C = 150 mA, I_B = 15 mA (Note 5)
$V_{CE(sat)}$	2N4026, 2N4028 2N4027, 2N4029		−0.25	−0.5	Volts	I_C = 500 mA, I_B = 50 mA (Note 5)
$V_{CE(sat)}$	2N4026, 2N4028		−0.5	−1.0	Volt	I_C = 1000 mA, I_B = 100 mA (Note 5)
$V_{BE(sat)}$	2N4026, 2N4028 2N4027, 2N4029		−0.8	−0.9	Volt	I_C = 150 mA, I_B = 15 mA (Note 5)
$V_{BE(sat)}$	2N4026, 2N4028 2N4027, 2N4029	-	- −0.95	−1.1 −1.1	Volts Volts	I_C = 500 mA, I_B = 50 mA (Note 5)
$V_{BE(sat)}$	2N4026, 2N4028	-	−1.05	−1.2	Volts	I_C = 1000 mA, I_B = 100 mA (Note 5)
BV_{CBO}	2N4026, 2N4028 2N4027, 2N4029	−60 −80	-	-	Volts Volts	I_E = 0, I_C = 10 μA
BV_{EBO}	2N4026, 2N4028 2N4026, 2N4028	−5.0	-	-	Volts	I_C = 0, I_E = 10 μA
$V_{CEO(sust)}$	2N4026, 2N4028 2N4027, 2N4029	−60 −80	-	-	Volts Volts	I_C = 10 mA (pulsed), I_B = 0 (Notes 4 and 5)
I_{CBO}	2N4026, 2N4028	-	0.2	50	nA	I_E = 0, V_{CB} = −50 Volts
I_{CBO}	2N4027, 2N4029	-	0.2	50	nA	I_E = 0, V_{CB} = −60 Volts
$I_{CBO(150°C)}$	2N4026, 2N4028	-	0.2	50	μA	I_E = 0, V_{CB} = −50 Volts
$I_{CBO(150°C)}$	2N4027, 2N4029	-	0.25	50	μA	I_E = 0, V_{CB} = −60 Volts

(1) These ratings are limiting values above which the serviceability of any individual semiconductor device may be impaired.

(2) These are steady state limits. The factory should be consulted on applications involving pulsed or low duty cycle operations.

(3) These ratings give a maximum junction temperature of 200°C and junction-to-case thermal resistance of 87.5°C/watt (derating factor of 11.4 mW/°C); junction-to-ambient thermal resistance of 350°C/watt (derating factor of 2.85 mW/°C).

(4) Rating refers to a high-current point where collector-to-emitter voltage is lowest.

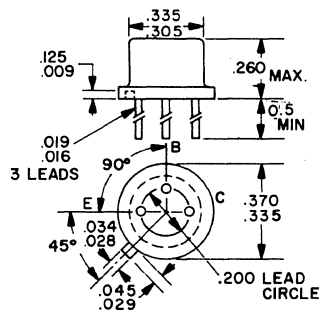
(5) Pulse Conditions: length = 300 μs; duty cycle = 1%.

(6) See switching circuit for exact values of I_C, I_{B1}, and I_{B2}.

GENERAL PURPOSE HIGH-VOLTAGE PNP SILICON PLANAR EPITAXIAL TRANSISTORS

- **High Voltage: −80V (2N4031, 3)**
- **High Gain: 100 min. @ 100mA (2N4032, 3)**
- **Low V_{CE} (sat): −0.15V @ 150mA**

DIMENSIONS



TO-5

The ITT 2N4030, 2N4031, 2N4032, 2N4033 are high voltage PNP silicon planar epitaxial transistors useful in a variety of applications. Excellent linearity of current gain, high breakdown voltage and low saturation voltage combine in this 150MHz f_t device to increase the possible uses for this device. Primary applications are high voltage output stages and complementary drivers.

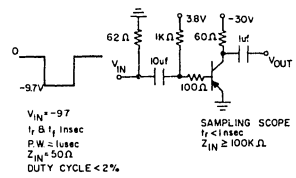
ABSOLUTE MAXIMUM RATINGS

CHARACTERISTICS	2N4030 2N4032	2N4031 2N4033	UNITS
Collector-to-Base Voltage	−60	−80	Volts
Collector-to-Emitter Voltage (open base)	−60	−80	Volts
Emitter-to-Base Voltage	−5	−5	Volts
Collector Current	1.0	1.0	Amps
Junction Temperature (op. and stg.)	−65 to +200		°C
Total Dissipation @ T_C=25°C	4.0		Watts
(derate above 25°C)	22.8		mW/°C
Total Dissipation @ T_A=25°C	0.8		Watts
(derate above 25°C)	4.56		mW/°C

ELECTRICAL CHARACTERISTICS @ 25°C unless otherwise noted.

SYMBOL	2N4030 MIN.	2N4030 MAX.	2N4031 MIN.	2N4031 MAX.	2N4032 MIN.	2N4032 MAX.	2N4033 MIN.	2N4033 MAX.	UNIT	CONDITIONS
BV_{CBO}	−60		−80		−60		−80		Vdc	I_C= −10μA
LV_{CEO}[1,2]	−60		−80		−60		−80		Vdc	I_C= −10mA
BV_{EBO}	−5.0		−5.0		−5.0		−5.0		Vdc	I_C= −10μA
h_{FE}[1]	40	120	40	120	100	300	100	300		I_C= −100mA V_{CE}= −5V
	30		30		75		75			I_C= −100μA V_{CE}= −5V
	25		25		70		70			I_C= −500mA V_{CE}= −5V
	15		15		40		40			I_C= −100mA V_{CE}= −5V
										T_A= −55°C
	15		10		40		25			I_C= −1A V_{CE}= −5V
$V_{CE}(sat)$[1]		−0.15		−0.15		−0.15		−0.15	Vdc	I_C= −150mA I_B= −15mA
		−0.50		−0.50		−0.50		−0.50	Vdc	I_C= −500mA I_B= −50mA
		−1.0				−1.0			Vdc	I_C= −1A I_B= −100mA
$V_{BE}(sat)$[1]		−0.9		−0.9		−0.9		−0.9	Vdc	I_C= −150mA I_B= −15mA
$V_{BE}(on)$		−1.1		−1.1		−1.1		−1.1	Vdc	I_C= −500mA V_{CE}= −0.5V
		−1.2				−1.2			Vdc	I_C= −1A V_{CE}= −1V
I_{CBO}		−50				−50			nAdc	V_{CB}= −50V
				−50				−50	nAdc	V_{CB}= −60V
		−50				−50			μAdc	V_{CB}= −50V T_A=150°C
				−50				−50	μAdc	V_{CB}= −60V T_A=150°C
I_{EBO}		−10		−10		−10		−10	μAdc	V_{EB}= −5V
C_{ob}		20		20		20		20	pF	V_{CB}= −10V f=1MHz
C_{ib}		110		110		110		110	pF	V_{EB}= −0.5V f=1MHz
$\|h_{fe}\|$	1.0	4.0	1.0	4.0	1.5	5.0	1.5	5.0		V_{CE}= −10V I_C= −50mA f=100MHz
t_{on}		100		100		100		100	ns	$I_C \approx 500mA$ $I_{B1} \approx 50mA$ $I_{B2} \approx 50mA$
t_s		350		350		350		350	ns	
t_f		50		50		50		50	ns	

SWITCHING TIME TEST CIRCUIT



2N4402, 2N4403

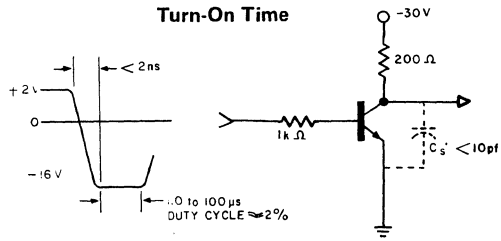
Package: To-92

GENERAL PURPOSE PNP SILICON SWITCHING AND AMPLIFYING TRANSISTOR

ABSOLUTE MAXIMUM RATINGS

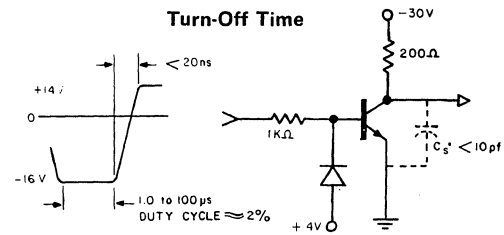
Characteristic	Unit
Collector-Emitter Voltage	40 Vdc
Collector-Base Voltage	40 Vdc
Emitter-Base Voltage	5.0 Vdc
Collector Current - Continuous	600 mAdc
Total Device Dissipation T_A = 25°C	310 mW
Derate above 25°C	2.81 mW/°C
Operating & Storage Junction Temperature Range	-55 to +135 °C
Thermal Resistance, Junction To Case	0.137 °C/mW
Thermal Resistance, Junction To Ambient	0.357 °C/mW

Turn-On Time



SCOPE RISE TIME 4ns
TOTAL SHUNT CAPACITANCE OF TEST JIG, CONNECTORS, AND OSCILLOSCOPE

Turn-Off Time



ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Min	Max	Unit	Conditions	
BV_{CEO}*	40	–	Vdc	I_C = 1 mAdc, I_B = 0	
BV_{CBO}	40	–	Vdc	I_C = 0.1 mAdc, I_E = 0	
BV_{EBO}	5.0	–	Vdc	I_E = 0.1 mAdc, I_C = 0	
I_{CEX}	–	0.1	*u*Adc	V_{CE} = 35 Vdc, $V_{BE(off)}$ = 0.4 Vdc	
I_{BL}	–	0.1	*u*Adc	V_{CE} = 35 Vdc, $V_{BE(off)}$ = 0.4 Vdc	
h_{FE}	30	–		I_C = 0.1 mAdc, V_{CE} = 1 Vdc	2N4403
	30	–		I_C = 1 mAdc, V_{CE} = 1 Vdc	2N4402
	60	–			2N4403
	50	–		I_C = 10 mAdc, V_{CE} = 1 Vdc	2N4402
	100	–			2N4403
	50	150		I_C = 150 mAdc, V_{CE} = 2 Vdc*	2N4402
	100	300			2N4403
	20	–		I_C = 500 mAdc, V_{CE} = 2 Vdc*	
$V_{CE(sat)}$	–	0.4	Vdc	I_C = 150 mAdc, I_B = 15 mAdc	
	–	0.75		I_C = 500 mAdc, I_B = 50 mAdc	
$V_{BE(sat)}$	0.75	0.95	Vdc	I_C = 150 mAdc, I_B = 15 mAdc	
	–	1.3		I_C = 500 mAdc, I_B = 50 mAdc	
f_T	150	–	MHz	2N4402 I_C = 20 mAdc, V_{CE} = 10 Vdc,	
	200	–		2N4403 f=100 MHz	

*Pulse Test: Pulse Width = 300 us, Duty Cycle = 2%.

ELECTRICAL CHARACTERISTICS ($T_A = 25°C$)

SYMBOL	MIN.	MAX.	UNITS	CONDITIONS
C_{cb}	–	8.5	pF	V_{CB} = 10 Vdc, I_E = 0, f = 140 kHz, emitter guarded
C_{eb}	–	30	pF	V_{BE} = 0.5 Vdc, I_C = 0, f - 140 kHz, collector guarded
h_{ie}	750 1.5k	7.5k 15k	ohms	I_C - 1 mAdc, V_{CE} = 10 Vdc, f = 1 kHz 2N4402 2N4403
h_{re}	0.1	8.0	X 10^{-4}	I_C = 1 mAdc, V_{CE} = 10 Vdc, f = 1 kHz
h_{fe}	30 60	250 500	–	I_C = 1 mAdc, V_{CE} = 10 Vdc, f = 1 kHz 2N4402 2N4403
h_{oe}	1.0	100	*u*mhoe	I_C = 1 mAdc, V_{CE} = 10 Vdc, f = 1 kHz
t_d	–	15	ns	V_{CC} = 30 Vdc, $V_{BE(off)}$ = 2 Vdc,
t_r	–	20	ns	I_C = 150 mAdc, I_{B1} = 15 mAdc
t_s	–	225	ns	V_{CC} = 30 Vdc, I_C = 150 mAdc,
t_f	–	30	ns	$I_{B1} = I_{B2}$ = 15 mAdc

2N5056, 2N5057Ⓕ

Package: TO-18

HIGH SPEED PNP SILICON SATURATED SWITCHING TRANSISTORS

- **Fast Switching** ..... t_{on} = 20 ns (max) at 30 mA
  t_{off} = 35 ns (max) at 30 mA
  τ_s = 30 ns (max) at 10 mA
- **High Frequency** ..... f_T = 800 MHz (min) at 30 mA
- **Low Capacitance** ..... C_{cb} = 4.5 pF (max) at 5 Volts
- **Low Saturation Voltage** ..... $V_{CE(sat)}$ = 0.19 Volts (max) at I_C = 30 mA

ABSOLUTE MAXIMUM RATINGS (Note 1)

Characteristics	Unit
Storage Temperature	−65°C to +200°C
Operating Junction Temperature	+200°C
Lead Temperature (Soldering, 60 second time limit)	+300°C
Total Device Dissipation:	
@ T_C = 25°C (Notes 2 and 3)	1.2 Watts
@ T_C = 100°C (Notes 2 and 3)	0.72 Watt
@ T_A = 25°C (Notes 2 and 3)	0.36 Watt
Collector-Base Voltage	−15 Volts
Collector-Emitter Voltage (Note 4)	−15 Volts
Emitter-Base Voltage	−4.5 Volts

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol		Min	Typ	Max	Unit	Conditions
t_{on}	2N5056	–	10	20	ns	$I_C \approx 30$ mA, $I_{B1} \approx 3.0$ mA
	2N5057	–	10	20	ns	(Note 6, Figure 1)
t_{off}	2N5056	–	15	35	ns	$I_C \approx 30$ mA, $I_B = I_{B2} \approx 3.0$ mA
	2N5057	–	15	35	ns	(Note 6, Figure 1)
τ_s	2N5056	–	15	30	ns	$I_C \approx 10$ mA, $I_{B1} \approx 10$ mA,
	2N5057	–	15	30	ns	$I_{B2} \approx -10$ mA (Note 6, Figure 1)
$V_{CE(sat)}$	2N5056	–	−0.08	−0.13	Volt	I_C = 10 mA, I_B = 1.0 mA
	2N5057	–	−0.08	−0.13	Volt	(Note 5)
$V_{CE(sat)}$	2N5056	–	−0.12	−0.19	Volt	I_C = 30 mA, I_B = 3.0 mA
	2N5057	–	−0.12	−0.19	Volt	(Note 5)
$V_{CE(sat)}$	2N5056	–	−0.28	−0.45	Volt	I_C = 100 mA, I_B = 10 mA
	2N5057	–	−0.28	−0.45	Volt	(Note 5)
$V_{BE(sat)}$	2N5056	−0.72	−0.82	−0.92	Volt	I_C = 10 mA, I_B = 1.0 mA
	2N5057	−0.72	−0.82	−0.92	Volt	(Note 5)
$V_{BE(sat)}$	2N5056	−0.80	−0.93	−1.15	Volts	I_C = 30 mA, I_B = 3.0 mA
	2N5057	−0.80	−0.93	−1.15	Volts	(Note 5)

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol		Min	Typ	Max	Unit	Conditions
$V_{BE(sat)}$	2N5056	−0.95	−1.14	−1.5	Volts	I_C = 100 mA, I_B = 10 mA
	2N5057	−0.95	−1.14	−1.5	Volts	
h_{fe}	2N5056	6.0	9.0	-	-	I_C = 30 mA, V_{CE} = −10 Volts
	2N5057	8.0	12	-	-	
C_{cb}	2N5056	-	3.3	4.5	pF	I_E = 0, V_{CB} = −5.0 Volts
	2N5057	-	3.3	4.5	pF	
C_{eb}	2N5056	-	4.7	6.0	pF	I_C = 0, V_{EB} = −0.5 Volt
	2N5057	-	4.7	6.0	pF	
I_{CES}	2N5056	-	0.3	50	nA	V_{CE} = −10 Volts, V_{BE} = 0
	2N5057	-	0.3	50	nA	
I_{CES}(+125°C)	2N5056	-	0.05	10	μA	V_{CE} = −10 Volts, V_{BE} = 0
	2N5057	-	0.05	10	μA	
$V_{CEO(sust)}$	2N5056	−15	-	-	Volts	I_C = 10 mA, I_E = 0
	2N5057	−15	-	-	Volts	(Notes 4 and 5)
BV_{CBO}	2N5056	−15	-	-	Volts	I_C = 10 μA, I_E = 0
	2N5057	−15	-	-	Volts	
BV_{CES}	2N5056	−15	-	-	Volts	I_C = 10 μA, V_{BE} = 0
	2N5057	−15	-	-	Volts	
BV_{EBO}	2N5056	−4.5	-	-	Volts	I_C = 0, I_E = 100 μA
	2N5057	−4.5	-	-	Volts	
h_{FE}	2N5056	12	25	-	-	I_C = 1.0 mA, V_{CE} = −0.5 Volt
	2N5057	20	44	-	-	(Note 5)
h_{FE}	2N5056	20	33	-	-	I_C = 10 mA, V_{CE} = −0.3 Volt
	2N5057	30	53	-	-	(Note 5)
h_{FE}	2N5056	30	48	100	-	I_C = 30 mA, V_{CE} = − 0.5 Volt
	2N5057	40	63	100	-	(Note 5)
h_{FE}	2N5056	20	45	-	-	I_C = 100 mA, V_{CE} = −1.0 Volt
	2N5057	30	55	-	-	(Note 5)
h_{FE}(−55°C)	2N5056	12	25	-	-	I_C = 30 mA, V_{CE} = −0.5 Volt
	2N5057	20	38	-	-	(Note 5)

NOTES:

(1) These ratings are limiting values above which the serviceability of any individual semiconductor device may be impaired.

(2) These are steady state limits. The factory should be consulted on applications involving pulsed or low duty cycle operations.

(3) These ratings give a maximum junction temperature of 200°C and junction-to-case thermal resistance of 146°C/watt (derating factor of 6.85 mW/°C); junction-to-ambient thermal resistance of 486°C/watt (derating factor of 2.06 mW/°C).

(4) This rating refers to a high-current point where collector to emitter voltage is lowest.

(5) Pulse Conditions: length = 300 μs; duty cycle = 1%.

(6) See switching circuit for exact values of I_C, I_{B1}, and I_{B2}.

SCHEMATIC

FIGURE 1
SWITCHING TIME TEST CIRCUIT

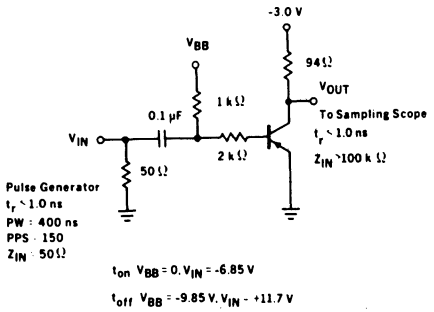


FIGURE 2
SWITCHING TIME TEST CIRCUIT

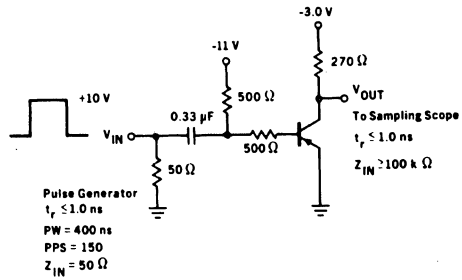


FIGURE 3
FIVE STAGE RING OSCILLATOR FOR
MEASUREMENT OF PROPAGATION DELAY

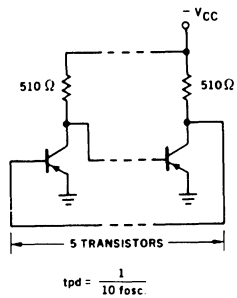
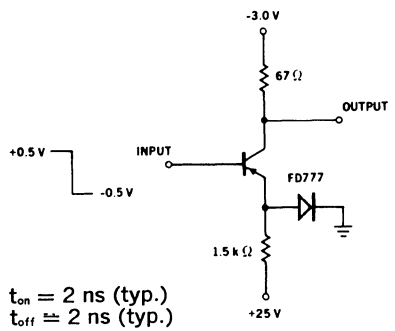


FIGURE 4
NON-SATURATED SWITCHING PERFORMANCE



Package: To-92

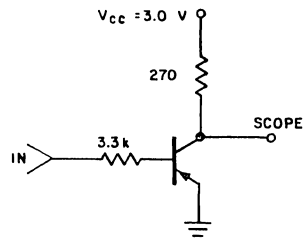
2N5228

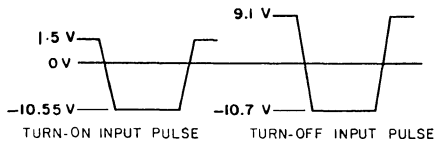
GENERAL PURPOSE PNP SILICON LOW-LEVEL SWITCHING TRANSISTOR

ABSOLUTE MAXIMUM RATINGS

Characteristic	Unit
Collector-Emitter Voltage	5.0 Vdc
Collector-Emitter Voltage	6.0 Vdc
Collector-Base Voltage	5.0 Vdc
Emitter-Base Voltage	3.0 Vdc
Collector Current	50 mAdc
Total Device Dissipation @ T_A = 25°C	310 mW
Derate above 25°C	2.81 mW/°C
Operating and Storage Junction Temperature Range	-55 to +135 °C
Thermal Resistance, Junction to Ambient	0.357 °C/mW

Figure 1 — Switching Time Test Circuit





GENERATOR SOURCE IMPEDANCE = 50 ohms

INPUT PULSE:
RISE TIME < 2.0 ns
FALL TIME < 2.0 ns
NOMINAL PULSEWIDTH = 300 ns
NOMINAL DUTY CYCLE = 2.0%

OSCILLOSCOPE:
RISE TIME 0.4ns
INPUT RESISTANCE < 50 ohms
INPUT CAPACITANCE < 4.0 pF

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Min	Max	Unit	Conditions
BV_{CEO}	5.0	—	Vdc	I_C = 10 mAdc, I_B = 0
BV_{CES}	6.0	—	Vdc	I_C = 100 uAdc, V_{BE} = 0
BV_{CBO}	5.0	—	Vdc	I_C = 100 uAdc, I_E = 0
BV_{EBO}	3.0	—	Vdc	I_E = 100 uAdc, I_C = 0
I_{CES}	—	100	nAdc	V_{CE} = 4.0 Vdc, V_{BE} = 0
I_{EBO}	—	100	uAdc	V_{BE} = 2.5 Vdc, I_C = 0
h_{FE}	30	—	—	I_C = 10 mAdc, V_{CE} = 0.3 Vdc
	15	—		I_C = 50 mAdc, V_{CE} = 1.0 Vdc
$V_{CE(sat)}$	—	0.4	Vdc	I_C = 10 mAdc, I_B = 3.0 mAdc
$V_{BE(sat)}$	0.65	1.25	Vdc	I_C = 10 mAdc, I_B = 3.0 mAdc
f_T	300	—	MHz	I_C = 10 mAdc, V_{CE} = 5.0 Vdc, f = 100 MHz
C_{cb}	—	5.0	pF	V_{CB} = 5.0 Vdc, I_E = 0, f = 1.0 MHz
t_d	—	25	ns	Delay Time See Figure 1
t_r	—	50	ns	Rise Time See Figure 1
t_s	—	90	ns	Storage Time See Figure 1
t_f	—	50	ns	Fall Time See Figure 1

2N2480, 2N2480A

Package: TO-92

NPN SILICON DUAL TRANSISTORS

ABSOLUTE MAXIMUM RATINGS (each side)

Characteristics	Unit
Collector-Emitter Voltage	40 Volts
Collector-Base Voltage (2N2480)	75 Volts
Collector-Base Voltage (2N2480A)	80 Volts
Emitter-Base Voltage	5.0 Volts
Collector Current	500 mA
Operating Junction Temperature	200°C
Storage Temperature Range	−65 to +200°C
Total Dissipation @ T_A = 25°C (one side)	0.5 Watt
Derate above 25°C	2.86 mW/°C
Total Dissipation @ T_C = 25°C	1.6 Watts
Derate above 25°C	9.1 mW/°C
Total Dissipation @ T_A = 25°C (both sides)	0.6 Watt
Derate above 25°C	3.43 mW/°C
Total Dissipation @ T_C = 25°C	3.0 Watts
Derate above 25°C	17.2 mW/°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Min	Max	Unit	Conditions
BV_{CEO}*	40	–	Volts	I_C = 20 mA, I_B = 0*
BV_{CBO}	75	–	Volts	(2N2480) I_C = 100 μA, I_E = 0
	80	–	Volts	(2N2480A)
BV_{EBO}	5.0	–	Volts	I_E = 100 μA, I_C = 0
I_{CBO}	–	15	μA	V_{CB} = 30 Volts, I_E = 0, T_A = 150°C
	–	0.050	μA	(2N2480) V_{CB} = 60 Volts, I_E = 0
	–	0.020	μA	(2N2480A)
I_{EBO}	–	50	nA	(2N2480) V_{BE} = 5.0 Volts, I_C = 0
	–	20	nA	(2N2480A)
h_{FE}	20	–	–	(2N2480) I_C = 100 μA, V_{CE} = 5.0 Volts
	35	–	–	(2N2480A)
h_{FE}	30	350	–	(2N2480) I_C = 1.0 mA, V_{CE} = 5.0 Volts
	50	200	–	(2N2480A)

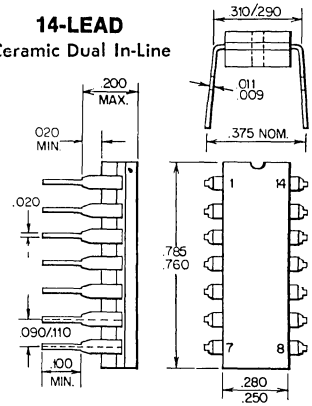
ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Min	Max	Unit	Conditions
$V_{CE(sat)}$	–	1.2	Volts	(2N2480) I_C = 50 mA, I_B = 5.0 mA
	–	1.3	Volts	(2N2480A)
$V_{BE(sat)}$	–	0.9	Volt	(2N2480) I_C = 50 mA, I_B = 5.0 mA
	–	1.0	Volt	(2N2480A)
f_T	50	–	MHz	I_C = 50 mA, V_{CE} = 10 Volts, f = 20 MHz
C_{ob}	–	20	pF	(2N2480) V_{CB} = 10 Volts, I_E = 0
	–	18	pF	(2N2480A) f = 1.0 MHz
C_{ib}	–	85	pF	(2N2480A) V_{BE} = 0.5 Volt, I_C = 0, f = 1.0 MHz
h_{ie}	1000	5000	ohms	(2N2480A) I_C = 1.0 mA, V_{CE} = 5.0 Volts, f = 1.0 kHz
h_{ib}	20	35	ohms	(2N2480A) I_C = 1.0 mA, V_{CB} = 5.0 Volts, f = 1.0 kHz
h_{fe}	50	300	–	(2N2480A) I_C = 1.0 mA, V_{CE} = 5.0 Volts, f = 1.0 kHz
h_{oe}	4.0	16	umhos	(2N2480A) I_C = 1.0 mA, V_{CE} = 5.0 Volts, f = 1.0 kHz
NF	–	8.0	dB	I_C = 0.3 mA, V_{CE} = 10 Volts, R_S = 510 ohms, f = 1.0 kHz, BW = 1.0 Hz

* Pulse Test: Pulse Width $\leq$ 300μs, Duty Cycle $\leq$ 2%.

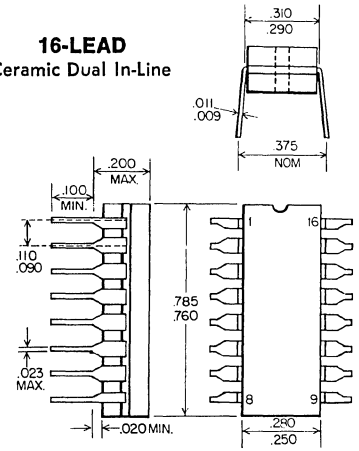
DIMENSIONS

14-LEAD
Ceramic Dual In-Line



NOTE: 1. Board drilling dimensions should equal your practice for a conventional .020 inch diameter lead.

16-LEAD
Ceramic Dual In-Line



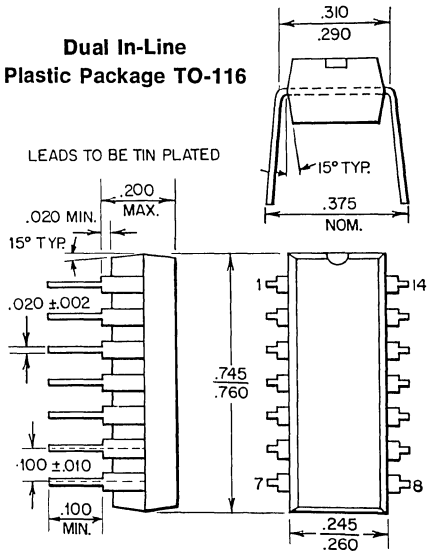
ORDERING CODE FOR 930 DTL, 9000 TTL, 9300 TTL, 950 CTL AND LINEAR CIRCUITS

Operating Temperature Range (add)
−1 for −55 to +125°C
−5 for 0 to +70°C
+75°C for digital

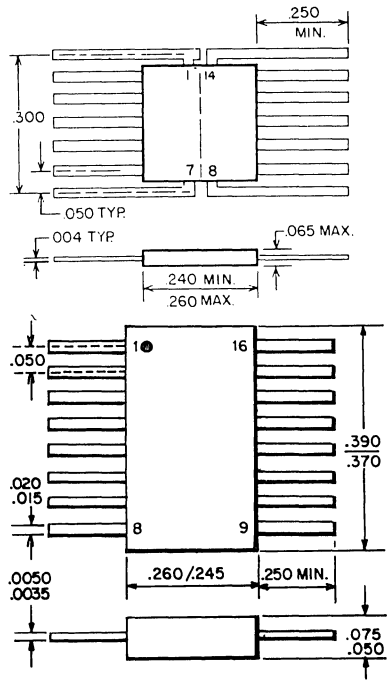
Package (add)
B for Flat Pack
C for TO-5 Style
D for Ceramic Dual In-Line
P for Plastic Dual In-Line

Example:
MIC 709A-1D
is −55 to +125°C
Range in Dual In-Line Package

Dual In-Line
Plastic Package TO-116



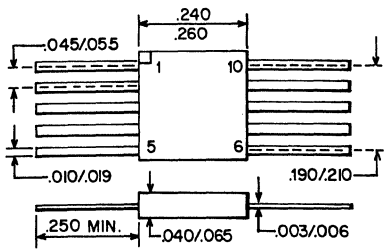
DIMENSIONS — FLAT PACK



16 LEAD—check factory for availability

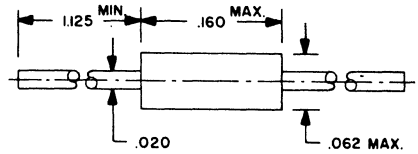
PACKAGE DIMENSIONS

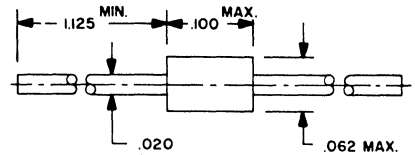
DIMENSIONS



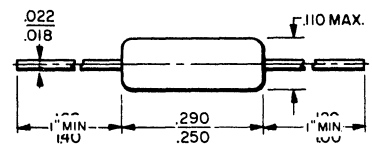
DOUBLE PLUG DIODE

STANDARD

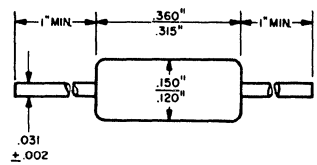




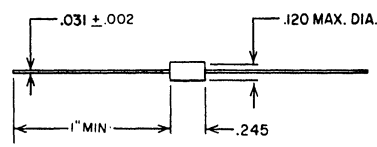
AVAILABLE



DO-7



DO-29



EPOXY PACKAGE

Lead-Material Silver Plated Copper

MECHANICAL DATA

Case: Hermetically sealed glass

Finish: All external surfaces corrosion resistant and leads readily solderable

Leads: Dumet, tin plated

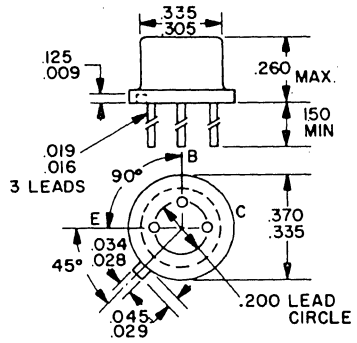
Weight: 0.135 grams (approx.)

Mounting Position: Any

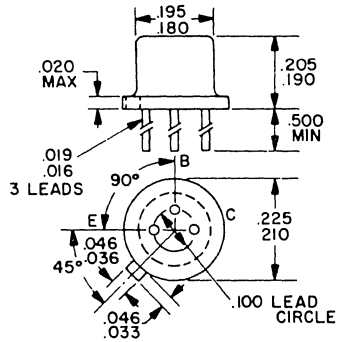
Marking: Diodes carry ITT identification, and are EIA Color Coded. Bands 1, 2, 3 and 4 on the illustration above indicate the first, second, third and fourth digit respectively of the type designation starting from the cathode end of the diode.

Black	0	Green	5
Brown	1	Blue	6
Red	2	Violet	7
Orange	3	Gray	8
Yellow	4	White	9

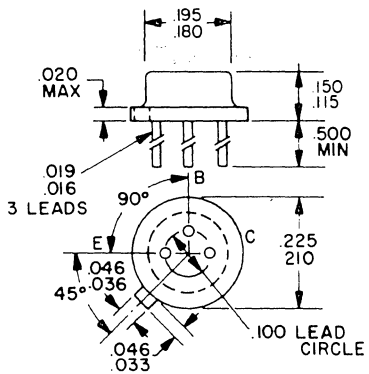
PHYSICAL DIMENSIONS



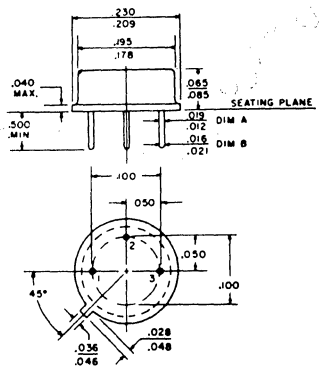
TO-5



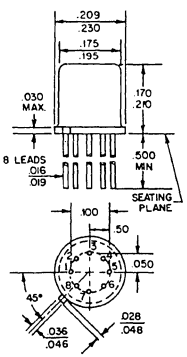
TO-18



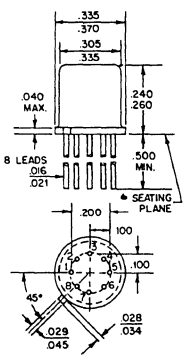
TO-52



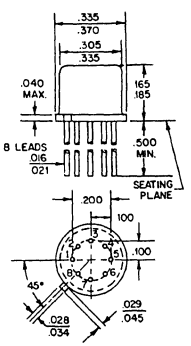
TO-46



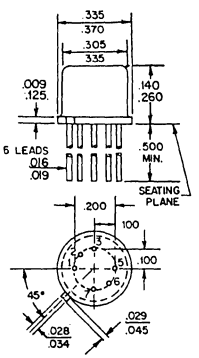
TO-71



TO-77



TO-78



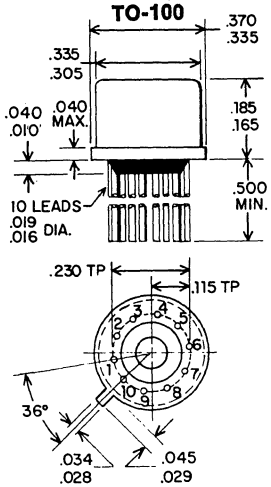
R-131c

NOTE: DIMENSIONS AS PER LATEST JS-10 COMMITTEE.

ALL DIMENSIONS IN INCHES.
LEADS ARE GOLD-PLATED KOVAR.

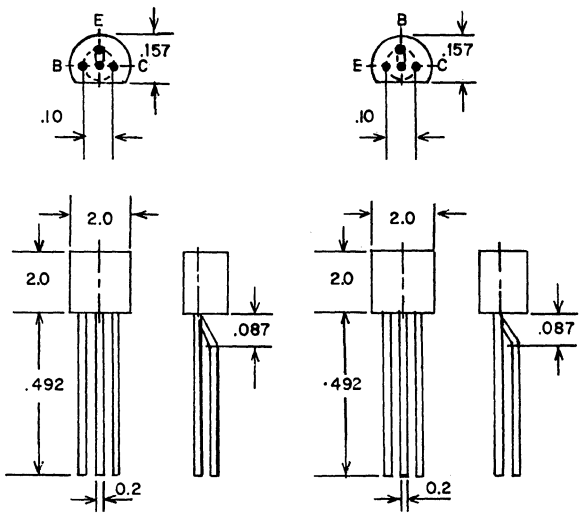
PACKAGE DIMENSIONS

DIMENSIONS
TO-100

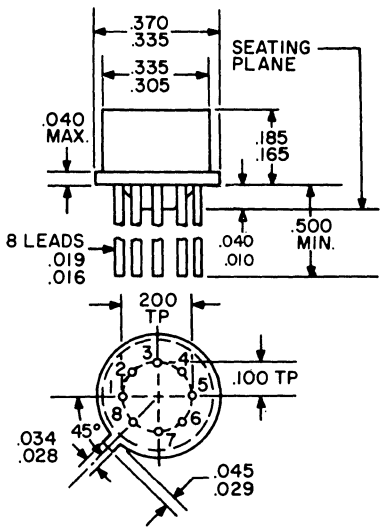


NOTES: LEADS ARE GOLD-PLATED KOVAR
PACKAGE WEIGHT IS 1.32 GRAMS

TO-92 PACKAGE



TO-99



NOTE: DIMENSIONS AS PER LATEST JS-10 COMMITTEE.
ALL DIMENSIONS IN INCHES.
LEADS ARE GOLD-PLATED KOVAR.
PACKAGE WEIGHT IS 1.12 GRAMS.

NOTE-ON SPECIAL ORDER

ITT Semiconductors will provide TO-18, TO-46 and TO-52 units with formed leads to the requirements of the TO-5 package. In addition disc insulators on the above devices are also available by special order.

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2N 5087	177
2N 5209	63
2N 5210	63
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2N 5221	178
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2N 5224	147
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2N 5227	180
2N 5228	209
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2N 5369	68
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